

54F/74F189 64-Bit Random Access Memory with TRI-STATE® Outputs

General Description

The 'F189 is a high-speed 64-bit RAM organized as a 16-word by 4-bit array. Address inputs are buffered to minimize loading and are fully decoded on-chip. The outputs are TRI-STATE and are in the high impedance state whenever the Chip Select ($\overline{CS}$) input is HIGH. The outputs are active only in the Read mode and the output data is the complement of the stored data.

Features

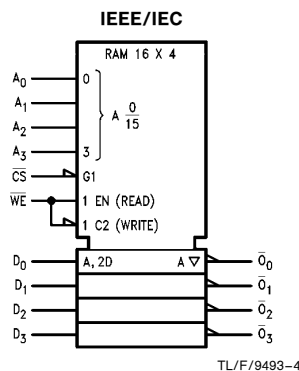
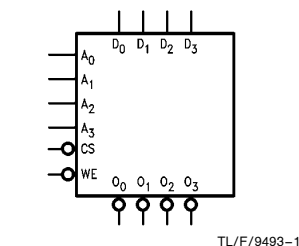
- TRI-STATE outputs for data bus applications
- Buffered inputs minimize loading
- Address decoding on-chip
- Diode clamped inputs minimize ringing
- Available in SOIC, (300 mil only)

Commercial	Military	Package Number	Package Description
74F189PC		N16E	16-Lead (0.300" Wide) Molded Dual-In-Line
	54F189DL (Note 2)	J16A	16-Lead Ceramic Dual-In-Line
74F189SC (Note 1)		M16A	16-Lead (0.150" Wide) Molded Small Outline, JEDEC
74F189SJ (Note 1)		M16D	16-Lead (0.300" Wide) Molded Small Outline, EIAJ
	54F189FL (Note 2)	W16A	16-Lead Cerpack
	54F189LL (Note 2)	E20A	20-Lead Ceramic Leadless Chip Carrier, Type C

Note 1: Devices also available in 13" reel. Use suffix = SCX and SJX.

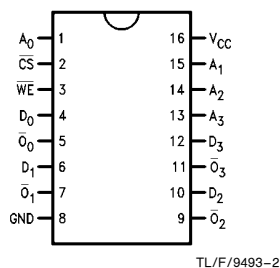
Note 2: Military grade device with environmental and burn-in processing. Use suffix = DLQB, FLQB and LLQB.

Logic Symbols

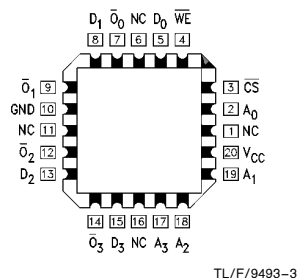


Connection Diagrams

Pin Assignment for DIP, SOIC and Flatpak



Pin Assignment for LCC



TRI-STATE® is a registered trademark of National Semiconductor Corporation.

Unit Loading/Fan Out

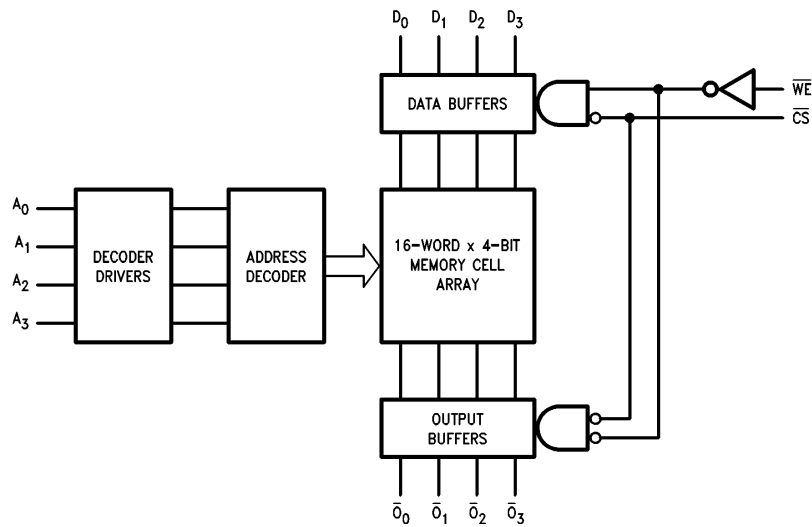
Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
A_0-A_3	Address Inputs	1.0/1.0	20 μA / -0.6 mA
$\overline{CS}$	Chip Select Input (Active LOW)	1.0/1.0	20 μA / -1.2 mA
$\overline{WE}$	Write Enable Input (Active LOW)	1.0/1.0	20 μA / -0.6 mA
D_0-D_3	Data Inputs	1.0/1.0	20 μA / -0.6 mA
$\overline{O}_0-\overline{O}_3$	Inverted Data Outputs	150/40 (33.3)	-3.0 mA/24 mA (20 mA)

Function Table

Inputs		Operation	Condition of Outputs
$\overline{CS}$	$\overline{WE}$		
L	L	Write	High Impedance
L	H	Read	Complement of Stored Data
H	X	Inhibit	High Impedance

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Block Diagram



TL/F/9493-5

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C
Plastic	−55°C to +150°C
V _{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V _{CC} = 0V)	
Standard Output	−0.5V to V _{CC}
TRI-STATE Output	−0.5V to +5.5V

Current Applied to Output in LOW State (Max) twice the rated I_{OL} (mA)

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	−55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

DC Electrical Characteristics

Symbol	Parameter		54F/74F			Units	V _{CC}	Conditions
			Min	Typ	Max			
V _{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V _{IL}	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
V _{CD}	Input Clamp Diode Voltage				−1.2	V	Min	I _{IN} = −18 mA
V _{OH}	Output HIGH Voltage	54F 10% V _{CC} 54F 10% V _{CC} 74F 10% V _{CC} 74F 10% V _{CC} 74F 5% V _{CC} 74F 5% V _{CC}	2.5 2.4 2.5 2.4 2.7 2.7			V	Min	I _{OH} = −1 mA I _{OH} = −3 mA I _{OH} = −1 mA I _{OH} = −3 mA I _{OH} = −1 mA I _{OH} = −3 mA
V _{OL}	Output LOW Voltage	54F 10% V _{CC} 74F 10% V _{CC}			0.5 0.5	V	Min	I _{OL} = 20 mA I _{OL} = 24 mA
I _{IH}	Input HIGH Current	54F 74F			20.0 5.0	μA	Max	V _{IN} = 2.7V
I _{BVI}	Input HIGH Current Breakdown Test	54F 74F			100 7.0	μA	Max	V _{IN} = 7.0V
I _{CEX}	Output HIGH Leakage Current	54F 74F			250 50	μA	Max	V _{OUT} = V _{CC}
V _{ID}	Input Leakage Test	74F	4.75			V	0.0	I _{ID} = 1.9 μA All Other Pins Grounded
I _{OD}	Output Leakage Circuit Current	74F			3.75	μA	0.0	V _{IOD} = 150 mV All Other Pins Grounded
I _{IL}	Input LOW Current				−0.6 −1.2	mA	Max	V _{IN} = 0.5V (except $\overline{CS}$) V _{IN} = 0.5V ($\overline{CS}$)
I _{OZH}	Output Leakage Current				50	μA	Max	V _{OUT} = 2.7V
I _{OZL}	Output Leakage Current				−50	μA	Max	V _{OUT} = 0.5V
I _{OS}	Output Short-Circuit Current		−60		−150	mA	Max	V _{OUT} = 0V
I _{ZZ}	Bus Drainage Test				500	μA	0.0V	V _{OUT} = 5.25V
I _{CCZ}	Power Supply Current			37	55	mA	Max	V _O = HIGH Z

AC Electrical Characteristics

Symbol	Parameter	74F			54F		74F		Units
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$*T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$		
		Min	Typ	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Access Time, HIGH or LOW A_n to $\overline{O}_n$	10.0 8.0	18.5 13.5	26.0 19.0	9.0 8.0	32.0 23.0	10.0 8.0	27.0 20.0	ns
t_{PZH} t_{PZL}	Access Time, HIGH or LOW $\overline{CS}$ to $\overline{O}_n$	3.5 5.0	6.0 9.0	8.5 13.0	3.5 5.0	10.5 15.0	3.5 5.0	9.5 14.0	ns
t_{PHZ} t_{PLZ}	Disable Time, HIGH or LOW $\overline{CS}$ to $\overline{O}_n$	2.0 3.0	4.0 5.5	6.0 8.0	2.0 2.5	8.0 10.0	2.0 3.0	7.0 9.0	ns
t_{PZH} t_{PZL}	Write Recovery Time, HIGH or LOW $\overline{WE}$ to $\overline{O}_n$	6.5 6.5	15.0 11.0	28.0 15.5	6.5 6.5	37.5 17.5	6.5 6.5	29.0 16.5	ns
t_{PHZ} t_{PLZ}	Disable Time, HIGH or LOW $\overline{WE}$ to $\overline{O}_n$	4.0 5.0	7.0 9.0	10.0 13.0	3.5 5.0	12.0 15.0	4.0 5.0	11.0 14.0	ns

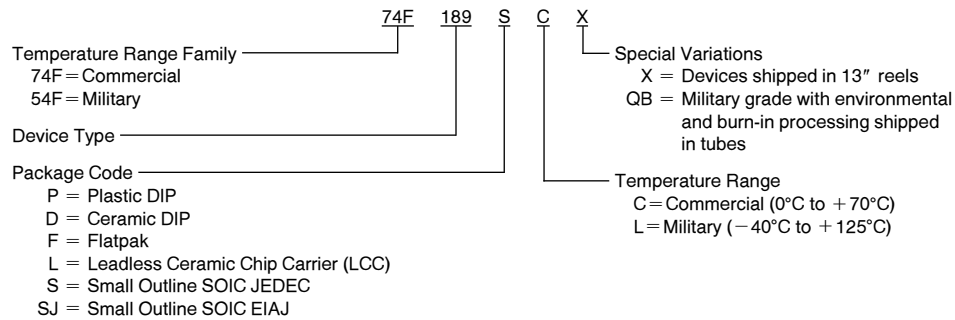
AC Operating Requirements

Symbol	Parameter	74F		54F		74F		Units
		T _A = +25°C V _{CC} = +5.0V		*T _A , V _{CC} = Mil		T _A , V _{CC} = Com		
		Min	Max	Min	Max	Min	Max	
t _S (H) t _S (L)	Setup Time, HIGH or LOW A _n to $\overline{WE}$	0 0		0 0		0 0		ns
t _H (H) t _H (L)	Hold Time, HIGH or LOW A _n to $\overline{WE}$	2.0 2.0		2.0 2.0		2.0 2.0		
t _S (H) t _S (L)	Setup Time, HIGH or LOW D _n to $\overline{WE}$	10.0 10.0		11.0 11.0		10.0 10.0		ns
t _H (H) t _H (L)	Hold Time, HIGH or LOW D _n to $\overline{WE}$	0 0		2.0 2.0		0 0		
t _S (L)	Setup Time, LOW $\overline{CS}$ to $\overline{WE}$	0		0		0		ns
t _H (L)	Hold Time, LOW $\overline{CS}$ to $\overline{WE}$	6.0		7.5		6.0		
t _W (L)	$\overline{WE}$ Pulse Width, LOW	6.0		15.0		6.0		ns

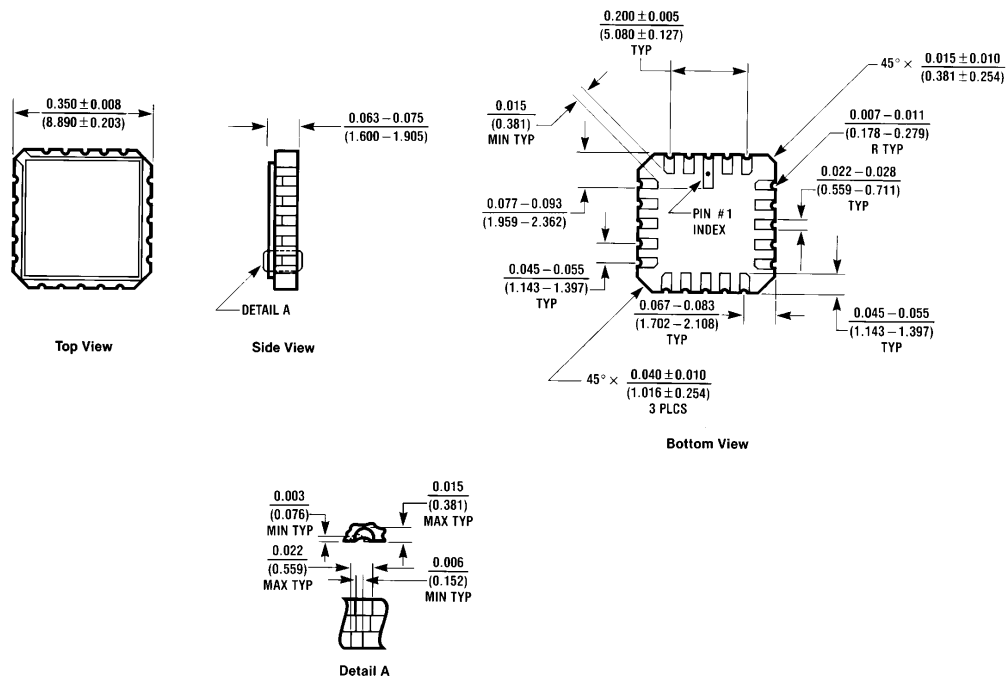
$*T_A = -55^{\circ}\text{C}$ to $+125^{\circ}\text{C}$

Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



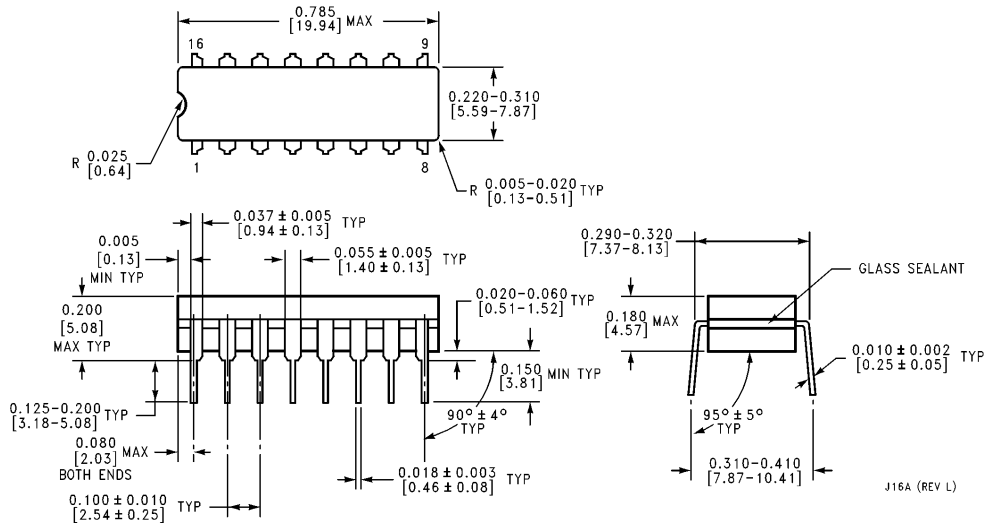
Physical Dimensions inches (millimeters)



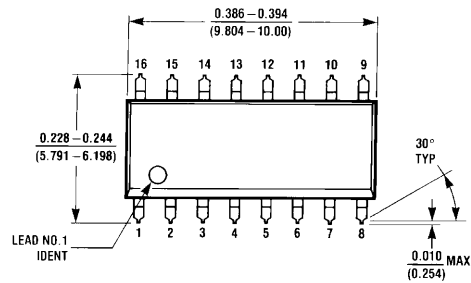
**20-Lead Ceramic Leadless Chip Carrier (L)
NS Package Number E20A**

E20A (REV D)

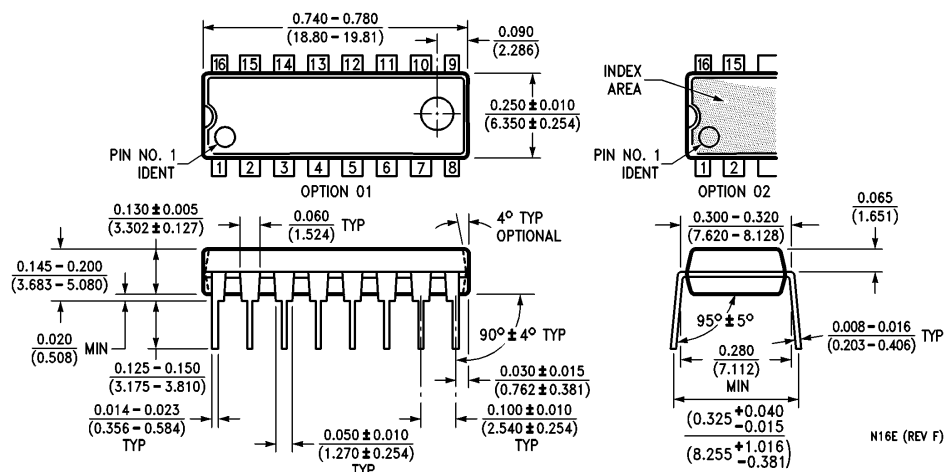
Physical Dimensions inches (millimeters) (Continued)



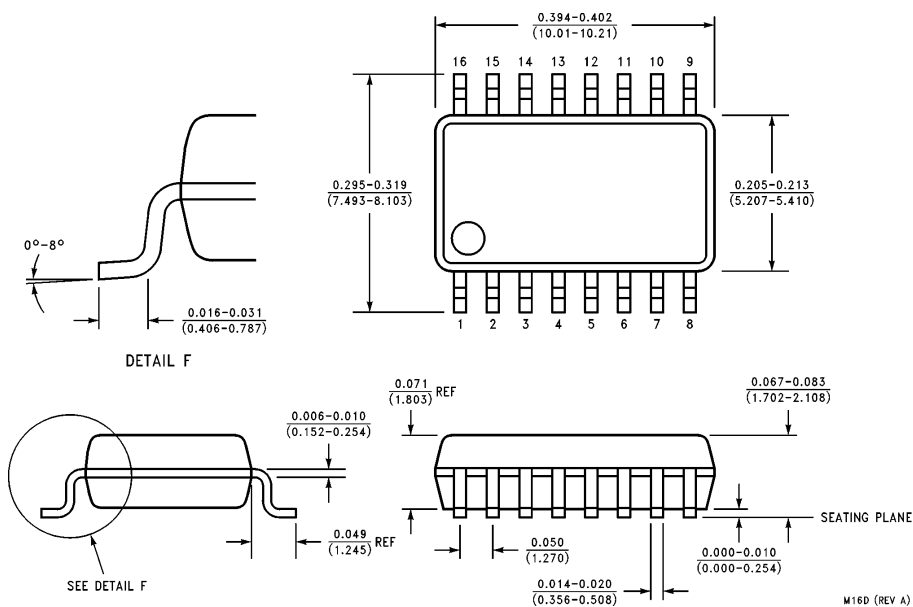
16-Lead Ceramic Dual-In-Line Package (D)
NS Package Number J16A



16-Lead (0.150" Wide) Molded Small Outline Package, JEDEC (S)
NS Package Number M16A

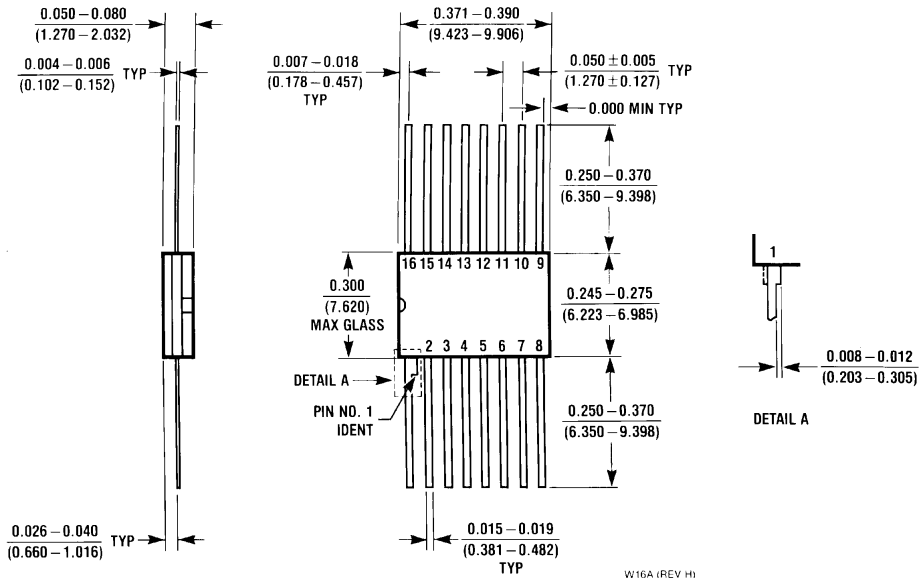
Physical Dimensions inches (millimeters) (Continued)

16-Lead (0.300" Wide) Molded Dual-In-Line Package (P)
NS Package Number N16E



**16-Lead (0.300" Wide) Molded Small Outline Package, EIAJ (SJ)
NS Package Number M16D**

Physical Dimensions inches (millimeters) (Continued)



16 Lead Ceramic Flatpak (F)
NS Package Number W16A

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.



National Semiconductor Corporation
1111 West Bardin Road
Arlington, TX 76017
Tel: 1(800) 272-9959
Fax: 1(800) 737-7018

National Semiconductor Europe
Fax: (+49) 0-180-530 85 86
Email: cnjwge@tevm2.nsc.com
Deutsch Tel: (+49) 0-180-530 85 85
English Tel: (+49) 0-180-532 78 32
Français Tel: (+49) 0-180-532 93 58
Italiano Tel: (+49) 0-180-534 16 80

National Semiconductor Hong Kong Ltd.
19th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 2737-1600
Fax: (852) 2736-9960

National Semiconductor Japan Ltd.
Tel: 81-043-299-2309
Fax: 81-043-299-2408

National does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and National reserves the right at any time without notice to change said circuitry and specifications.