

54F/74F253

Dual 4-Input Multiplexer with TRI-STATE® Outputs

General Description

The 'F253 is a dual 4-input multiplexer with TRI-STATE® outputs. It can select two bits of data from four sources using common select inputs. The output may be individually switched to a high impedance state with a HIGH on the respective Output Enable ($\overline{OE}$) inputs, allowing the outputs to interface directly with bus oriented systems.

Features

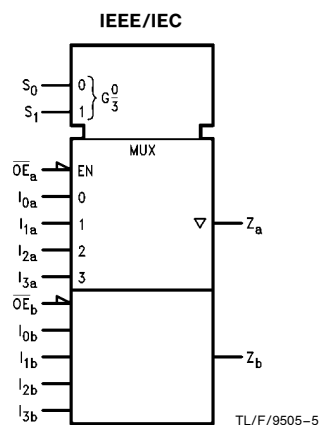
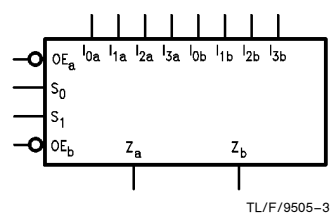
- Multifunction capability
- Non-inverting TRI-STATE outputs
- Guaranteed 4000V minimum ESD protection

Commercial	Military	Package Number	Package Description
74F253PC		N16E	16-Lead (0.300" Wide) Molded Dual-In-Line
	54F253DM (Note 2)	J16A	16-Lead Ceramic Dual-In-Line
74F253SC (Note 1)		M16A	16-Lead (0.150" Wide) Molded Small Outline, JEDEC
74F253SJ (Note 1)		M16D	16-Lead (0.300" Wide) Molded Small Outline, EIAJ
	54F253FM (Note 2)	W16A	16-Lead Cerpack
	54F253LL (Note 2)	E20A	20-Lead Ceramic Leadless Chip Carrier, Type C

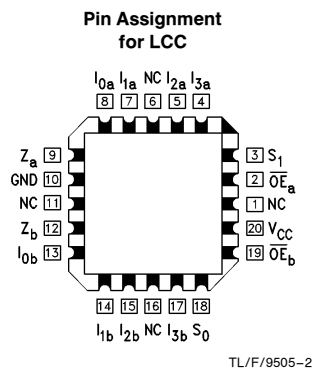
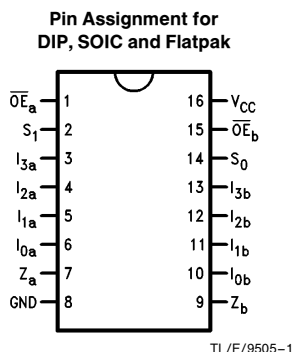
Note 1: Devices also available in 13" reel. Use suffix = SCX and SJX.

Note 2: Military grade device with environmental and burn-in processing. Use suffix = DMQB, FMQB and LMQB.

Logic Symbols



Connection Diagrams



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Unit Loading/Fan Out

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
$I_{0a}-I_{3a}$	Side A Data Inputs	1.0/1.0	20 μ A/ -0.6 mA
$I_{0b}-I_{3b}$	Side B Data Inputs	1.0/1.0	20 μ A/ -0.6 mA
S_0-S_1	Common Select Inputs	1.0/1.0	20 μ A/ -0.6 mA
$\overline{OE}_a$	Side A Output Enable Input (Active LOW)	1.0/1.0	20 μ A/ -0.6 mA
$\overline{OE}_b$	Side B Output Enable Input (Active LOW)	1.0/1.0	20 μ A/ -0.6 mA
Z_a, Z_b	TRI-STATE Outputs	150/40(33.3)	-3 mA/24 mA (20 mA)

Functional Description

This device contains two identical 4-input multiplexers with TRI-STATE outputs. They select two bits from four sources selected by common Select inputs (S_0, S_1). The 4-input multiplexers have individual Output Enable ($\overline{OE}_a, \overline{OE}_b$) inputs which, when HIGH, force the outputs to a high impedance (High Z) state. This device is the logic implementation of a 2-pole, 4-position switch, where the position of the switch is determined by the logic levels supplied to the two select inputs. The logic equations for the outputs are shown below:

$$Z_a = \overline{OE}_a \cdot (I_{0a} \cdot S_1 \cdot \overline{S_0} + I_{1a} \cdot \overline{S_1} \cdot S_0 + I_{2a} \cdot S_1 \cdot \overline{S_0} + I_{3a} \cdot \overline{S_1} \cdot S_0)$$

$$Z_b = \overline{OE}_b \cdot (I_{0b} \cdot S_1 \cdot \overline{S_0} + I_{1b} \cdot \overline{S_1} \cdot S_0 + I_{2b} \cdot S_1 \cdot \overline{S_0} + I_{3b} \cdot \overline{S_1} \cdot S_0)$$

If the outputs of TRI-STATE devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Output Enable signals to TRI-STATE devices whose outputs are tied together are designed so that there is no overlap.

Truth Table

Select Inputs		Data Inputs				Output Enable	Output
S_0	S_1	I_0	I_1	I_2	I_3	$\overline{OE}$	$\overline{Z}$
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
H	L	X	L	X	X	L	L
H	L	X	H	X	X	L	H
L	H	X	X	L	X	L	L
L	H	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Address inputs S_0 and S_1 are common to both sections.

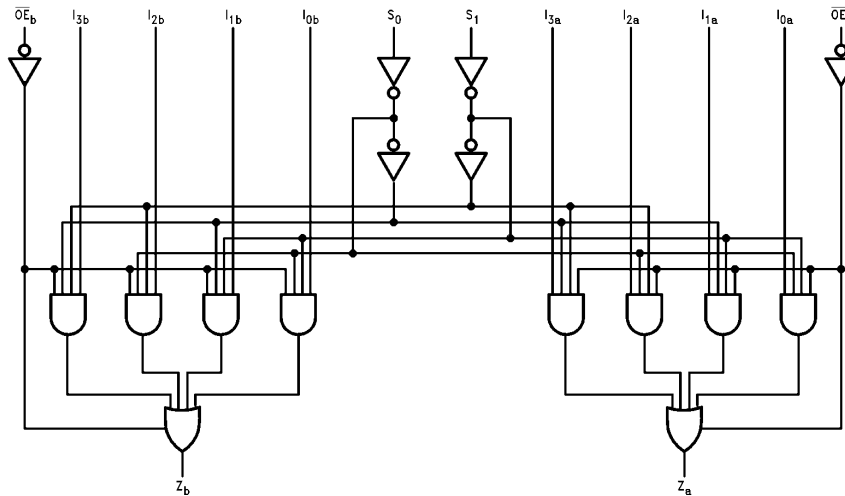
H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

Z = High Impedance

Logic Diagram



TL/F/9505-4

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C
Plastic	−55°C to +150°C
V _{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V _{CC} = 0V)	
Standard Output	−0.5V to V _{CC}
TRI-STATE Output	−0.5V to +5.5V

Current Applied to Output in LOW State (Max) twice the rated I_{OL} (mA)

ESD Last Passing Voltage (Min) 4000V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	−55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

DC Electrical Characteristics

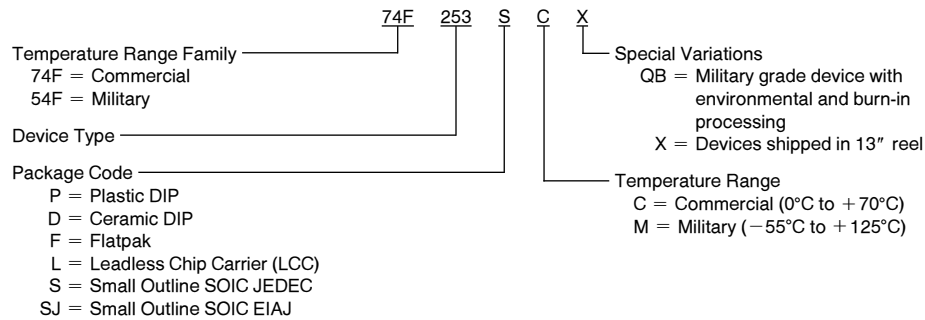
Symbol	Parameter		54F/74F			Units	V _{CC}	Conditions
			Min	Typ	Max			
V _{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V _{IL}	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
V _{CD}	Input Clamp Diode Voltage				−1.2	V	Min	I _{IN} = −18 mA
V _{OH}	Output HIGH Voltage	54F 10% V _{CC}	2.5			V	Min	I _{OH} = −1 mA
		54F 10% V _{CC}	2.4					I _{OH} = −3 mA
		74F 10% V _{CC}	2.5					I _{OH} = −1 mA
		74F 10% V _{CC}	2.4					I _{OH} = −3 mA
		74F 5% V _{CC}	2.7					I _{OH} = −1 mA
		74F 5% V _{CC}	2.7					I _{OH} = −3 mA
V _{OL}	Output LOW Voltage	54F 10% V _{CC}			0.5	V	Min	I _{OL} = 20 mA
		74F 10% V _{CC}			0.5			I _{OL} = 24 mA
I _{IH}	Input HIGH Current	54F			20.0	μA	Max	V _{IN} = 2.7V
		74F			5.0			
I _{BVI}	Input HIGH Current Breakdown Test	54F			100	μA	Max	V _{IN} = 7.0V
		74F			7.0			
I _{CEX}	Output HIGH Leakage Current	54F			250	μA	Max	V _{OUT} = V _{CC}
		74F			50			
V _{ID}	Input Leakage Test	74F	4.75			V	0.0	I _{ID} = 1.9 μA All Other Pins Grounded
I _{OD}	Output Leakage Circuit Current	74F			3.75	μA	0.0	V _{IOD} = 150 mV All Other Pins Grounded
I _{IL}	Input LOW Current				−0.6	mA	Max	V _{IN} = 0.5V
I _{OZH}	Output Leakage Current				50	μA	Max	V _{OUT} = 2.7V
I _{OZL}	Output Leakage Current				−50	μA	Max	V _{OUT} = 0.5V
I _{OS}	Output Short-Circuit Current		−60 −100	−150 −225		mA	Max	V _{OUT} = 0V V _{OUT} = 0V
I _{ZZ}	Bus Drainage Test				500	μA	0.0V	V _{OUT} = V _{CC}
I _{CCH}	Power Supply Current			11.5	16	mA	Max	V _O = HIGH
I _{CCL}	Power Supply Current			16	23	mA	Max	V _O = LOW
I _{CCZ}	Power Supply Current			16	23	mA	Max	V _O = HIGH Z

AC Electrical Characteristics

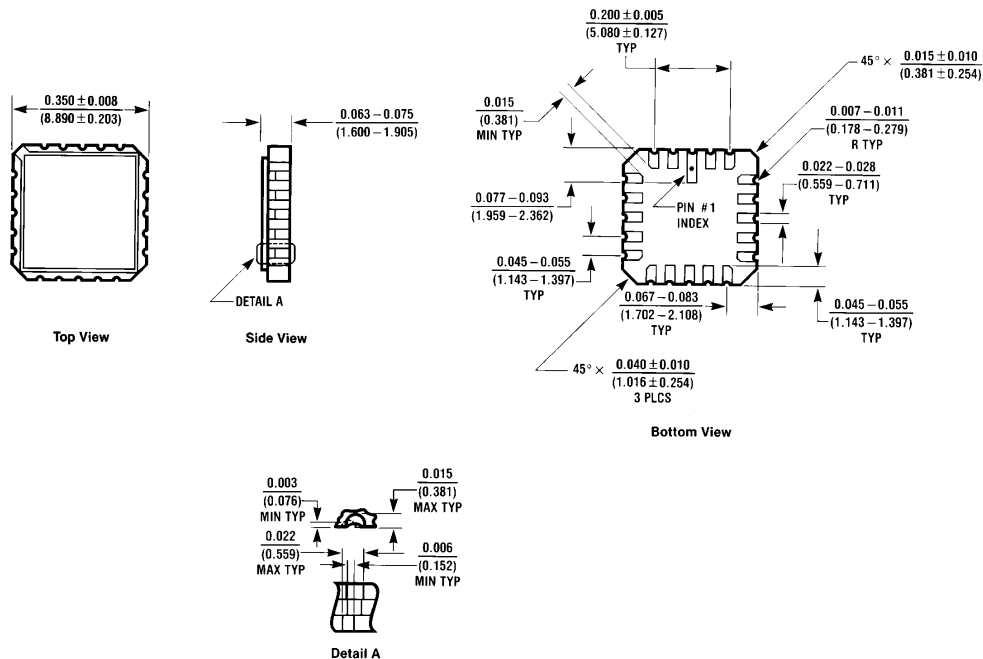
Symbol	Parameter	74F			54F		74F		Units
		T _A = +25°C V _{CC} = +5.0V C _L = 50 pF			T _A , V _{CC} = Mil C _L = 50 pF		T _A , V _{CC} = Com C _L = 50 pF		
		Min	Typ	Max	Min	Max	Min	Max	
t _{PLH} t _{PHL}	Propagation Delay S _n to Z _n	4.5 3.0	8.5 6.5	11.5 9.0	3.5 2.5	15.0 11.0	4.5 3.0	13.0 10.0	ns
t _{PLH} t _{PHL}	Propagation Delay I _n to Z _n	3.0 2.5	5.5 4.5	7.0 6.0	2.5 2.5	9.0 8.0	3.0 2.5	8.0 7.0	ns
t _{PZH} t _{PZL}	Output Enable Time	3.0 3.0	6.0 6.0	8.0 8.0	2.5 2.5	10.0 10.0	3.0 3.0	9.0 9.0	ns
t _{PHZ} t _{PLZ}	Output Disable Time	2.0 2.0	3.7 4.4	5.0 6.0	2.0 2.0	6.5 8.0	2.0 2.0	6.0 7.0	

Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



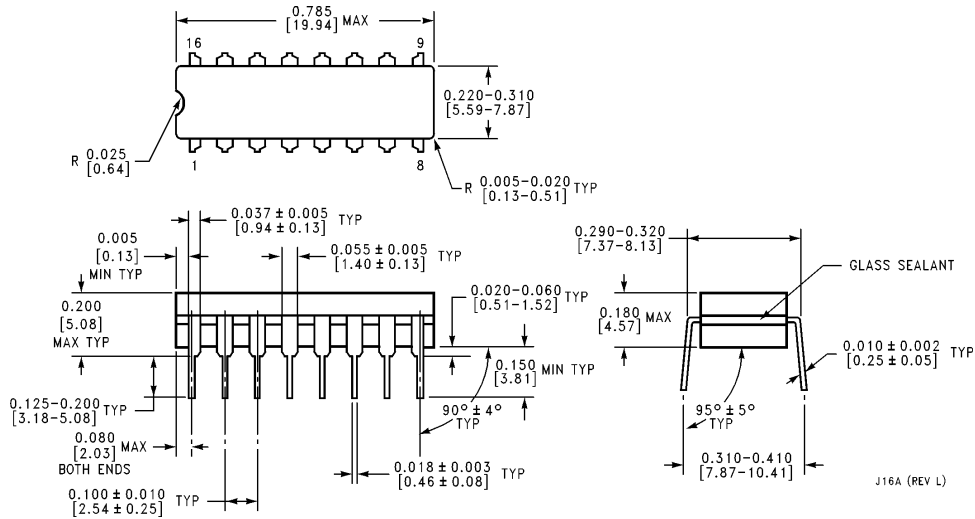
Physical Dimensions inches (millimeters)



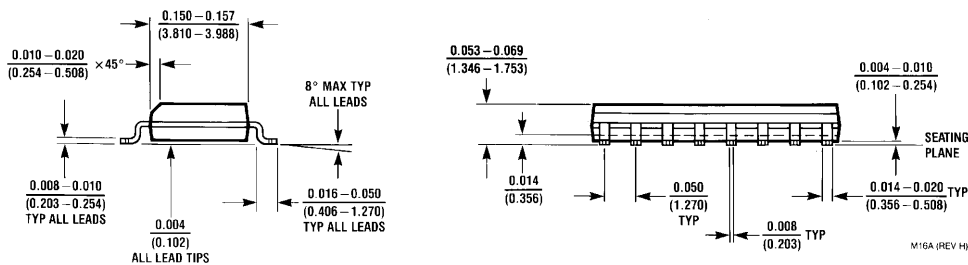
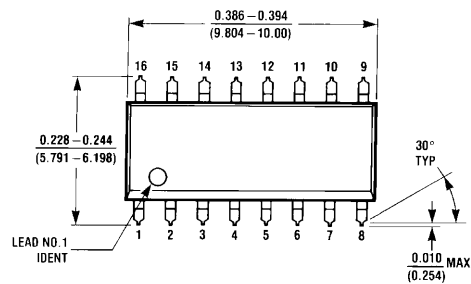
**20-Lead Ceramic Leadless Chip Carrier (L)
NS Package Number E20A**

E20A (REV D)

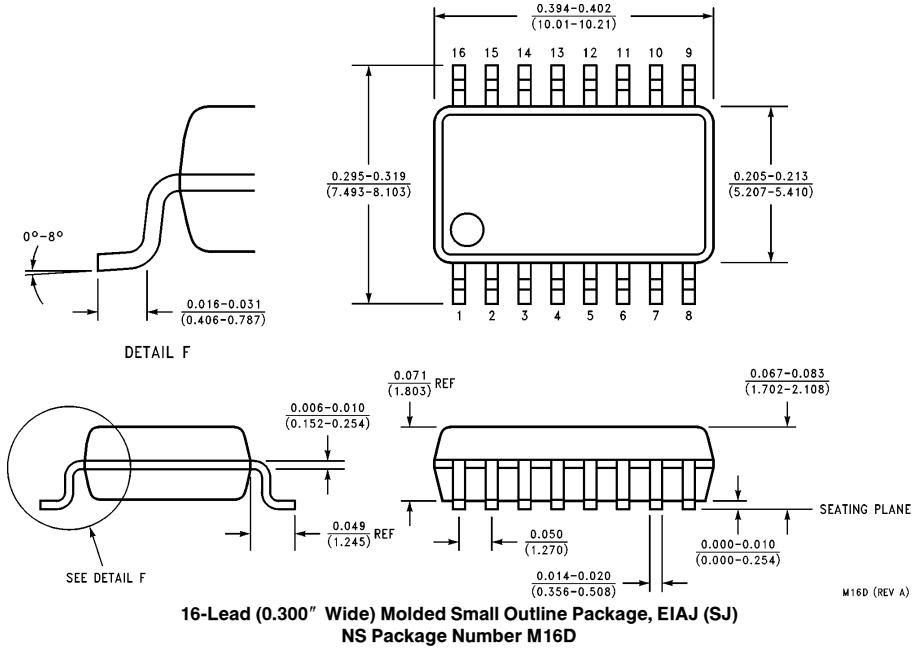
Physical Dimensions inches (millimeters) (Continued)



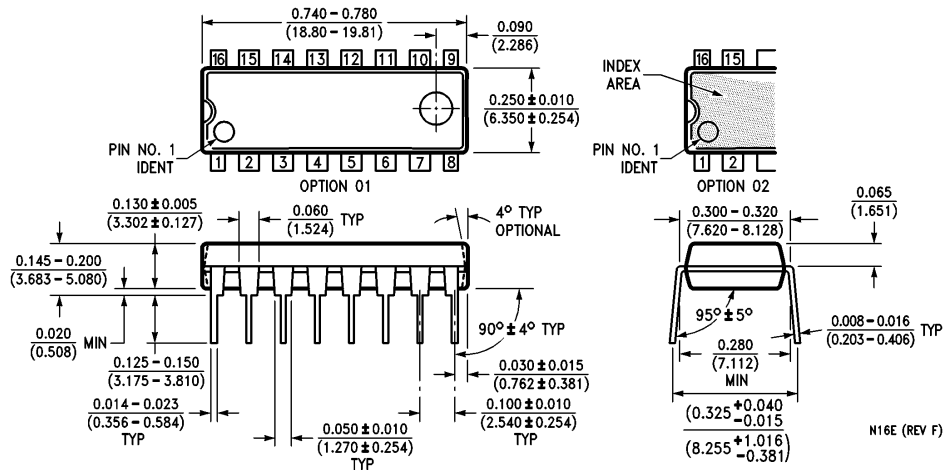
16-Lead Ceramic Dual-In-Line Package (D)
NS Package Number J16A



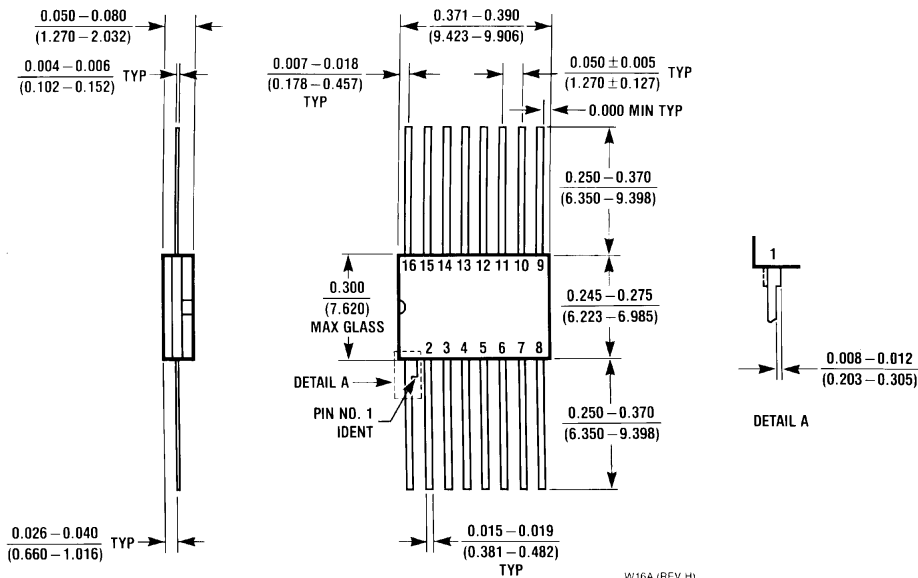
16-Lead (0.150" Wide) Molded Small Outline Package, JEDEC (S)
NS Package Number M16A

Physical Dimensions inches (millimeters) (Continued)

**16-Lead (0.300" Wide) Molded Small Outline Package, EIAJ (SJ)
NS Package Number M16D**



**16-Lead (0.300" Wide) Molded Dual-In-Line Package (P)
NS Package Number N16E**

Physical Dimensions inches (millimeters) (Continued)

16-Lead Ceramic Flatpak (F)
NS Package Number W16A

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