National Semiconductor

PRELIMINARY
November 1996

74LVT162245
3.3V ABT 16-Bit Transceiver with TRI-STATE® Outputs

General Description

The LVT162245 contains sixteen non-inverting bidirectional buffers with TRI-STATE outputs and is intended for bus oriented applications. The device is byte controlled. Each byte has separate control inputs which can be shorted together for full 16-bit operation. The $T/\overline{R}$ inputs determine the direction of data flow through the device. The $\overline{OE}$ inputs disable both the A and B ports by placing them in a high impedance state.

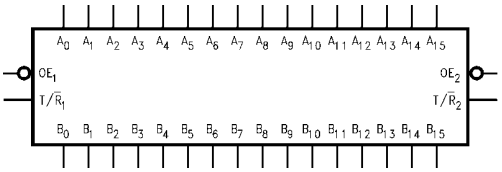
The LVT162245 is designed with equivalent 25Ω series resistance in both the High and Low states of the output. This design reduces line noise in applications such as memory address drivers, clock drivers, and bus transceivers/transmitters.

This non-inverting transceiver is designed for low-voltage (3.3V) V_{CC} applications, but with the capability to provide a TTL interface to a 5V environment. The LVT162245 is fabricated with an advanced BiCMOS technology to achieve high speed operation similar to 5V ABT while maintaining a low power dissipation.

Features

- Input and output interface capability to systems at 5V V_{CC}
- Bus-Hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power Up/Down high impedance provides glitch-free bus loading
- Outputs include equivalent series resistance of 25Ω making external termination resistors unnecessary and reducing overshoot and undershoot
- Available in SSOP and TSSOP
- Functionally compatible with the 74 series 162245
- Latch-up performance exceeds 500 mA

Logic Symbol



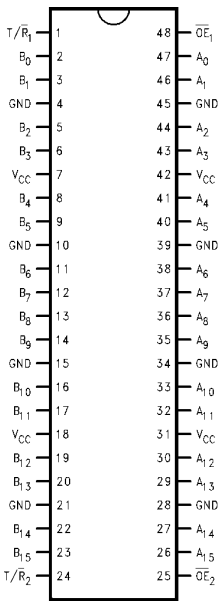
TL/F/12446–1

Pin Names	Description
$\overline{OE}_n$	Output Enable Input (Active Low)
$T/\overline{R}_n$	Transmit/Receive Input
A_0–A_{15}	Side A Inputs/TRI-STATE Outputs
B_0–B_{15}	Side B Inputs/TRI-STATE Outputs

	SSOP	TSSOP
Order Number	74LVT162245MEA 74LVT162245MEAX	74LVT162245MTD 74LVT162245MTDX
See NS Package Number	MS48A	MTD48

Connection Diagram

Pin Assignment for SSOP and TSSOP



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Functional Description

The LVT162245 contains sixteen non-inverting bidirectional buffers with TRI-STATE outputs. The device is byte controlled with each byte functioning identically, but independent of the other. The control pins can be shorted together to obtain full 16-bit operation.

Truth Tables

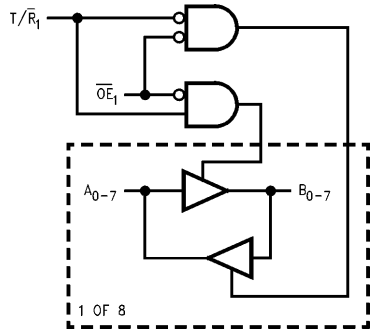
Inputs		Outputs
$\overline{OE}_1$	$T/\overline{R}_1$	
L	L	Bus B_0–B_7 Data to Bus A_0–A_7
L	H	Bus A_0–A_7 Data to Bus B_0–B_7
H	X	HIGH-Z State on A_0–A_7, B_0–B_7

H = High Voltage Level L = Low Voltage Level

Inputs		Outputs
$\overline{OE}_2$	$T/\overline{R}_2$	
L	L	Bus B_8–B_{15} Data to Bus A_8–A_{15}
L	H	Bus A_8–A_{15} Data to Bus B_8–B_{15}
H	X	HIGH-Z State on A_8–A_{15}, B_8–B_{15}

X = Immaterial Z = High Impedance

Logic Diagrams



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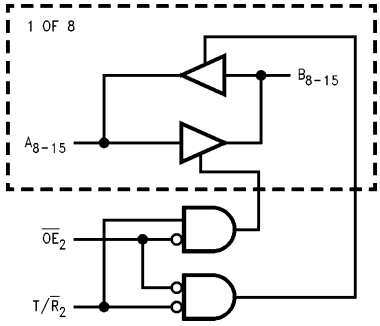

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Please note that these diagrams are provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	−0.5 to +7.0		V
V_I	DC Input Voltage	−0.5 to +7.0		V
V_O	Output Voltage	−0.5 to +7.0	Output in TRI-STATE	V
		−0.5 to +7.0	Output in High or Low State (Note 2)	V
I_{IK}	DC Input Diode Current	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50	V_O < GND	mA
I_O	DC Output Current	64	V_O > V_{CC} Output at HIGH State	mA
		128	V_O > V_{CC} Output at LOW State	
I_{CC}	DC Supply Current per Supply Pin	±64		mA
I_{GND}	DC Ground Current per Ground Pin	±128		mA
T_{STG}	Storage Temperature	−65 to +150		°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: I_O Absolute Maximum Rating must be observed.

Recommended Operating Conditions

Symbol	Symbol		Min	Max	Units
V_{CC}	Supply Voltage	Operating	2.7	3.6	V
		Data Retention	1.5	3.6	
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage	HIGH or LOW State	0	V_{CC}	V
		TRI-STATE	0	5.5	
I_{OH}	High-Level Output Current	B Port		−32	mA
		A Port		−8	
I_{OL}	Low-Level Output Current	B Port		64	mA
		A Port		8	
T_A	Free Air Operating Temperature		−40	+85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V		0	10	ns/V

DC Electrical Characteristics

Symbol	Parameter		V_{CC} (V)	$T_A = -40°C$ to $+85°C$			Units	Conditions
				Min	Typ (Note 3)	Max		
V_{IK}	Input Clamp Diode Voltage		2.7			−1.2	V	$I_I = -18$ mA
V_{IH}	Input HIGH Voltage		2.7–3.6	2.0			V	$V_O \leq 0.1V$ or $V_O \geq V_{CC} - 0.1V$
V_{IL}	Input LOW Voltage		2.7–3.6			0.8		
V_{OH}	Output HIGH Voltage	A Port	3.0	2.0			V	$I_{OH} = -8$ mA
		B Port	2.7–3.6	$V_{CC} - 0.2$			V	$I_{OH} = -100$ μA
			2.7	2.4			V	$I_{OH} = -8$ mA
			3.0	2.0			V	$I_{OH} = -32$ mA
V_{OL}	Output LOW Voltage	A Port	3.0			0.8	V	$I_{OL} = 8$ mA
		B Port	2.7			0.2	V	$I_{OL} = 100$ μA
			2.7			0.5	V	$I_{OL} = 24$ mA
			3.0			0.4	V	$I_{OL} = 16$ mA
			3.0			0.5	V	$I_{OL} = 32$ mA
			3.0			0.55	V	$I_{OL} = 64$ mA
$I_{I(HOLD)}$	Bus-Hold Input Minimum Drive		3.0	75			μA	$V_I = 0.8V$
				−75			μA	$V_I = 2.0V$
$I_{I(OD)}$	Bus-Hold Input Over-Drive Current to Change State		3.0	500			μA	(Note 4)
				−500			μA	(Note 5)
I_I	Input Current		3.6			10	μA	$V_I = 5.5V$
		Control Pins	3.6			±1	μA	$V_I = 0V$ or V_{CC}
		Data Pins	3.6			−5	μA	$V_I = 0V$
						1	μA	$V_I = V_{CC}$
I_{OFF}	Power Off Leakage Current		0			±100	μA	$0V \leq V_I$ or $V_O \leq 5.5V$
$I_{PU/PD}$ (Note 6)	Power Up/Down TRI-STATE Current		0–1.2V			±100	μA	$V_O = 0.5V$ to V_{CC}, V_I = GND or V_{CC}
I_{OZL}	TRI-STATE Output Leakage Current		3.6			−5	μA	$V_O = 0.5V$
I_{OZH}	TRI-STATE Output Leakage Current		3.6			5	μA	$V_O = 3.0V$
I_{OZH}^+	TRI-STATE Output Leakage Current		3.6			10	μA	$V_{CC} < V_O \leq 5.5V$
I_{CCH}	Power Supply Current		3.6			0.09	mA	Outputs High
I_{CCL}	Power Supply Current		3.6			5	mA	Outputs Low
I_{CCZ}	Power Supply Current		3.6			0.09	mA	Outputs Disabled
I_{CCZ}^+	Power Supply Current		3.6			0.09	mA	$V_{CC} \leq V_O \leq 5.5V$, Outputs Disabled
ΔI_{CC}	Increase in Power Supply Current (Note 7)		3.6			0.2	mA	One Input at $V_{CC} - 0.6V$, Other Inputs at V_{CC} or GND

Note 3: All typical values are at $V_{CC} = 3.3V$, $T_A = 25°C$.

Note 4: An external driver must source at least the specified current to switch from LOW to HIGH.

Note 5: An external driver must sink at least the specified current to switch from HIGH to LOW.

Note 6: This parameter is valid for any V_{CC} between 0V and 1.2V at 25°C only.

Note 7: This is the increase in supply current for each input that is at the specified voltage level rather than V_{CC} or GND.

Dynamic Switching Characteristics (Note 8)

Symbol	Parameter	V_{CC} (V)	$T_A = 25°C$			Units	Conditions $C_L = 50$ pF, $R_L = 500\Omega$
			Min	Typ	Max		
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	3.3		0.8		V	(Note 9)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	3.3		−0.8		V	(Note 9)

Note 8: Characterized in SOIC package. Guaranteed parameter, but not tested.

Note 9: Max number of outputs defined as (n). n−1 data inputs are driven 0V to 3V. Output under test held LOW.

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40°C$ to $+85°C$, $C_L = 50$ pF, $R_L = 500\Omega$					Units
		$V_{CC} = 3.3V \pm 0.3V$			$V_{CC} = 2.7V$		
		Min	Typ (Note 3)	Max	Min	Max	
t_{PLH}	Propagation Delay Data to A Port Output	1.0		5.5	1.0	6.9	ns
t_{PHL}		1.0		4.7	1.0	5.6	
t_{PLH}	Propagation Delay Data to B Port Output	1.0		4.1	1.0	5.0	ns
t_{PHL}		1.0		4.1	1.0	5.2	
t_{PZH}	Output Enable Time for A Port Output	1.0		7.2	1.0	9.4	ns
t_{PZL}		1.0		6.6	1.0	8.2	
t_{PZH}	Output Enable Time for B Port Output	1.0		5.3	1.0	6.8	ns
t_{PZL}		1.0		5.2	1.0	6.7	
t_{PHZ}	Output Disable Time for A Port Output	1.8		7.3	1.8	8.0	ns
t_{PLZ}		1.8		6.7	1.8	7.1	
t_{PHZ}	Output Disable Time for B Port Output	1.8		6.4	1.8	7.2	ns
t_{PLZ}		1.8		5.8	1.8	6.1	
t_{OSHL}	A Port Output to Output Skew (Note 10)			1.0			ns
t_{OSLH}							
t_{OSHL}	B Port Output to Output Skew (Note 10)			1.0			ns
t_{OSLH}							

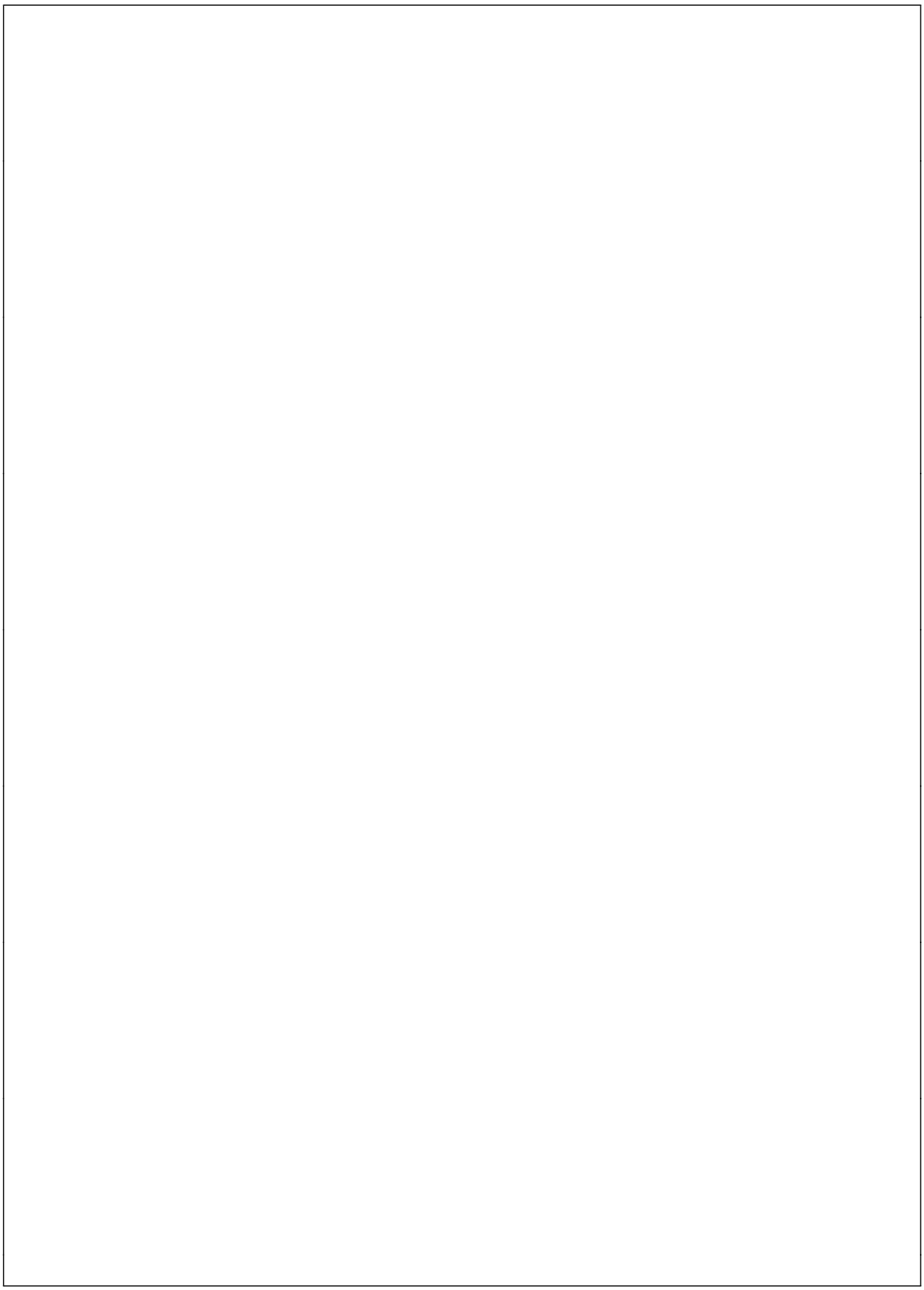
Note 3: All typical values are at $V_{CC} = 3.3V$, $T_A = 25°C$.

Note 10: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

Capacitance (Note 11)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
C_{IN}	Input Capacitance		4		pF	$V_{CC} = 0V$, $V_I = 0V$ or V_{CC}
C_{OUT}	Output Capacitance		10.5		pF	$V_{CC} = 3.0V$, $V_O = 0V$ or V_{CC}

Note 11: Capacitance is measured at frequency f = 1 MHz, per MIL-STD-883B, Method 3012.



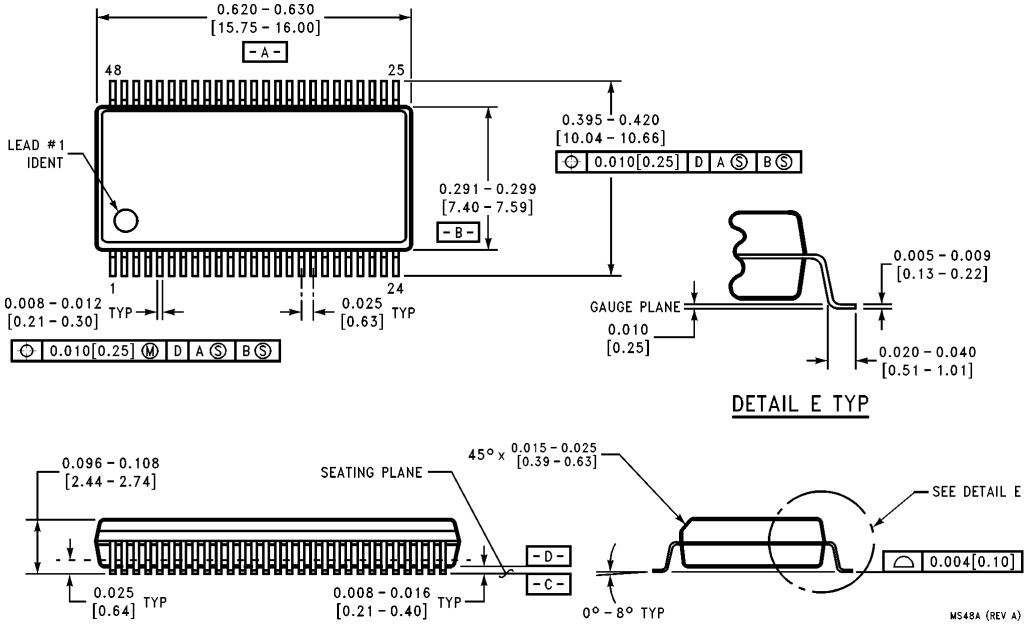
74LVT162245 Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:

74LVT 162245 MEA X

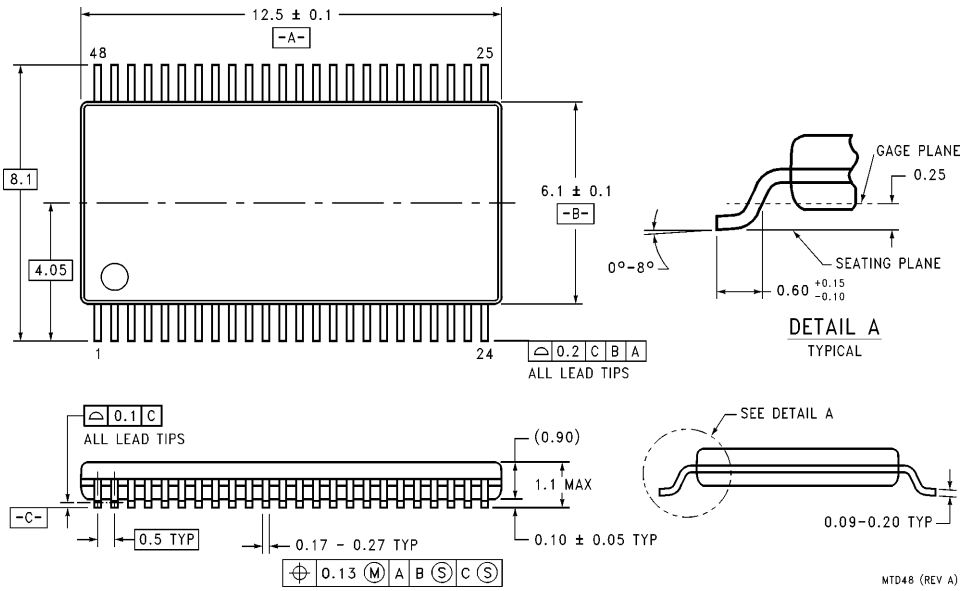
- Temperature Range Family
  - 74 = Commercial
- Device Type
- Package Code
  - MEA = Molded Shrink Small Outline Package, EIAJ
  - MTD = Molded Thin Shrink Small Outline Package, JEDEC, 4.4 mm Body Width
- Special Variations
  - "X" = Tape and Reel
  - " " = Rail/Tube

Physical Dimensions inches (millimeters) unless otherwise noted



48-Lead Molded Shrink Small Outline Package, EIAJ
Order Number 74LVT162245MEA or 74LVT162245MEAX
NS Package Number MS48A

Physical Dimensions millimeters (Continued)



48-Lead Molded Thin Shrink Small Outline Package, JEDEC, 6.1 mm Body Width
Order Number 74LVT162245MTD or 74LVT162245MTDX
NS Package Number MTD48

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