National Semiconductor

PRELIMINARY
November 1996

74LVT16240
3.3V ABT 16-Bit Inverting Buffer/Line Driver with TRI-STATE® Outputs

General Description

The LVT16240 contains sixteen inverting buffers with TRI-STATE outputs designed to be employed as a memory and address driver, clock driver, or bus-oriented transmitter/-receiver. The device is nibble controlled.

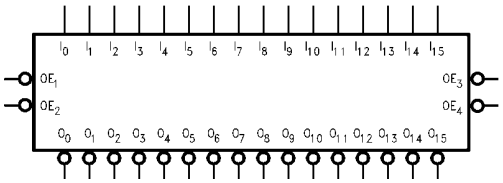
Individual TRI-STATE control inputs can be shorted together for 8-bit or 16-bit operation.

These buffers and line drivers are designed for low-voltage (3.3V) V_{CC} applications, but with the capability to provide a TTL interface to a 5V environment. The LVT16240 is fabricated with an advanced BiCMOS technology to achieve high speed operation similar to 5V ABT while maintaining a low power dissipation.

Features

- Input and output interface capability to systems at 5V V_{CC}
- Bus-Hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power Up/Down high impedance provides glitch-free bus loading
- Outputs source/sink −32 mA/+64 mA
- Available in SSOP and TSSOP
- Functionally compatible with the 74 series 16240
- Latch-up performance exceeds 500 mA

Logic Symbol



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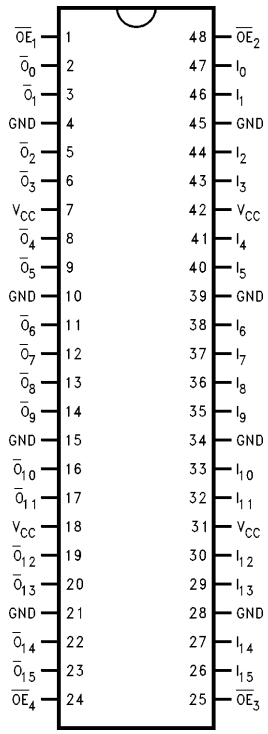
Pin Names	Description
$\overline{OE}_n$	Output Enable Inputs (Active Low)
I_0–I_{15}	Inputs
$\overline{O}_0$–$\overline{O}_{15}$	TRI-STATE Outputs

	SSOP	TSSOP
Order Number	74LVT16240MEA 74LVT16240MEAX	74LVT16240MTD 74LVT16240MTDX
See NS Package Number	MS48A	MTD48

Preliminary Data: National Semiconductor reserves the right to make changes at any time without notice.

Connection Diagram

Pin Assignment for SSOP and TSSOP



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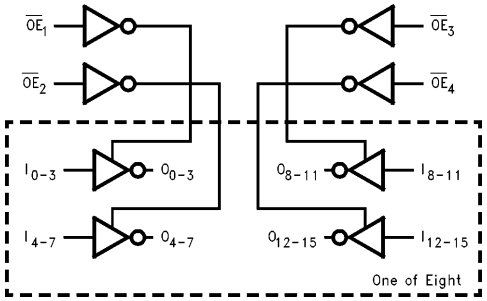
74LVT16240 3.3V ABT 16-Bit Inverting Buffer/Line Driver with TRI-STATE Outputs

Functional Description

The LVT16240 contains sixteen inverting buffers with TRI-STATE standard outputs. The device is nibble (4 bits) controlled with each nibble functioning identically, but independent of the other. The control pins may be shorted together to obtain full 16-bit operation. The TRI-STATE outputs are controlled by an Output Enable ($\overline{OE}_n$) input for each nibble. When $\overline{OE}_n$ is LOW, the outputs are in 2-state mode. When $\overline{OE}_n$ is HIGH, the outputs are in the high impedance mode, but this does not interfere with entering new data into the inputs.

Logic Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Truth Tables

Inputs		Outputs
$\overline{OE}_1$	I_0–I_3	$\overline{O}_0$–$\overline{O}_3$
L	L	H
L	H	L
H	X	Z

Inputs		Outputs
$\overline{OE}_2$	I_4–I_7	$\overline{O}_4$–$\overline{O}_7$
L	L	H
L	H	L
H	X	Z

Inputs		Outputs
$\overline{OE}_3$	I_8–I_{11}	$\overline{O}_8$–$\overline{O}_{11}$
L	L	H
L	H	L
H	X	Z

Inputs		Outputs
$\overline{OE}_4$	I_{12}–I_{15}	$\overline{O}_{12}$–$\overline{O}_{15}$
L	L	H
L	H	L
H	X	Z

H = High Voltage Level L = Low Voltage Level

X = Immaterial Z = High Impedance

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	−0.5 to +7.0		V
V_I	DC Input Voltage	−0.5 to +7.0		V
V_O	DC Output Voltage	−0.5 to +7.0	Output in TRI-STATE	V
		−0.5 to V_{CC} + 0.5	Output in High or Low State (Note 2)	V
I_{IK}	DC Input Diode Current	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50	V_O < GND	mA
I_O	DC Output Current	64	V_O > V_{CC} Output at High State	mA
		128	Output at Low State	
I_{CC}	DC Supply Current per Supply Pin	±64		mA
I_{GND}	DC Ground Current per Ground Pin	±128		mA
T_{STG}	Storage Temperature	−65 to +150		°C

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the ''Electrical Characteristics'' table are not guaranteed at the Absolute Maximum Ratings. The ''Recommended Operating Conditions'' table will define the conditions for actual device operation.

Note 2: I_O Absolute Maximum Rating must be observed.

Recommended Operating Conditions

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply Voltage	Operating	2.0	3.6	V
		Data Retention	1.5	3.6	
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage	HIGH or LOW State	0	V_{CC}	V
		TRI-STATE	0	5.5	
I_{OH}	High-Level Output Current			−32	mA
I_{OL}	Low-Level Output Current			64	
T_A	Free-Air Operating Temperature		−40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V		0	10	ns/V

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	T_A = −40°C to +85°C			Units	Conditions
			Min	Typ (Note 3)	Max		
V_{IK}	Input Clamp Diode Voltage	2.7			−1.2	V	I_I = −18 mA
V_{IH}	Input HIGH Voltage	2.7–3.6	2.0			V	$V_O \leq$ 0.1V or $V_O \geq V_{CC}$ − 0.1V
V_{IL}	Input LOW Voltage	2.7–3.6			0.8		
V_{OH}	Output HIGH Voltage	2.7–3.6	V_{CC} − 0.2			V	I_{OH} = −100 μA
		2.7	2.4			V	I_{OH} = −8 mA
		3.0	2.0			V	I_{OH} = −32 mA
V_{OL}	Output LOW Voltage	2.7			0.2	V	I_{OL} = 100 μA
		2.7			0.5	V	I_{OL} = 24 mA
		3.0			0.4	V	I_{OL} = 16 mA
		3.0			0.5	V	I_{OL} = 32 mA
		3.0			0.55	V	I_{OL} = 64 mA

DC Electrical Characteristics (Continued)

Symbol	Parameter		V_{CC} (V)	$T_A = -40°C$ to $+85°C$			Units	Conditions
				Min	Typ (Note 3)	Max		
$I_{I(HOLD)}$	Bus-Hold Input Minimum Drive		3.0	75			μA	$V_I = 0.8V$
				−75			μA	$V_I = 2.0V$
$I_{I(OD)}$	Bus-Hold Input Over-Drive Current to Change State		3.0	500			μA	(Note 4)
				−500			μA	(Note 5)
I_I	Input Current	Control Pins	0 or 3.6			10	μA	$V_I = 5.5V$
			3.6			±1	μA	$V_I = 0V$ or V_{CC}
		Data Pins	3.6			−5	μA	$V_I = 0V$
						1	μA	$V_I = V_{CC}$
I_{OFF}	Power Off Leakage Current		0			±100	μA	$0V \le V_I$ or $V_O \le 5.5V$
$I_{PU/PD}$ (Note 6)	Power Up/Down TRI-STATE Output Current		0–1.2V			±100	μA	$V_O = 0.5V$ to V_{CC} V_I = GND or V_{CC}
I_{OZL}	TRI-STATE Output Leakage Current		3.6			−5	μA	$V_O = 0.5V$
I_{OZH}	TRI-STATE Output Leakage Current		3.6			5	μA	$V_O = 3.0V$
$I_{OZH}{}^+$	TRI-STATE Output Leakage Current		3.6			10	μA	$V_{CC} < V_O \le 5.5V$
I_{CCH}	Power Supply Current		3.6			0.13	mA	V_I = GND or V_{CC}, Outputs High
I_{CCL}	Power Supply Current		3.6			5	mA	V_I = GND or V_{CC}, Outputs Low
I_{CCZ}	Power Supply Current		3.6			0.13	mA	V_I = GND or V_{CC}, Outputs Disabled
$I_{CCZH}{}^+$	Power Supply Current		3.6			0.13	mA	V_I = GND or V_{CC}, $V_{CC} \le V_O \le 5.5V$, Outputs Disabled
ΔI_{CC}	Increase in Power Supply Current (Note 7)		3.6			0.2	mA	One Input at $V_{CC} - 0.6V$ Other Inputs at V_{CC} or GND

Note 3: All typical values are at $V_{CC} = 3.3V$, $T_A = 25°C$.

Note 4: An external driver must source at least the specified current to switch from LOW to HIGH.

Note 5: An external driver must sink at least the specified current to switch from HIGH to LOW.

Note 6: This parameter is valid for any V_{CC} between 0V and 1.2V at 25°C only.

Note 7: This is the increase in supply current for each input that is at the specified voltage level rather than V_{CC} or GND.

Dynamic Switching Characteristics

Symbol	Parameter	V_{CC} (V)	$T_A = 25°C$			Units	Conditions $C_L = 50$ pF, $R_L = 500\Omega$
			Min	Typ	Max		
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	3.3		0.8		V	(Note 9)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	3.3		−0.8		V	(Note 9)

Note 8: Characterized in SOIC package. Guaranteed parameter, but not tested.

Note 9: Max number of outputs defined as (n). n−1 data inputs are driven 0V to 3V. Output at LOW.

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40°C$ to $+85°C$, $C_L = 50$ pF, $R_L = 500\Omega$					Units
		$V_{CC} = 3.3V \pm 0.3V$			$V_{CC} = 2.7V$		
		Min	Typ (Note 3)	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation Delay Data to Output	1.0 1.0		4.1 4.1	1.0 1.0	5.0 5.2	ns
t_{PZH} t_{PZL}	Output Enable Time	1.0 1.0		5.2 5.2	1.0 1.0	6.3 6.7	ns
t_{PHZ} t_{PLZ}	Output Disable Time	1.8 1.8		5.7 5.1	1.8 1.8	6.3 5.6	ns
t_{OSHL} t_{OSLH}	Output to Output Skew (Note 10)			1.0			ns

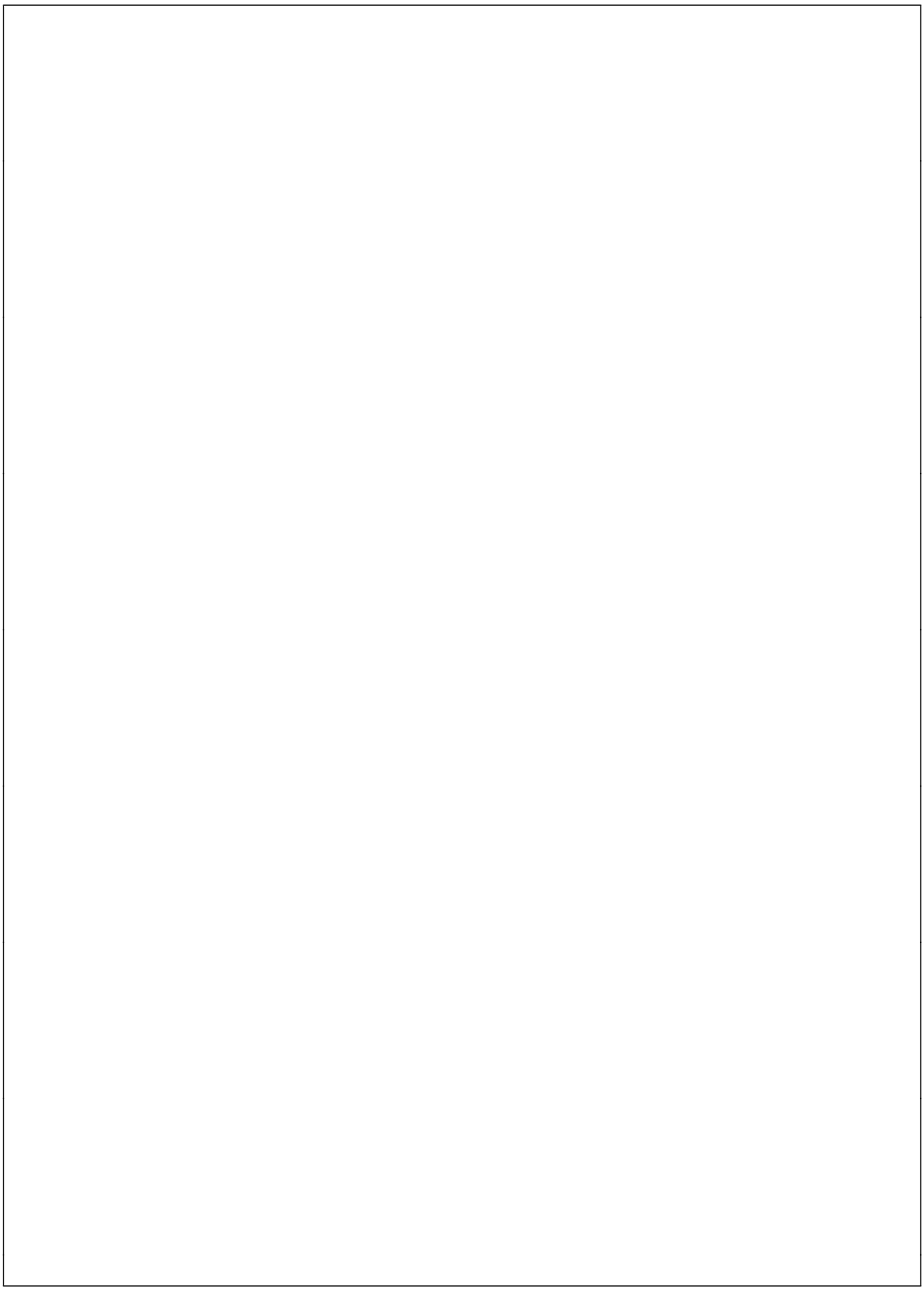
Note 3: All typical values are at $V_{CC} = 3.3V$, $T_A = 25°C$.

Note 10: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

Capacitance (Note 11)

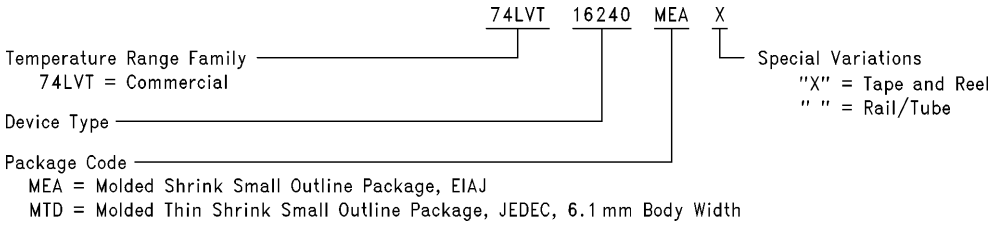
Symbol	Parameter	Min	Typ	Max	Units	Conditions
C_{IN}	Input Capacitance		4		pF	$V_{CC} = 0V$, $V_I = 0V$ or V_{CC}
C_{OUT}	Output Capacitance		10		pF	$V_{CC} = 3.0V$, $V_O = 0V$ or V_{CC}

Note 11: Capacitance is measured at frequency f = 1 MHz, per MIL-STD-883B, Method 3012.



74LVT16240 Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



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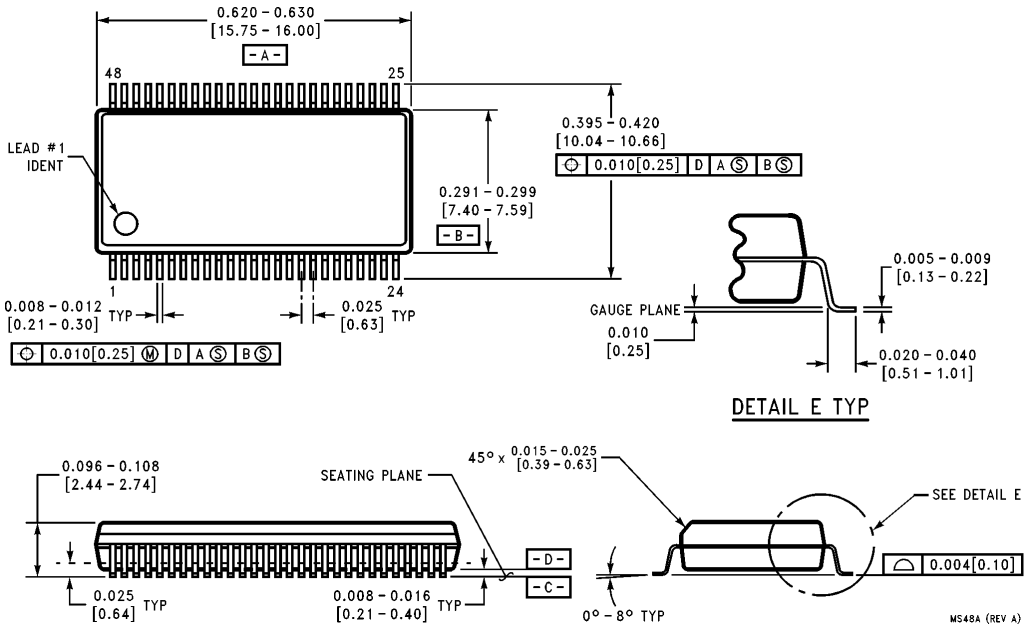
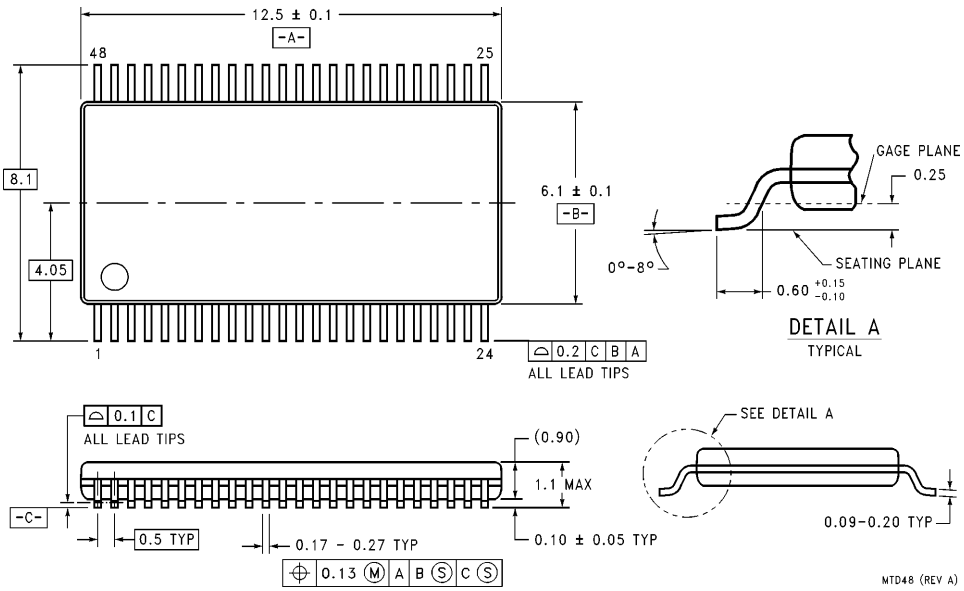
Physical Dimensions inches (millimeters) unless otherwise noted



48-Lead (0.300″ Wide) Molded Shrink Small Outline Package
Order Number 74LVT16240MEA or 74LVT16240MEAX
NS Package Number MS48A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



48-Lead Molded Thin Shrink Small Outline Package, JEDEC, 6.1 mm Body Width
Order Number 74LVT16240MTD or 74LVT16240MTDX
NS Package Number MTD48

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