

## 74LVX3245 8-Bit Dual Supply Translating Transceiver with TRI-STATE® Outputs

### General Description

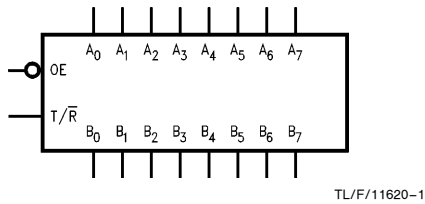
The LVX3245 is a dual-supply, 8-bit translating transceiver that is designed to interface between a 3V bus and a 5V bus in a mixed 3V/5V supply environment. The Transmit/Receive (T/ $\bar{R}$ ) input determines the direction of data flow. Transmit (active-HIGH) enables data from A ports to B ports; Receive (active-LOW) enables data from B ports to A ports. The Output Enable input, when HIGH, disables both A and B ports by placing them in a HIGH Z condition. The A port interfaces with the 3V bus; the B port interfaces with the 5V bus.

The LVX3245 is suitable for mixed voltage applications such as notebook computers using 3.3V CPU and 5V peripheral components.

### Features

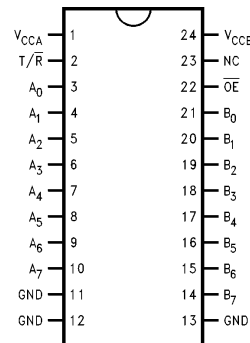
- Bidirectional interface between 3V and 5V buses
- Inputs compatible with TTL level
- 3V data flow at A port and 5V data flow at B port
- Outputs source/sink 24 mA
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Available in SOIC, QSOP and TSSOP packages
- Implements proprietary EMI reduction circuitry
- Functionally compatible with the 74 series 245

### Logic Symbol



### Connection Diagram

Pin Assignment  
for SOIC, QSOP and TSSOP



Pin Names	Description
$\overline{OE}$	Output Enable Input
T/ $\bar{R}$	Transmit/Receive Input
A <sub>0</sub> -A <sub>7</sub>	Side A Inputs or TRI-STATE Outputs
B <sub>0</sub> -B <sub>7</sub>	Side B Inputs or TRI-STATE Outputs

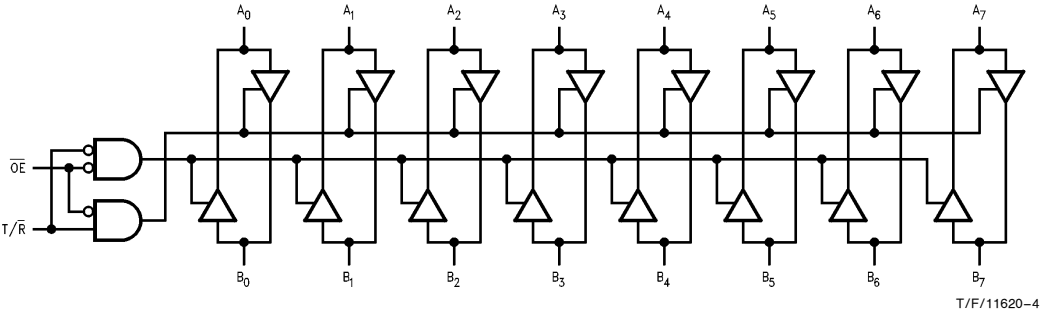
	SOIC JEDEC	QSOP	TSSOP
Order Number	74LVX3245WM 74LVX3245WMX	74LVX3245QSC 74LVX3245QSCX	74LVX3245MTC 74LVX3245MTCX
See NS Package Number	M24B	MQA24	MTC24

TRI-STATE® is a registered trademark of National Semiconductor Corporation.

**Truth Table**

Inputs		Outputs
$\overline{OE}$	$T/\overline{R}$	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	HIGH-Z State

**Logic Diagram**



## Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ( $V_{CCA}, V_{CCB}$ )	-0.5V to +7.0V
DC Input Voltage ( $V_I$ ) @ $\overline{OE}, T/\overline{R}$	-0.5V to $V_{CCB} + 0.5V$
DC Input/Output Voltage ( $V_{I/O}$ )	
@ A(n)	-0.5V to $V_{CCA} + 0.5V$
@ B(n)	-0.5V to $V_{CCB} + 0.5V$
DC Input Diode Current ( $I_{IN}$ ) @ $\overline{OE}, T/\overline{R}$	$\pm 20$ mA
DC Output Diode Current ( $I_{OK}$ )	$\pm 50$ mA
DC Output Source or Sink Current ( $I_O$ )	$\pm 50$ mA
DC $V_{CC}$ or Ground Current per Output Pin ( $I_{CC}$ or $I_{GND}$ ) and Max Current @ $I_{CCA}$	$\pm 50$ mA
@ $I_{CCB}$	$\pm 100$ mA
@ $I_{CCB}$	$\pm 200$ mA
Storage Temperature Range ( $T_{STG}$ )	-65°C to +150°C
DC Latch-Up Source or Sink Current	$\pm 300$ mA

## Recommended Operating Conditions

Supply Voltage		2.7V to 3.6V
$V_{CCA}$		4.5V to 5.5V
$V_{CCB}$		
Input Voltage ( $V_I$ ) @ $\overline{OE}, T/\overline{R}$		0V to $V_{CCB}$
Input/Output Voltage ( $V_{I/O}$ )		
@ A(n)		0V to $V_{CCA}$
@ B(n)		0V to $V_{CCB}$
Free Air Operating Temperature ( $T_A$ )		
74LVX		-40°C to +85°C
Minimum Input Edge Rate ( $\Delta t/\Delta V$ )		8 ns/V
$V_{IN}$ from 30% to 70% of $V_{CC}$		
$V_{CC}$ @ 3.0V, 4.5V, 5.5V		

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

## DC Electrical Characteristics

Symbol	Parameter		$V_{CCA}$ (V)	$V_{CCB}$ (V)	74LVX3245		74LVX3245		Units	Conditions
					$T_A = +25^\circ\text{C}$		$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$			
					Typ	Guaranteed Limits	Typ	Guaranteed Limits		
$V_{IHA}$	Minimum High Level Input Voltage	A(n), $T/\overline{R}$ , $\overline{OE}$	3.6	5.0		2.0	2.0	V	$V_{OUT} \leq 0.1V$ or $\geq V_{CC} - 0.1V$	
		B(n)	3.3	4.5		2.0	2.0			
$V_{IHB}$	Input Voltage	B(n)	3.3	5.5		2.0	2.0	V	$V_{OUT} \leq 0.1V$ or $\geq V_{CC} - 0.1V$	
			3.3	5.5		2.0	2.0			
$V_{ILA}$	Maximum Low Level Input Voltage	A(n), $T/\overline{R}$ , $\overline{OE}$	3.6	5.0		0.8	0.8	V	$V_{OUT} \leq 0.1V$ or $\geq V_{CC} - 0.1V$	
		B(n)	3.3	4.5		0.8	0.8			
$V_{ILB}$	Input Voltage	B(n)	3.3	5.5		0.8	0.8	V	$V_{OUT} \leq 0.1V$ or $\geq V_{CC} - 0.1V$	
			3.3	5.5		0.8	0.8			
$V_{OHA}$	Minimum High Level Output Voltage		3.0	4.5	2.99	2.9	2.9	V	$I_{OUT} = -100 \mu\text{A}$ $I_{OH} = -24 \text{ mA}$ $I_{OH} = -12 \text{ mA}$ $I_{OH} = -24 \text{ mA}$	
			3.0	4.5	2.65	2.35	2.25			
			2.7	4.5	2.5	2.3	2.2			
			2.7	4.5	2.3	2.1	2.0			
$V_{OHB}$	Output Voltage		3.0	4.5	4.5	4.4	4.4	V	$I_{OUT} = -100 \mu\text{A}$ $I_{OH} = -24 \text{ mA}$	
			3.0	4.5	4.25	3.86	3.76			
$V_{OLA}$	Maximum Low Level Output Voltage		3.0	4.5	0.002	0.1	0.1	V	$I_{OUT} = 100 \mu\text{A}$ $I_{OL} = 24 \text{ mA}$ $I_{OL} = 12 \text{ mA}$ $I_{OL} = 24 \text{ mA}$	
			3.0	4.5	0.21	0.36	0.44			
			2.7	4.5	0.11	0.36	0.44			
			2.7	4.5	0.22	0.42	0.5			
$V_{OLB}$	Output Voltage		3.0	4.5	0.002	0.1	0.1	V	$I_{OUT} = 100 \mu\text{A}$ $I_{OL} = 24 \text{ mA}$	
			3.0	4.5	0.18	0.36	0.44			
$I_{IN}$	Maximum Input Leakage Current @ $\overline{OE}, T/\overline{R}$		3.6	5.5		$\pm 0.1$	$\pm 1.0$	$\mu\text{A}$	$V_I = V_{CCB}, \text{GND}$	
$I_{OZA}$	Maximum TRI-STATE Output Leakage @ A(n)		3.6	5.5		$\pm 0.5$	$\pm 5.0$	$\mu\text{A}$	$V_I = V_{IL}, V_{IH}$ $\overline{OE} = V_{CCA}$ $V_O = V_{CCA}, \text{GND}$	

## DC Electrical Characteristics (Continued)

Symbol	Parameter	V <sub>CCA</sub> (V)	V <sub>CCB</sub> (V)	74LVX3245		74LVX3245		Units	Conditions
				T <sub>A</sub> = +25°C		T <sub>A</sub> = -40°C to +85°C			
				Typ	Guaranteed Limits				
I <sub>oZB</sub>	Maximum TRI-STATE Output Leakage @ B(n)	3.6	5.5		±0.5	±5.0	μA	V <sub>I</sub> = V <sub>IL</sub> , V <sub>IH</sub> OE = V <sub>CCA</sub> V <sub>O</sub> = V <sub>CCB</sub> , GND	
ΔI <sub>CC</sub>	Maximum I <sub>CC</sub> T/Input @	B(n)	3.6	5.5	1.0	1.35	1.5	mA	V <sub>I</sub> = V <sub>CCB</sub> - 2.1V
		A(n), T/ $\bar{R}$ , OE	3.6	5.5		0.35	0.5	mA	V <sub>I</sub> = V <sub>CCA</sub> - 0.6V
I <sub>CCA</sub>	Quiescent V <sub>CCA</sub> Supply Current	3.6	5.5		5	50	μA	A(n) = V <sub>CCA</sub> or GND B(n) = V <sub>CCB</sub> or GND, OE = GND, T/ $\bar{R}$ = GND	
I <sub>CCB</sub>	Quiescent V <sub>CCB</sub> Supply Current	3.6	5.5		8	80	μA	A(n) = V <sub>CCA</sub> or GND B(n) = V <sub>CCB</sub> or GND, OE = GND, T/ $\bar{R}$ = V <sub>CCA</sub>	
V <sub>OLPA</sub> V <sub>OLPB</sub>	Quiet Output Maximum Dynamic V <sub>OL</sub>	3.3	5.0		0.8		V	(Notes 1, 2)	
		3.3	5.0		1.5				
V <sub>OLVA</sub> V <sub>OLVB</sub>	Quiet Output Minimum Dynamic V <sub>OL</sub>	3.3	5.0		-0.8		V	(Notes 1, 2)	
		3.3	5.0		-1.2				
V <sub>IHDA</sub> V <sub>IHDB</sub>	Minimum High Level Dynamic Input Voltage	3.3	5.0		2.0	2.0	V	(Notes 1, 3)	
V <sub>ILDA</sub> V <sub>ILDB</sub>	Maximum Low Level Dynamic Input Voltage	3.3	5.0		0.8	0.8	V	(Notes 1, 3)	

†Maximum test duration 2.0 ms, one output loaded at a time.

**Note 1:** Worst case package.

**Note 2:** Max number of outputs defined as (n). Data inputs are driven 0V to V<sub>CC</sub> level; one output at GND.

**Note 3:** Max number of Data Inputs (n) switching. (n - 1) inputs switching 0V to V<sub>CC</sub> level. Input-under-test switching: V<sub>CC</sub> level to threshold (V<sub>IHD</sub>), 0V to threshold (V<sub>ILD</sub>), f = 1 MHz.

## AC Electrical Characteristics

Symbol	Parameters	74LVX3245			74LVX3245		74LVX3245		Units
		$T_A = +25^\circ\text{C}$ $C_L = 50\text{ pF}$ $**V_{CCA} = 3.3\text{V}$ $*V_{CCB} = 5.0\text{V}$			$T_A = -40^\circ\text{C to } +85^\circ\text{C}$ $C_L = 50\text{ pF}$ $**V_{CCA} = 3.3\text{V}$ $*V_{CCB} = 5.0\text{V}$		$T_A = -40^\circ\text{C to } +85^\circ\text{C}$ $C_L = 50\text{ pF}$ $V_{CCA} = 2.7\text{V}$ $*V_{CCB} = 5.0\text{V}$		
		Min	Typ	Max	Min	Max	Min	Max	
$t_{PHL}$ $t_{PLH}$	Propagation Delay A to B	1.0	5.4	8.0	1.0	8.5	1.0	9.0	ns
$t_{PHL}$ $t_{PLH}$	Propagation Delay B to A	1.0	5.1	7.5	1.0	8.0	1.0	8.5	
$t_{PZL}$ $t_{PZH}$	Output Enable Time $\overline{OE}$ to B	1.0	4.8	8.0	1.0	8.5	1.0	9.0	ns
$t_{PZL}$ $t_{PZH}$	Output Enable Time $\overline{OE}$ to A	1.0	6.3	8.5	1.0	9.0	1.0	9.5	
$t_{PHZ}$ $t_{PLZ}$	Output Disable Time $\overline{OE}$ to B	1.0	5.3	7.5	1.0	8.0	1.0	8.5	ns
$t_{PHZ}$ $t_{PLZ}$	Output Disable Time $\overline{OE}$ to A	1.0	4.2	7.0	1.0	7.5	1.0	8.0	
$t_{OSHL}$ $t_{OSLH}$	Output to Output Skew*** Data to Output		1.0	1.5		1.5		1.5	ns

\*Voltage Range 5.0V is 5.0V  $\pm 0.5\text{V}$ .

\*\*Voltage Range 3.3V is 3.3V  $\pm 0.3\text{V}$ .

\*\*\*Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW ( $t_{OSHL}$ ) or LOW to HIGH ( $t_{OSLH}$ ). Parameter guaranteed by design.

## Capacitance

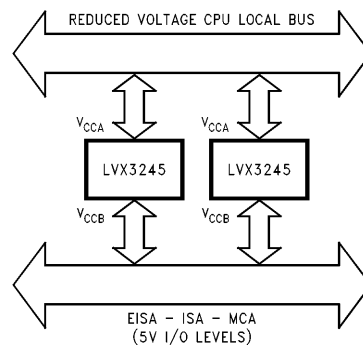
Symbol	Parameter	Typ	Units	Conditions	
$C_{IN}$	Input Capacitance	4.5	pF	$V_{CC} = \text{Open}$	
$C_{I/O}$	Input/Output Capacitance	15	pF	$V_{CCA} = 3.3\text{V}$ $V_{CCB} = 5.0\text{V}$	
$C_{PD}$	Power Dissipation Capacitance	A $\rightarrow$ B	55	pF	$V_{CCB} = 5.0\text{V}$ $V_{CCA} = 3.3\text{V}$
		B $\rightarrow$ A	40		

$C_{PD}$  is measured at 10 MHz

## 8-Bit Dual Supply Translating Transceiver

The LVX3245 is a dual supply device capable of bidirectional signal translation. This level shifting ability provides an efficient interface between low voltage CPU local bus with memory and a standard bus defined by 5V I/O levels. The device control inputs can be controlled by either the low voltage CPU and core logic or a bus arbitrator with 5V I/O levels.

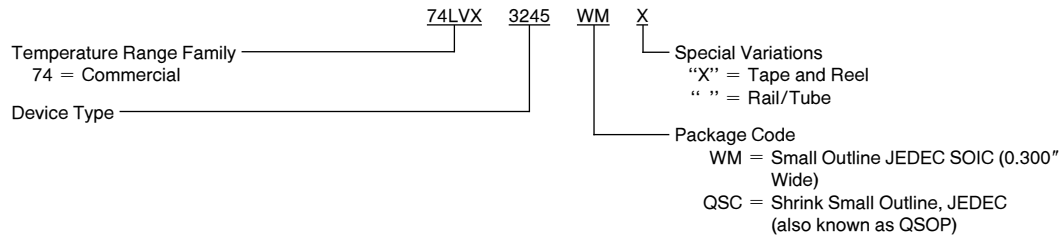
Manufactured on a sub-micron CMOS process, the LVX3245 is ideal for mixed voltage applications such as notebook computers using 3.3V CPU's and 5V peripheral devices.



TL/F/11620-3

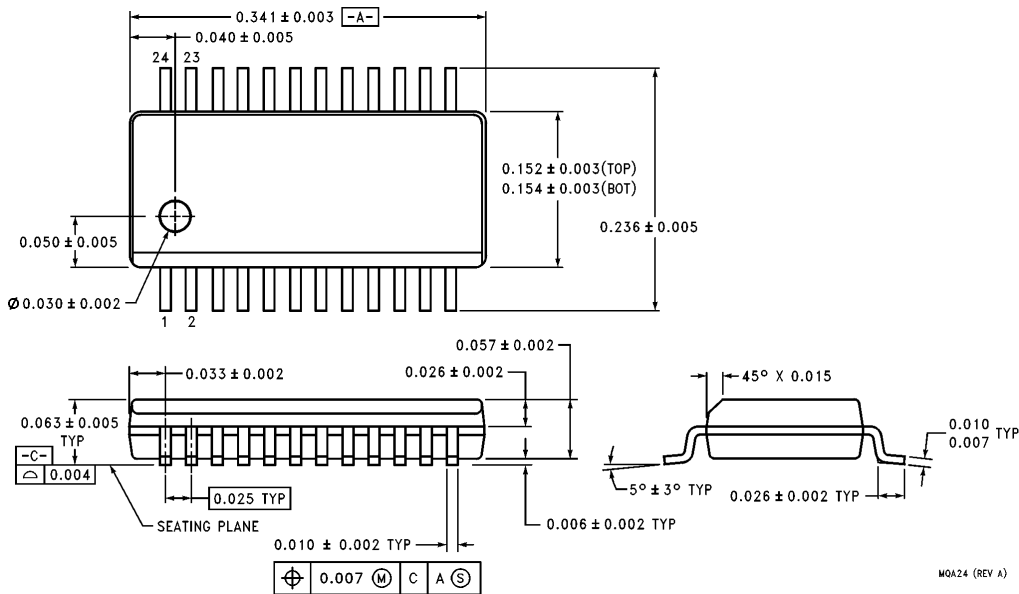
## 74LVX3245 Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:





**Physical Dimensions** inches (Continued)



MQA24 (REV A)

**24-Lead (0.150" Wide) Molded Shrink Small Outline Package, JEDEC**  
(also known as: QSOP)

**Order Number 74LVX3245QSC or 74LVX3245QSCX**  
**NS Package Number MQA24**

**LIFE SUPPORT POLICY**

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.



**National Semiconductor Corporation**  
**Americas**  
Tel: 1(800) 272-9959  
Fax: 1(800) 737-7018  
Email: support@nsc.com

**National Semiconductor Europe**  
Fax: +49 (0) 180-530 85 86  
Email: europe.support@nsc.com  
Deutsch Tel: +49 (0) 180-530 85 85  
English Tel: +49 (0) 180-532 78 32  
Français Tel: +49 (0) 180-532 93 58  
Italiano Tel: +49 (0) 180-534 16 80

**National Semiconductor Southeast Asia**  
Fax: (852) 2376 3901  
Email: sea.support@nsc.com

**National Semiconductor Japan Ltd.**  
Tel: 81-3-5620-7561  
Fax: 81-3-5620-6179

<http://www.national.com>

National does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and National reserves the right at any time without notice to change said circuitry and specifications.