National Semiconductor

MICROCIRCUIT DATA SHEET

MJLF147-X REV 1B1

Original Creation Date: 02/09/95
Last Update Date: 08/24/98
Last Major Revision Date: 11/09/95

WIDE BANDWIDTH QUAD JFET INPUT OPERATIONAL AMPLIFIER

General Description

The LF147 is a low cost, high speed quad JFET input operational amplifier with an internally trimmed input offset voltage (BI-FET II[TM] technology). The device requires a low supply current and yet maintains a large gain bandwidth product and a fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The LF147 is pin compatible with the standard LM148. This feature allows designers to immediately upgrade the overall performance of existing LF148 and LM124 designs.

The LF147 may be used in applications such as high speed integrators, fast D/A converters, sample-and-hold circuits and many other circuits requiring low input bias current, high input impedance, high slew rate and wide bandwidth. The device has low noise and offset voltage drift.

Industry Part Number

LF147

NS Part Numbers

JL147BCA

Prime Die

LF147

Controlling Document

38510/11906

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-833 , Method 5005

Subgrp	Description	Temp (^{O}C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55
12	Settling time at	+25

Features

- Internally trimmed offset voltage	5mV Max
- Low input bias current	50pA Typ
- Low input noise current	0.01 pA/Root Hz Typ
- Wide gain bandwidth	4MHz Typ
- High slew rate	13V/uS Typ
- Low supply current	7.2mA Typ
- High input impedance	10E12 Ohms Typ
- Low total harmonic distortion Av = 10, RL = 10K, Vo = 20Vp-p, BW = 20HZ - 20KHz	<0.02% Typ
- Low 1/f noise corner	50Hz Typ
- Fast settling time to 0.01%	2uS Typ

(Absolute Maximum Ratings)

Supply Voltage	±18V
Differential Input Voltage	±30V
Input Voltage Range (Note 1)	±15V
Output Short Circuit Duration (Note 2)	Continuous
Power Dissipation (Note 3, 4)	900mW
Tj Max	175 C
ThetaJA CERAMIC DIP	70 C/W
Operating Temperature Range	-55 C ≤ TA ≤ 125 C

Note 1: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.
Note 2: Any of the amplifier outputs can be shorted to ground indefinetly, however, more than one should not be simultaneously shorted as the maximum junction temperature will be exceeded.
Note 3: For operating at elevated temperature, these devices must be derated based on a thermal resistance of ThetaJa.
Note 4: Maximum Power Dissipation is defined by the package characteristics. Operating the part near the Max. Power Dissipation may cuase the part to operate outside guaranteed limits.

Recommended Operating Conditions

Supply Voltage Range	±5V to ±15V
Storage Temperature Range	-65 C ≤ TA ≤ 150 C
Lead Temperature Soldering, (10 seconds)	260 C
Soldering Information Dual-In-Line Package (Soldering, 10 seconds)	260 C
ESD Tolerance (Note 1)	900V

Note 1: Human body model, 1.5K Ohms in series with 100pF.

Electrical Characteristics

DC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: ±Vcc = ±15V, Vcm = 0V

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Vio	Input Offset Voltage	+Vcc = 26V, -Vcc = -4V, Vcm = -11V			-5	5	mV	1
					-7	7	mV	2, 3
		+Vcc = 4V, -Vcc = -26V, Vcm = 11V			-5	5	mV	1
					-7	7	mV	2, 3
		+Vcc = 15V, -Vcc = -15V, Vcm = 0V			-5	5	mV	1
					-7	7	mV	2, 3
		+Vcc = 5V, -Vcc = -5V, Vcm = 0V			-5	5	mV	1
					-7	7	mV	2, 3
+Iib	Input Bias Current	+Vcc = 26V, -Vcc = -4V, Vcm = -11V			-0.4	0.2	nA	1
					-10	50	nA	2
		+Vcc = 15V, -Vcc = -15V, Vcm = 0V			-0.2	0.2	nA	1
					-10	50	nA	2
		+Vcc = 4V, -Vcc = -26V, Vcm = 11V			-0.2	1.2	nA	1
					-10	70	nA	2, 3
-Iib	Input Bias Current	+Vcc = 26V, -Vcc = -4V, Vcm = -11V			-0.4	0.2	nA	1
					-10	50	nA	2
		+Vcc = 15V, -Vcc = -15V, Vcm = 0V			-0.2	0.2	nA	1
					-10	50	nA	2
		+Vcc = 4V, -Vcc = -26V, Vcm = 11V			-0.2	1.2	nA	1
					-10	70	nA	2
Iio	Input Offset Current	+Vcc = 15V, -Vcc = -15V, Vcm = 0V			-0.1	0.1	nA	1
					-20	20	nA	2
+PSRR	Power Supply Rejection Ratio	-Vcc = -15V, +Vcc = 20V to 10V			80		dB	1, 2, 3
-PSRR	Power Supply Rejection Ratio	+Vcc = 15V, -Vcc = -20V to -10V			80		dB	1, 2, 3
CMR	Input Voltage Common Mode Rejection	±Vcc = ±4V to ±26V, Vcm = -11V to +11V			80		dB	1, 2, 3
Ios+	Output Short Circuit Current	+Vcc = 15V, -Vcc = -15V, Vcm = -10V, t ≤25mS			-80		mA	1, 2, 3
Ios-	Output Short Circuit Current	+Vcc = 15V, -Vcc = -15V, Vcm = 10V, t ≤25mS				80	mA	1, 2, 3

Electrical Characteristics

DC PARAMETERS(Continued)

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: ±Vcc = ±15V, Vcm = 0V

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Icc	Supply Current	+Vcc = 15V, -Vcc = -15V				14	mA	1, 2
						16	mA	3
DELTA Vio/ DELTA T	Input Offset Voltage Temp. Sensitivity	25 C ≤ TA ≤ +125 C	1		-30	30	uV/ C	2
		-55 C ≤ TA ≤ 25 C	1		-30	30	uV/ C	3
+Vop	Output Voltage Swing	+Vcc = 15V, -Vcc = -15V, RL=10K Ohms, Vcm = -15V			12		V	4, 5, 6
		+Vcc = 15V, -Vcc = -15V, RL=2K Ohms, Vcm = -15V			10		V	4, 5, 6
-Vop	Output Voltage Swing	+Vcc = 15V, -Vcc = -15V, RL=10K Ohms, Vcm = 15V				-12	V	4, 5, 6
		+Vcc = 15V, -Vcc = -15V, RL = 2K Ohms, Vcm = 15V				-10	V	4, 5, 6
AVS+	Open Loop Voltage Gain	+Vcc = 15V, -Vcc = -15V, RL = 2K Ohms, Vout = 0 to 10V			50		V/mV	4
					25		V/mV	5, 6
AVS-	Open Loop Voltage Gain	+Vcc = 15V, -Vcc = -15V, RL = 2K Ohms, Vout = 0 to -10V			50		V/mV	4
					25		V/mV	5, 6
AVS	Open Loop Voltage Gain	+Vcc = 5V, -Vcc = -5V, RL = 10K Ohms, Vout = ±2V			20		V/mV	4, 5, 6

Electrical Characteristics

AC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: ±Vcc = ±15V

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Sr+	Slew Rate	Vin = -5V to +5V			7		V/uS	7
					5		V/uS	8A, 8B
Sr-	Slew Rate	Vin = +5V to -5V			7		V/uS	7
					5		V/uS	8A, 8B
tR(tr)	Transient Response Rise Time	AV=1, Vin=50mV, CL=100pF, RL=2K Ohms				200	nS	7, 8A, 8B
tR(os)	Transient Response Overshoot	AV=1, Vin=50mV, CL=100pF, RL=2K Ohms				40	%	7, 8A, 8B
NI(BB)	Noise Broadband	BW = 10Hz to 15KHz, Rs = 0 Ohms				15	uVrms	7
NI(PC)	Noise Popcorn	BW = 10Hz to 15KHz, Rs = 100K Ohms	2			80	uVpk	7
CS	Channel Separation	RL = 2K Ohms			80		dB	7
		RL = 2K Ohms, Vin = ±10V, A to B			80		dB	7
		RL = 2K Ohms, Vin = ±10V, A to C			80		dB	7
		RL = 2K Ohms, Vin = ±10V, A to D			80		dB	7
		RL = 2K Ohms, Vin = ±10V, B to A			80		dB	7
		RL = 2K Ohms, Vin = ±10V, B to C			80		dB	7
		RL = 2K Ohms, Vin = ±10V, B to D			80		dB	7
		RL = 2K Ohms, Vin = ±10V, C to A			80		dB	7
		RL = 2K Ohms, Vin = ±10V, C to B			80		dB	7
		RL = 2K Ohms, Vin = ±10V, C to D			80		dB	7
		RL = 2K Ohms, Vin = ±10V, D to A			80		dB	7
		RL = 2K Ohms, Vin = ±10V, D to B			80		dB	7
		RL = 2K Ohms, Vin = ±10V, D to C			80		dB	7
tS(±)	Settling Time	AV = 1				1500	nS	12

Electrical Characteristics

DC PARAMETERS: DRIFT VALUES

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: ±Vcc = ±15V, Vcm = 0V. "Delta calculations performed on JAN S and QMLV devices at group B, subgroup 5 only".

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Vio	Input Offset Voltage	+Vcc = 15V, -Vcc = -15V, Vcm = 0V			-1	1	mV	1
+Iib	Input Bias Current	+Vcc = 15V, -Vcc = -15V, Vcm = 0V			-0.1	0.1	nA	1
-Iib	Input Bias Current	+Vcc = 15V, -Vcc = -15V, Vcm = 0V			-0.1	0.1	nA	1

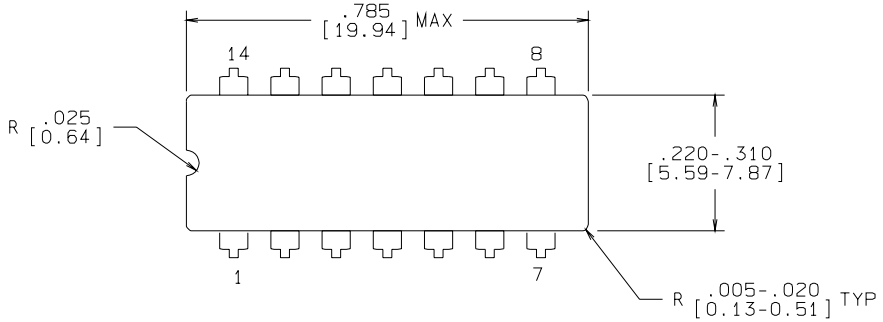
Note 1: Calculated parameters.
Note 2: Test on either A360, J273 or bench test.

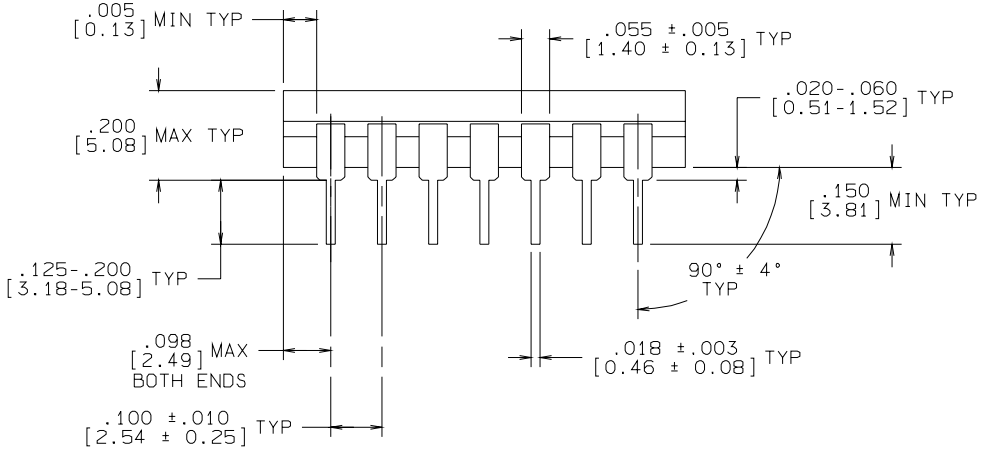
Graphics and Diagrams

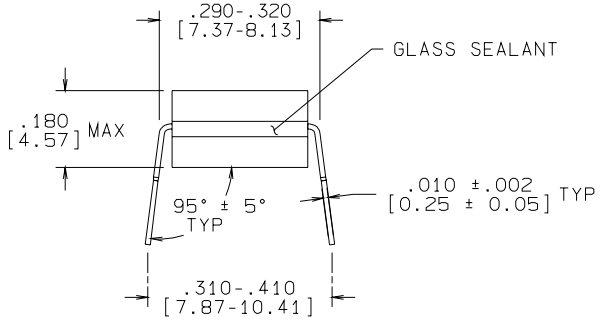
GRAPHICS#	DESCRIPTION
05817HRA3	CERDIP (J), 14 LEAD (B/I CKT)
J14ARH	CERDIP (J), 14 LEAD (P/P DWG)
P000193A	CERDIP (J), 14 LEAD (PINOUT)

See attached graphics following this page.

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
H	REVISE PER CURRENT STD; REDRAW	10001	09/15/93	TL/







CONTROLLING DIMENSION: INCH

MIL/AERO CONFIGURATION CONTROL

MIL-M-38510 CONFIGURATION CONTROL

NOTES: UNLESS OTHERWISE SPECIFIED

1. LEAD FINISH TO BE 200 MICROINCHES / 5.08 MICROMETERS MINIMUM SOLDER MEASURED AT THE CREST OF THE MAJOR FLATS.
2. JEDEC REGISTRATION MO-036, VARIATION AB, DATED 04/1981.

APPROVALS	DATE
DRAWN T. LEQUANG	09/15/93
DFTG. CHK.	
ENGR. CHK.	
APPROVAL	

PROJECTION

INCH
[MM]

NATIONAL SEMICONDUCTOR CORPORATION
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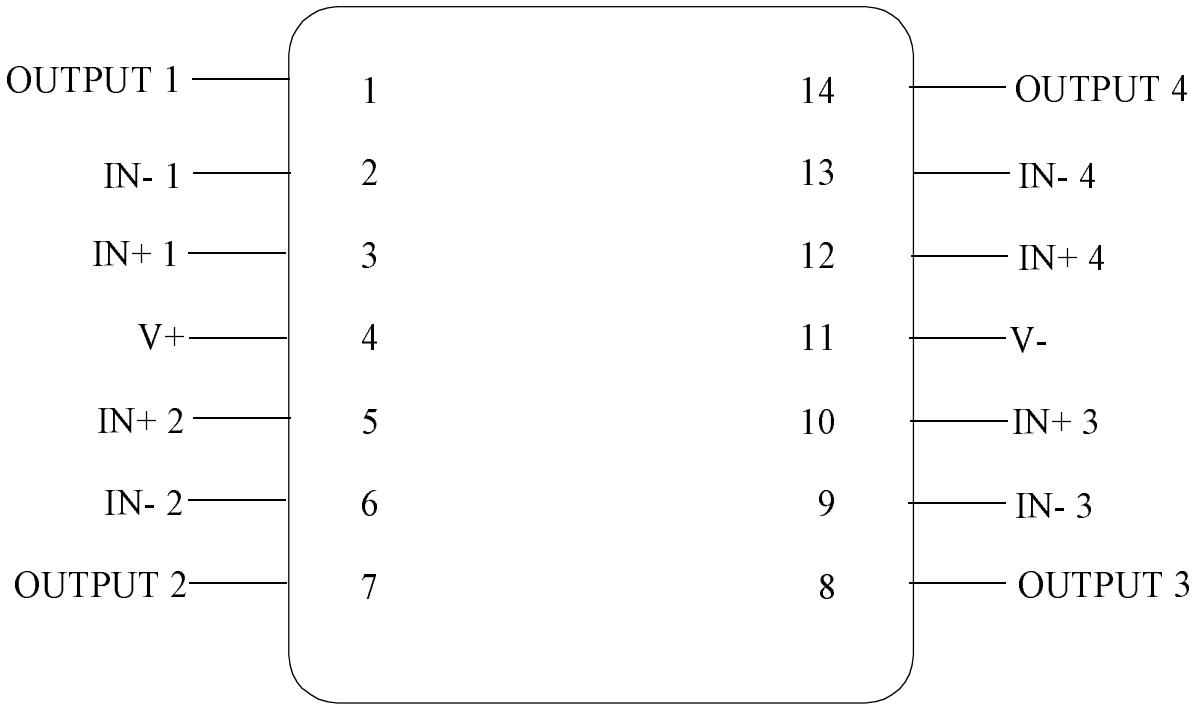
CERDIP (J), 14 LEAD,

SCALE	SIZE	DRAWING NUMBER	REV
N/A	B	MKT-J14A	H

DO NOT SCALE DRAWING | SHEET 1 OF 1



LF147J
14 - LEAD DIP
CONNECTION DIAGRAM
TOP VIEW
P000193A

National Semiconductor™
MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050

Revision History

Rev	ECN #	Rel Date	Originator	Changes
1B1	M0003006	08/24/98	Rose Malone	Update MDS: MJLF147-X Rev. 1B0 to MJLF147-X Rev. 1B1. Updated Burn-in graphic and added pinout.