National Semiconductor

MICROCIRCUIT DATA SHEET

MNADC1175-X REV 1A0

Original Creation Date: 03/12/04
Last Update Date: 05/13/04
Last Major Revision Date: 04/14/04

ADC1175 8-BIT, 20MHz, 60mW A/D CONVERTER

General Description

The ADC1175 is a low power, 20 Msps analog-to-digital converter that digitizes signals to 8 bit while consuming just 60mW of power (typ). The ADC1175 uses a unique architecture that achieves 7.5 Effective Bits. Output formatting is straight binary coding.

The excellent DC and AC characteristics of this device, together with its low power consumption and +5V single supply operation, make it ideally suited for many video, imaging and communications applications, including use in portable equipment. Furthermore, the ADC1175 is resistant to latchup and the outputs are short-circuit proof. The top and bottom of the ADC1175's reference ladder is available for connections, enabling a wide range of input possibilities.

Industry Part Number

ADC1175

NS Part Numbers

ADC1175MW-MLS
ADC1175MW-QML

Prime Die

ADC1175

Controlling Document

SEE FEATURES SECTION

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883, Method 5005

Subgrp	Description	Temp (°C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

Features

- Internal Sample-and Hold Function
- Single +5V Operation
- Internal Reference Bias Resistors
- Industry Standard Pinout
- TRI-STATE Outputs

Key Specifications

- Resolution	8	Bits
- Maximum Sampling Frequency	20	Msps (min)
- THD	55	dB (typ)
- DNL	1.00	LSB (max)
- ENOB	7.5	Bits (typ)
- Guaranteed No Missing Codes		
- Differential Phase	0.5	Degree (typ)
- Differential Gain	0.4%	(typ)
- Power Consumption (excluding reference current)	60mW	(typ)

CONTROLLING DOCUMENTS:

ADC1175MW-QML 5962-0420801QXA

Applications

- Video Digitization
- Digital Still Cameras
- Set Top Boxes
- Communications
- Medical Imaging
- Personal Computer Video Cameras
- Digital Television
- CCD Imaging
- Electro-Optics

(Absolute Maximum Ratings)

(Note 1)

AVdd, DVdd	6.5V
Voltage on Any Pin	-0.3V to 6.5V
Vrt, Vrb	AVss to AVdd
CLK, $\overline{OE}$ Voltage	-0.5 to (AVdd +0.5V)
Digital Output Voltage	DVss to DVdd
Input Current (Note 2)	$\pm$25mA
Package Input Current (Note 2)	$\pm$50mA
Package Dissipation (Note 3)	25 C
Storage Temperature	-65 C $\leq$ Ta $\leq$ +150 C
Thermal Resistance	
ThetaJA	
(Still Air @ 0.5 C/W	110 C/W
(500 LF/Min Air flow @ 0.5 C/W	72 C/W
ThetaJC	14 C/W
Lead Temperature (Note 4)	
(Soldering, 10 seconds)	300 C
ESD Tolerance (Note 5)	
Human Body Model	2000V

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is funtional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: All voltages are measured with respect to GND = AVss = DVss = 0V, unless otherwise specified.

Note 3: When the input voltage at any pin exceeds the power supplies (that is, less than AVss or DVss, or greater than AVdd or DVdd), the current at that pin should be limited to 25mA. The 50mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 25mA to two.

Note 4: The absolute maximum junction temperatures (Tjmax) for this device is 150 degree C. The maximum allowable power dissipation is dictated by Tjmax, the junction-to-ambient thermal resistance ThetaJA, and the ambient temperature, Ta, and can be calculated using the formula PdMAX = (Tjmax - Ta) / ThetaJA.

Note 5: Human body model is 100pF capacitor discharged through a 1.5k Ohms resistor.

Recommended Operating Conditions

(Note 1, 2)

Temperature Range	-55 C ≤ Ta ≤ +125 C
AVdd, DVdd	+4.75V to +5.25V
AVdd - DVdd	<0.5V
|AVss -DVss|	0V to 100mV
Vrt	1.0V to Vdd
Vrb	0V to 4.0V
Vin Voltage Range	Vrb to Vrt

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is funtional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: All voltages are measured with respect to GND = AVss = DVss = 0V, unless otherwise specified.

Electrical Characteristics

DC PARAMETERS: DC Accuracy

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: AVdd = DVdd = +5.0Vdc, $\overline{OE}$ = 0V, Vrt = +2.6V, Vrb = 0.6V, Cl = 20pF, fclk = 20MHz AT 50% duty cycle

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
INL	Integral Non Linearity	fclk = 20MHz	1, 2			±1.3	LBS	1, 2, 3
DNL	Differential Non Linearity	fclk = 20MHz	1, 2			±.99	LSB	1, 2, 3
	Missing Codes		1, 2			0		1, 2, 3

DC PARAMETERS: Analog Input and Reference Characteristics

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: AVdd = DVdd = +5.0Vdc, $\overline{OE}$ = 0V, Vrt = +2.6V, Vrb = 0.6V, Cl = 20pF, fclk = 20MHz AT 50% duty cycle

Vin	Input Range		1, 2		Vrb	Vrt	V	1, 2, 3
Rfef	Reference Ladder Resistance	Vrt to Vrb	1, 2		200	400	Ohms	1, 2, 3
Ifef	Reference Ladder Current	Vrt = Vrts, Vrb = Vrbs	1, 2		4.8	9.3	mA	1, 2, 3
		Vrt = Vrts, Vrb = AVss	1, 2		5.4	10.5	mA	1, 2, 3
Vrb	Reference Bottom Self Bias Voltage	Vrt connected to Vrts, Vrb connected to Vrbs	1, 2		0.55	0.70	V	1, 2, 3
Vrts - Vrbs	Self Bias Voltage Delta	Vrt connected to Vrts, Vrb connected to Vrbs	1, 2		1.89	2.15	V	1, 2, 3
Vrt - Vrb	Reference Voltage Delta		1, 2		1.0	3.0	V	1, 2, 3

DC PARAMETERS: Power Supply Characteristics

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: AVdd = DVdd = +5.0Vdc, $\overline{OE}$ = 0V, Vrt = +2.6V, Vrb = 0.6V, Cl = 20pF, fclk = 20MHz AT 50% duty cycle

IAVdd + IDVdd	Total Operating Current	DVdd = AVdd = 5.25V, fclk = 20MHz	1, 2			19	mA	1, 2, 3
	Power Consumption	DVdd = AVdd = 5.25V, fclk = 20MHz	1, 2			90	mW	1, 2, 3

AC PARAMETERS: CLK, $\overline{OE}$ Digital Input Characteristics

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: AVdd = DVdd = +5.0Vdc, $\overline{OE}$ = 0V, Vrt = +2.6V, Vrb = 0.6V, Cl = 20pF, fclk = 20MHz AT 50% duty cycle

Vih	Logical High Input Voltage	DVdd = AVdd = +5.25V	1, 2		3.0		V	1, 2, 3
Vil	Logical Low Input Voltage	DVdd = AVdd = +5.25V	1, 2			1.0	V	1, 2, 3

Electrical Characteristics

AC PARAMETERS: Digital Output Characteristics

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: AVdd = DVdd = +5.0Vdc, $\overline{OE}$ = 0V, Vrt = +2.6V, Vrb = 0.6V, Cl = 20pF, fclk = 20MHz AT 50% duty cycle

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Ioh	High Level Output Current	DVdd = 4.75V, Voh = 2.4V	1, 2		-1.1		mA	1, 2, 3
Iol	Low Level Output Current	DVdd = 4.75V, Vol = 0.4V	1, 2			1.6	mA	1, 2, 3

AC PARAMETERS: AC ELECTRICAL CHARACTERISTICS

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: AVdd = DVdd = +5.0Vdc, $\overline{OE}$ = 0V, Vrt = +2.6V, Vrb = 0.6V, Cl = 20pF, fclk = 20MHz AT 50% duty cycle

fc1	Maximum Conversion Rate		1, 2		20		MHz	4, 5, 6
ENOB	Effective Number of Bits	fin = 4.43MHz, Vin = FS - 2LSB	1, 2		6.5		Bits	4, 5, 6
SINAD	Signal-to-Noise & Distortion	fin = 4.43MHz, Vin = FS - 2LSB	1, 2		40		dB	4, 5, 6
SNR	Signal-to-Noise Ratio	fin = 4.43MHz, Vin = FS - 2LSB	1, 2		40		dB	4, 5, 6

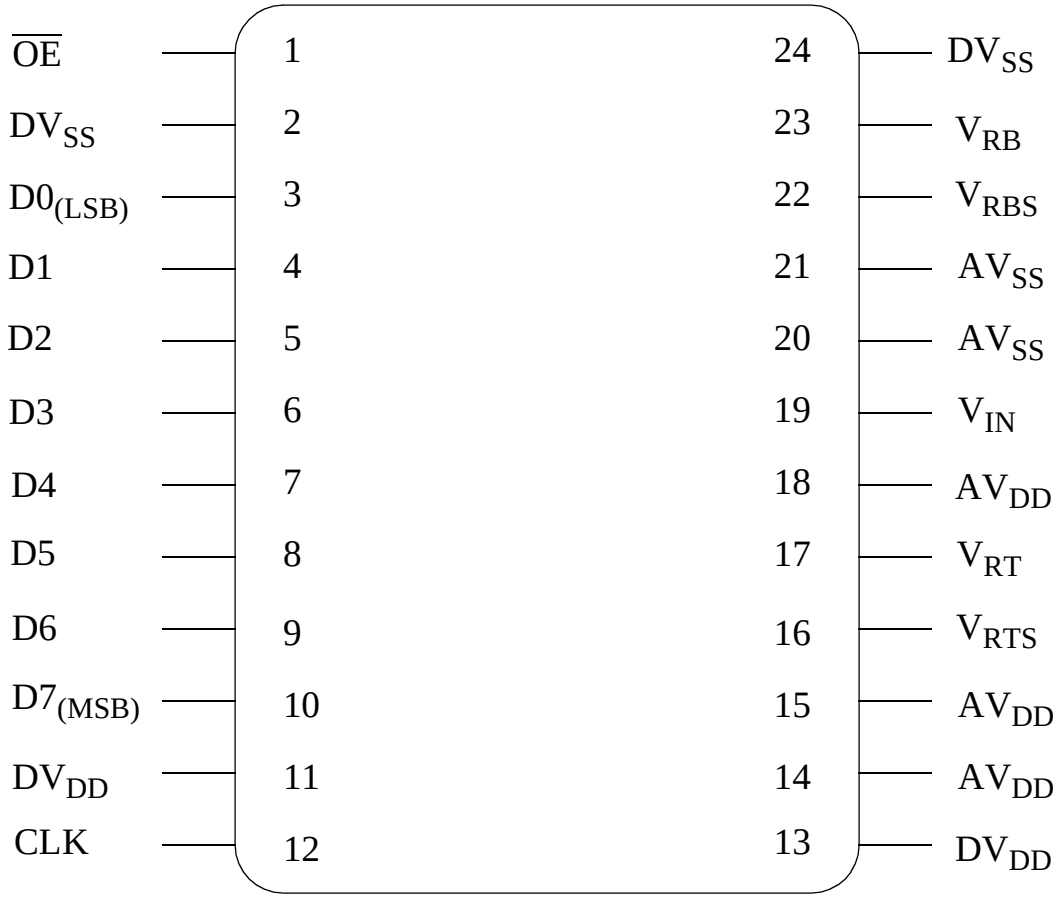
Note 1: The analog inputs are protected as shown below. Input voltage magnitudes up to 6.5V or to 500mV below GND will not damage this device. However, errors in the A/D conversion can occur if the input goes above Vdd or below GND by more than 50mV. As an example, if AVdd is 4.75Vdc, the full-scale input voltage must be $\leq$4.80Vdc to ensure accurate conversions.

Note 2: To guarantee accuracy, it is required that AVdd and DVdd be well bypassed. Each supply pin must be decoupled with separate bypass capacitors.

Graphics and Diagrams

GRAPHICS#	DESCRIPTION
06405HRA1	CERPACK (W), 14 LEAD (B/I CKT)
P000487A	CERPACK (W), 24 LEAD (PIN OUT)
W24CRF	CERPACK (W), 24 LEAD (P/P DWG)

See attached graphics following this page.



ADC1175W

24 - LEAD W

CONNECTION DIAGRAM

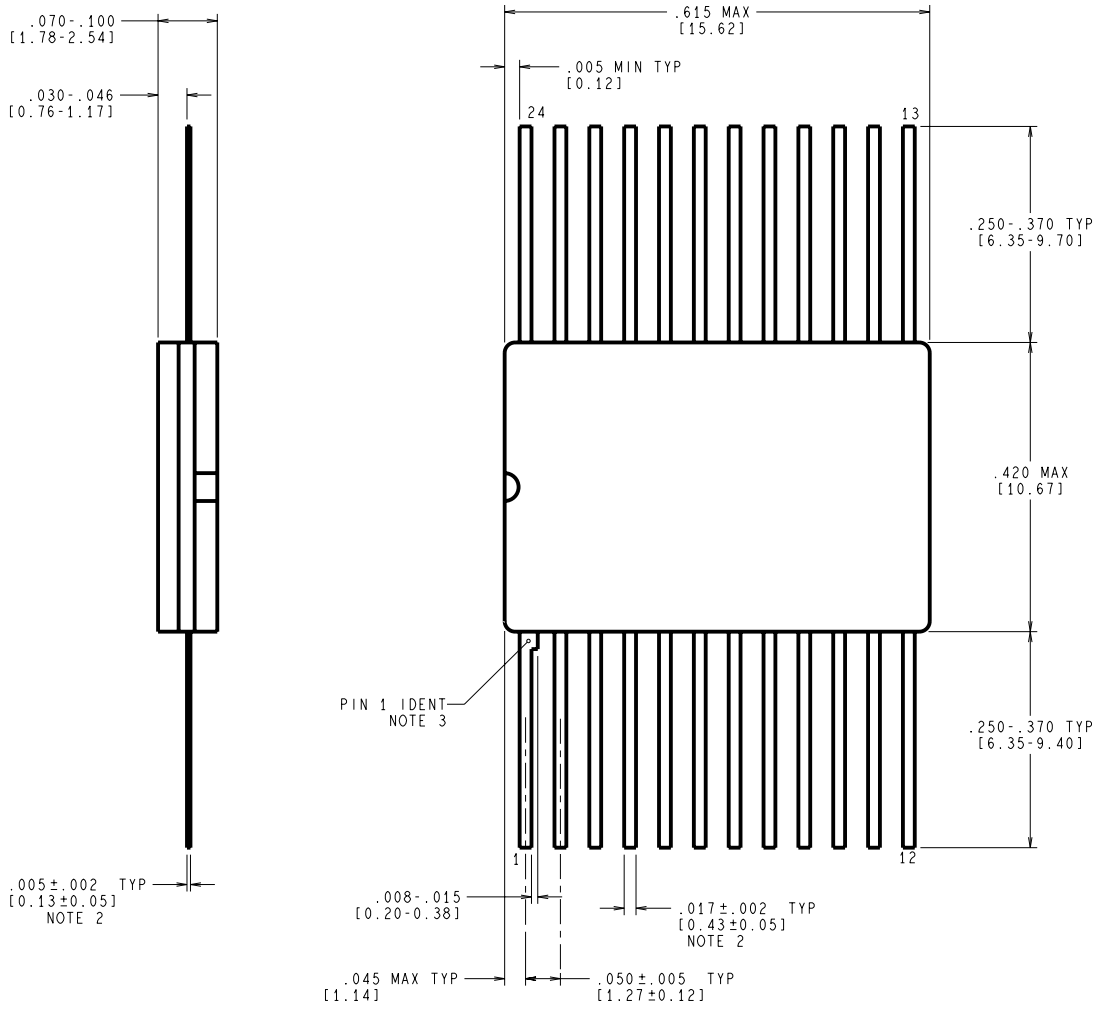
TOP VIEW

P000487A

National Semiconductor

MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
F	REVISE AND REDRAW PER CURRENT STANDARD; UPDATE TITLE & MIL/AERO STAMP.	11046	07/13/95	MS/



CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS

NOTES: UNLESS OTHERWISE SPECIFIED

1. LEAD FINISH: SOLDER DIPPED WITH Sn60 OR Sn63
   SOLDER CONFORMING TO A MINIMUM THICKNESS
   OF 200 MICROINCHES/ 5.08 MICROMETERS.
   SOLDER MAY BE APPLIED OVER LEAD BASIS METAL OR Sn PLATE.
2. LEAD THICKNESS MAY BE INCREASED BY .003 INCHES/ 0.08 MILLIMETERS
   MAXIMUM AFTER LEAD FINISH APPLIED.
3. LEAD 1 IDENTIFICATION SHALL BE:
   a) A NOTCH OR OTHER MARK WITHIN THIS AREA
   b) A TAB ON LEAD 1, EITHER SIDE
4. NO JEDEC REGISTRATION AS OF 07/17/95.

MIL-PRF-38535
CONFIGURATION CONTROL

APPROVALS	DATE
DRAWN: MARTA SUCHY	07/13/95
DFTG. CHK.	
ENGR. CHK.	

PROJECTION INCH [MM]

National Semiconductor
2900 Semiconductor dr, Santa Clara, CA 95052-8090

CERPAC, 24 LEAD

SCALE	SIZE	DRAWING NUMBER	REV
N/A	C	MKT-W24C	F

DO NOT SCALE DRAWING | SHEET 1 of 1

Revision History

Rev	ECN #	Rel Date	Originator	Changes
0A0	M0004170	05/13/04	Rose Malone	Initial MDS Release: MNADC1175-X, Rev. 0A0
1A0	M0004380	05/13/04	Rose Malone	Update MDS: MNADC1175-X, Rev. 0A0 to 1A0. Electrical Section - Limit changes for the following symbols: DNL from ±1.0 to ±.99 LSB, Vrb MAX from 0.65 to 0.70V, Vrt - Vrb MAX from 2.8 to 3.0V. Deleted Video Accuracy Section, and in AC Electrical Characteristics Section symbols: SFDR and THD.