National Semiconductor

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CD4023M/CD4023C Triple 3-Input NAND Gate
CD4025M/CD4025C Triple 3-Input NOR Gate

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General Description

These triple gates are monolithic complementary MOS (CMOS) integrated circuits constructed with N- and P-channel enhancement mode transistors. All inputs are protected against static discharge with diodes to V_{DD} and V_{SS}.

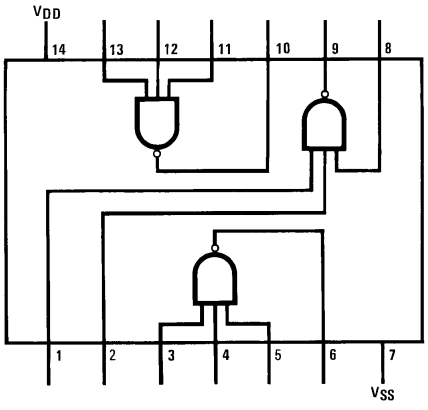
Features

■ Wide supply voltage range	3.0V to 15V
■ High noise immunity	0.45 V_{DD} (typ.)
■ 5V–10V parametric ratings	
■ Low power	

Connection Diagrams

Dual-In-Line Packages

CD4023M/CD4023C



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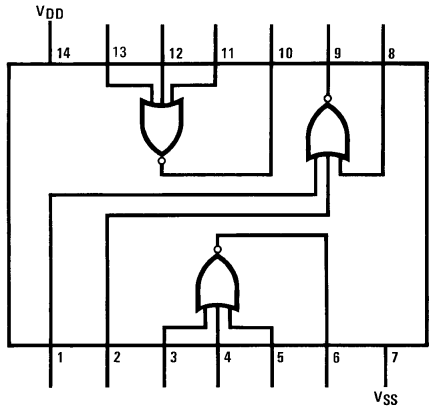
Top View

CD4025M/CD4025C



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Top View

Order Number CD4023 or CD4025

RRD-B30M105/Printed in U. S. A.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage at Any Pin	$V_{SS}-$ to $V_{DD}+0.3V$
Operating Temperature Range	
CD4023M, CD4025M	$-55°C$ to $+125°C$
CD4023C, CD4025C	$-40°C$ to $+85°C$
Storage Temperature Range	$-65°C$ to $+150°C$
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Operating V_{DD} Range	$V_{SS}+3.0V$ to $V_{SS}+15V$
Lead Temperature	
(Soldering, 10 seconds)	260°C

DC Electrical Characteristics CD4023M, CD4025M

Symbol	Parameter	Conditions	Limits							Units
			$-55°C$		$+25°C$			$+125°C$		
			Min	Max	Min	Typ	Max	Min	Max	
I_L	Quiescent Device Current	$V_{DD}=5.0V$		0.05		0.001	0.05		3.0	μA
		$V_{DD}=10V$		0.1		0.001	0.1		6.0	μA
P_D	Quiescent Device Dissipation/Package	$V_{DD}=5.0V$		0.25		0.005	0.25		15	μW
		$V_{DD}=10V$		1.0		0.01	1.0		60	μW
V_{OL}	Output Voltage Low Level	$V_{DD}=5.0V, V_I=V_{DD}, I_O=0A$		0.05		0	0.05		0.05	V
		$V_{DD}=10V, V_I=V_{DD}, I_O=0A$		0.05		0	0.05		0.05	V
V_{OH}	Output Voltage High Level	$V_{DD}=5.0V, V_I=V_{SS}, I_O=0A$	4.95		4.95	5.0		4.95		V
		$V_{DD}=10V, V_I=V_{SS}, I_O=0A$	9.95		9.95	10		9.95		V
V_{NL}	Noise Immunity (All Inputs)	$V_{DD}=5.0V, V_O=3.6V, I_O=0A$	1.5		1.5	2.25		1.4		V
		$V_{DD}=10V, V_O=7.2V, I_O=0A$	3.0		3.0	4.5		2.9		V
V_{NH}	Noise Immunity (All Inputs)	$V_{DD}=5.0V, V_O=0.95V, I_O=0A$	1.4		1.5	2.25		1.5		V
		$V_{DD}=10V, V_O=2.9V, I_O=0A$	2.9		3.0	4.5		3.0		V
I_DN	Output Drive Current N-Channel (4025) (Note 2)	$V_{DD}=5.0V, V_O=0.4V, V_I=V_{DD}$	0.5		0.40	1.0		0.28		mA
		$V_{DD}=10V, V_O=0.5V, V_I=V_{DD}$	1.1		0.9	2.5		0.65		mA
I_DP	Output Drive Current P-Channel (4025) (Note 2)	$V_{DD}=5.0V, V_O=2.5V, V_I=V_{SS}$	-0.62		-0.5	-2.0		-0.35		mA
		$V_{DD}=10V, V_O=9.5V, V_I=V_{SS}$	-0.62		-0.5	-1.0		-0.35		mA
I_DN	Output Drive Current N-Channel (4023) (Note 2)	$V_{DD}=5.0V, V_O=0.4V, V_I=V_{DD}$	0.31		0.25	0.5		0.175		mA
		$V_{DD}=10V, V_O=0.5V, V_I=V_{DD}$	0.63		0.5	0.6		0.35		mA
I_DP	Output Drive Current P-Channel (4023) (Note 2)	$V_{DD}=5.0V, V_O=2.5V, V_I=V_{SS}$	-0.31		-0.25	-0.5		-0.175		mA
		$V_{DD}=10V, V_O=9.5V, V_I=V_{SS}$	-0.75		-0.6	-1.2		-0.4		mA
I_I	Input Current					10				pA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

Note 2: I_DN and I_DP are tested one output at a time.

DC Electrical Characteristics CD4023C, CD4025C

Symbol	Parameter	Conditions	Limits							Units
			−40°C		+25°C			+85°C		
			Min	Max	Min	Typ	Max	Min	Max	
I_L	Quiescent Device Current	$V_{DD} = 5.0V$ $V_{DD} = 10V$		0.05 5.0		0.005 0.005	0.5 5.0		15 30	μA μA
P_D	Quiescent Device Dissipation/Package	$V_{DD} = 5.0V$ $V_{DD} = 10V$		2.5 50		0.025 0.05	2.5 50		75 300	μW μW
V_{OL}	Output Voltage Low Level	$V_{DD} = 5.0V$, $V_I = V_{DD}$, $I_O = 0A$ $V_{DD} = 10V$, $V_I = V_{DD}$, $I_O = 0A$		0.01 0.01		0 0	0.01 0.01		0.05 0.05	V V
V_{OH}	Output Voltage High Level	$V_{DD} = 5.0V$, $V_I = V_{SS}$, $I_O = 0A$ $V_{DD} = 10V$, $V_I = V_{SS}$, $I_O = 0A$	4.99 9.99		4.99 9.99	5.0 10		4.95 9.95		V V
I_I	Input Current					10				pA
V_{NL}	Noise Immunity (All Inputs)	$V_{DD} = 5.0V$, $V_O = 3.6V$, $I_O = 0A$ $V_{DD} = 10V$, $V_O = 7.2V$, $I_O = 0A$	1.5 3.0		1.5 3.0	2.25 4.5		1.4 2.9		V V
V_{NH}	Noise Immunity (All Inputs)	$V_{DD} = 5.0V$, $V_O = 0.95V$, $I_O = 0A$ $V_{DD} = 10V$, $V_O = 2.9V$, $I_O = 0A$	1.4 2.9		1.5 3.0	2.25 4.5		1.5 3.0		V V
I_DN	Output Drive Current N-Channel (4025) (Note 2)	$V_{DD} = 5.0V$, $V_O = 0.4V$, $V_I = V_{DD}$ $V_{DD} = 10V$, $V_O = 0.5V$, $V_I = V_{DD}$	0.35 0.72		0.3 0.6	1.0 2.5		0.24 0.48		mA mA
I_DP	Output Drive Current P-Channel (4025) (Note 2)	$V_{DD} = 5.0V$, $V_O = 2.5V$, $V_I = V_{SS}$ $V_{DD} = 10V$, $V_O = 9.5V$, $V_I = V_{SS}$	−0.35 −0.3		−0.3 −0.25	−2.0 −1.0		−0.24 −0.2		mA mA
I_DN	Output Drive Current N-Channel (4023) (Note 2)	$V_{DD} = 5.0V$, $V_O = 0.4V$, $V_I = V_{DD}$ $V_{DD} = 10V$, $V_O = 0.5V$, $V_I = V_{DD}$	0.145 0.3		0.12 0.25	0.5 0.6		0.095 0.2		mA mA
I_DP	Output Drive Current P-Channel (4023) (Note 2)	$V_{DD} = 5.0V$, $V_O = 2.5V$, $V_I = V_{SS}$ $V_{DD} = 10V$, $V_O = 9.5V$, $V_I = V_{SS}$	−0.145 −0.35		−0.12 −0.3	−0.5 −1.2		−0.095 −0.24		mA mA
I_I	Input Current					10				pA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

Note 2: I_DN and I_DP are tested one output at a time.

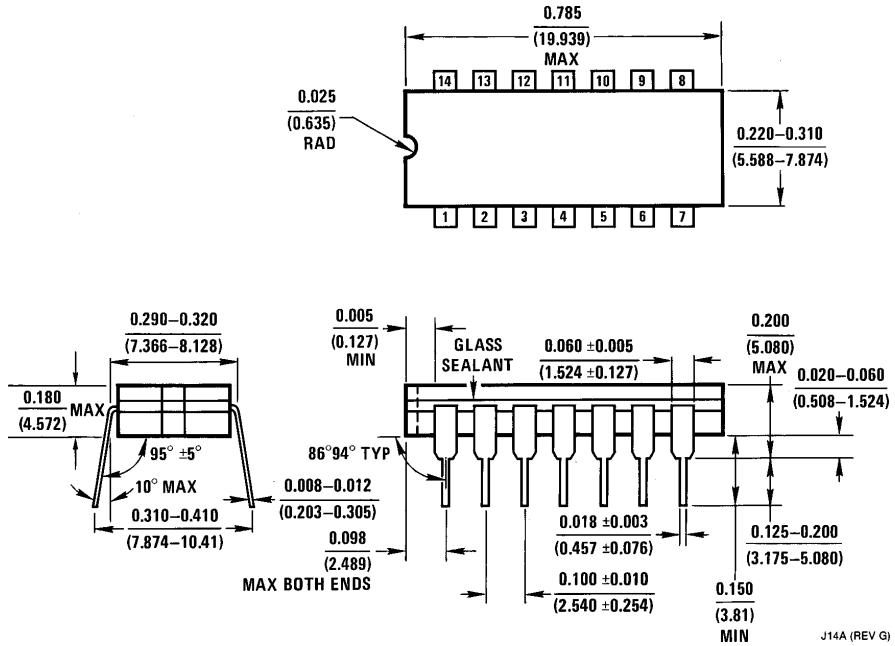
AC Electrical Characteristics*

$T_A = 25°C$, $C_L = 15$ pF, and input rise and fall times = 20 ns. Typical temperature coefficient for all values of $V_{DD} = 0.3\%/°C$

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CD4025M						
t_{PHL}	Propagation Delay Time High to Low Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		35 25	50 40	ns ns
t_{PLH}	Propagation Delay Time Low to High Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		35 25	40 70	ns ns
t_{THL}	Transition Time High to Low Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		65 35	125 70	ns ns
t_{TLH}	Transition Time Low to High Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		65 35	175 75	ns ns
C_I	Input Capacitance	Any Input		5.0		pF
CD4025C						
t_{PHL}	Propagation Delay Time High to Low Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		35 25	80 55	ns ns
t_{PLH}	Propagation Delay Time Low to High Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		35 25	120 65	ns ns
t_{THL}	Transition Time High to Low Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		65 35	200 115	ns ns
t_{TLH}	Transition Time Low to High Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		65 35	300 125	ns ns
C_I	Input Capacitance	Any Input		5.0		pF
CD4023M						
t_{PHL}	Propagation Delay Time High to Low Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		50 25	75 40	ns ns
t_{PLH}	Propagation Delay Time Low to High Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		50 25	75 40	ns ns
t_{THL}	Transition Time High to Low Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		75 50	125 75	ns ns
t_{TLH}	Transition Time Low to High Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		75 40	100 60	ns ns
C_I	Input Capacitance	Any Input		5.0		pF
CD4023C						
t_{PHL}	Propagation Delay Time High to Low Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		50 25	100 50	ns ns
t_{PLH}	Propagation Delay Time Low to High Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		50 25	100 50	ns ns
t_{THL}	Transition Time High to Low Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		75 50	150 100	ns ns
t_{TLH}	Transition Time Low to High Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		75 40	125 75	ns ns
C_I	Input Capacitance	Any Input		5.0		pF

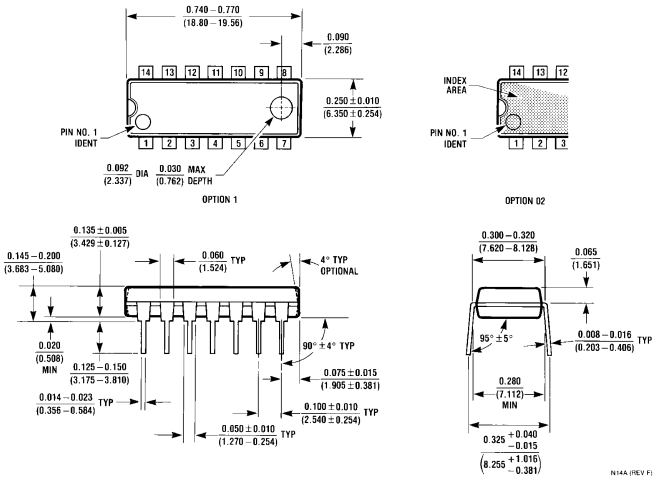
*AC Parameters are guaranteed by DC correlated testing.

Physical Dimensions inches (millimeters)



Ceramic Dual-In-Line Package (J)
Order Number CD4023MJ, CD4023CJ, CD4025MJ or CD4025CJ
NS Package Number J14A

Physical Dimensions inches (millimeters) (Continued)



Molded Dual-In-Line Package (N)
Order Number CD4023MN, CD4023CN, CD4025MN or CD4025CN
NS Package Number N14A

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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