National Semiconductor

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Comlinear CLC400
Fast Settling, Wideband Low-Gain Monolithic Op Amp

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General Description

The CLC400 is a high-speed, fast-settling operational amplifier designed for low-gain applications. Constructed using a unique, proprietary design and an advanced complementary bipolar process, the CLC400 offers performance far beyond that normally offered by ordinary monolithic op amps. In addition, unlike many other high-speed op amps the CLC400 offers both high performance and stability without the need for compensation circuitry—even at a gain of +1.

The fast 12ns settling to 0.05% and its ability to drive capacitive loads makes the CLC400 an ideal flash A/D driver. The wide bandwidth of 200MHz and the very linear phase ensure unsurpassed signal fidelity. Systems employing digital to analog converters also benefit from the use of the CLC400—especially if linearity and drive levels are important to system performance.

The CLC400 provides a simple, high-performance solution for video distribution and line driving applications. The 50mA output current and guaranteed specifications for 100 ohm loads provide ample drive capability and assured performance.

The CLC400 is based on Comlinear's proprietary op amp topology that uses current feedback instead of the usual voltage feedback. This unique design has many advantages over conventional designs (such as settling time that is relatively independent of gain), yet it is used in basically the same way (see the gain equations in Figures 1 and 2, page 4). However, an understanding of the topology will aid in achieving the best performance. The following discussion will proceed for the non-inverting gain configuration with the inverting mode analysis being very similar.

The CLC400 is available in several versions to meet a variety of requirements. A three-letter suffix determines the version:

CLC400AJP	-40°C to +85°C	8-pin plastic DIP
CLC400AJE	-40°C to +85°C	8-pin plastic SOIC
CLC400AIB	-40°C to +85°C	8-pin hermetic CERDIP
CLC400A8B	-55°C to +125°C	8-pin hermetic CERDIP, MIL-STD-833, Level B
CLC400ALC	-40°C to +85°C	dice
CLC400AMC	-55°C to +125°C	dice qualified to Method 5008, MIL-STD-883, Level B
CLC400AID	-40°C to +85°C	8-pin sidebrazed CERDIP
CLC400A8D	-55°C to +125°C	8-pin sidebrazed CERDIP, MIL-STD-883, Level B

DESC SMD number: 5962-89970

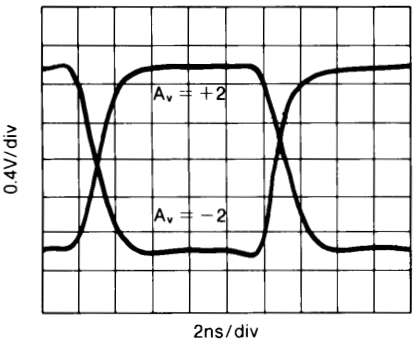
Features

- -3dB bandwidth of 270MHz
- 0.05% settling in 12ns
- Low power, 150mW
- Low distortion, -60dBc at 20MHz
- Stable without compensation
- Overload and short circuit protected
- ±1 to ±8 closed-loop gain range

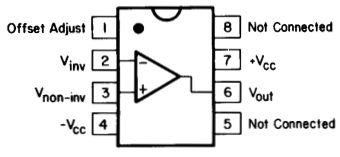
Applications

- Flash, precision A/D conversion
- Video distribution
- Line drivers
- D/A current-to-voltage conversion
- Photodiode, CCD preamps
- IF processors
- High-speed communications

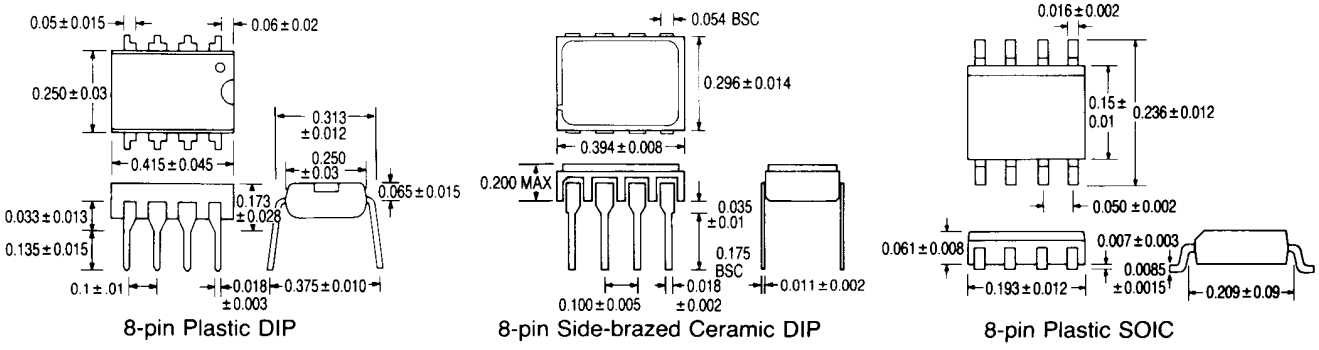
Pulse Response



Pinout
DIP & SOIC



Package Dimensions



CLC400 Electrical Characteristics (A_V = +2, V_{cc} = ±5V, R_L = 100Ω, R_f = 250Ω; unless specified)

PARAMETERS	CONDITIONS	TYP	MAX & MIN RATINGS			UNITS	SYMBOL
Ambient Temperature	CLC400AJ/AI	+25°C	−40°C	+25°C	+85°C		
Ambient Temperature	CLC400A8/AM/AL	+25°C	−55°C	+25°C	+125°C		
FREQUENCY DOMAIN RESPONSE							
†−3dB bandwidth	V_{out}<0.5V_{pp}	200	150	150	120	MHz	SSBW
	V_{out}<5V_{pp}, A_v = + 5	50	35	35	35	MHz	LSBW
gain flatness[1]	V_{out}<0.5$_{pp}$						
† peaking	<40MHz	0	0.4	0.3	0.4	dB	GFPL
† peaking	>40MHz	0	0.7	0.5	0.7	dB	GFPH
† rolloff	<75MHz	0.6	1.0	1.0	1.3	dB	GFR
linear phase deviation	to 75MHz	0.2	1.0	1.0	1.2	°	LPD
TIME DOMAIN RESPONSE							
rise and fall time	0.5V step	1.6	2.4	2.4	2.4	ns	TRS
	5V step	6.5	10	10	10	ns	TRL
settling time to ±0.1%	2V step	10	13	13	13	ns	TSP
±0.05%	2V step	12	15	15	15	ns	TS
overshoot	0.5V step	0	15	10	10	%	OS
slew rate A_v = +2		700	430	430	430	V/μs	SR
A_v = −2		1600	—	—	—	V/μs	SR1
DISTORTION AND NOISE RESPONSE							
†2nd harmonic distortion	2V_{pp}, 20MHz	−60	−40	−45	−45	dBc	HD2
†3rd harmonic distortion	2V_{pp}, 20MHz	−60	−50	−50	−50	dBc	HD3
equivalent input noise							
noise floor	>1MHz	−157	−154	−154	−153	dBm(1Hz)	SNF
integrated noise	1MHz to 200MHz	40	57	57	63	μV	INV
STATIC, DC PERFORMANCE							
*input offset voltage		2	±8.2	±5.0	±9.0	mV	VIO
average temperature coefficient		20	±40	—	±40	μV/°C	DVIO
*input bias current	non-inverting	10	±36	±20	±20	μA	IBN
average temperature coefficient		100	±200	—	±100	nA/°C	DIBN
*input bias current	inverting	10	±36	±20	±30	μA	IBI
average temperature coefficient		50	±200	—	±100	nA/°C	DIBI
‡power supply rejection ratio		50	45	45	45	dB	PSRR
common mode rejection ratio		50	45	45	45	dB	CMRR
*supply current	no load	15	23	23	23	mA	ICC
MISCELLANEOUS PERFORMANCE							
non-inverting input	resistance	200	>50	>100	>100	kΩ	RIN
	capacitance	0.5	<2.0	<2.0	<2.0	pF	CIN
output impedance	at DC	0.1	<0.2	<0.2	<0.2	Ω	RO
output voltage range	no load	±3.5	>3.0	>3.2	>3.2	V	VO
common mode input range	for rated performance	±2.1	>1.2	>2.0	>2.0	V	CMIR
output current	−40°C to +85°C	±70	>35	>50	>50	mA	IO
	−55°C to +125°C	±70	>30	>50	>50	mA	IO

Min/max ratings are based on product characterization and simulation. Individual parameters are tested as noted. Outgoing quality levels are determined from tested parameters.

Absolute Maximum Ratings

V_{cc}	±7V
I_{out} output is short circuit protected to ground, but maximum reliability will be maintained if I_{out} does not exceed...	70mA
common mode input voltage	±V_{cc}
differential input voltage	10V
junction temperature	+ 175°C
operating temperature range	
AI/AJ:	− 40°C to + 85°C
A8/AM/AL:	− 55°C to + 125°C
storage temperature range	− 65°C to + 150°C
lead solder duration (+ 300°C)	10 sec

Miscellaneous Ratings

recommended gain range ±1 to ±8

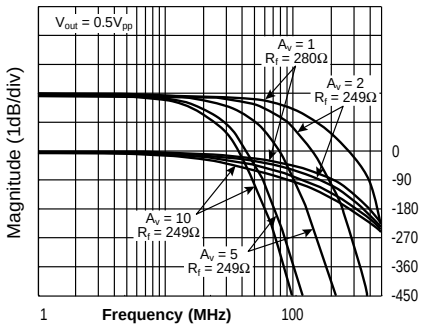
NOTES:

*	AI, AJ	100% tested at + 25°C, sample at + 85°C.
†	AJ	Sample tested at + 25°C.
†	AI	100% tested at + 25°C.
*	A8	100% tested at + 25°C, −55°C, + 125°C.
†	A8	100% tested at + 25°C, sample − 55°C, +125°C.
*	AL,AM	100% wafer probe tested at + 25°C to + 25°C min/max specifications.

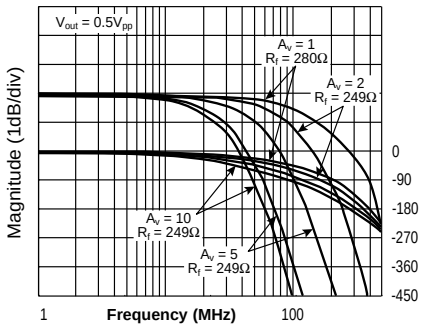
note 1: Gain flatness tests performed from 0.1MHz.

CLC400 Typical Performance Characteristics (T_A = 25°, A_V = +2, V_{CC} = ±5V, R_L = 100Ω; unless specified)

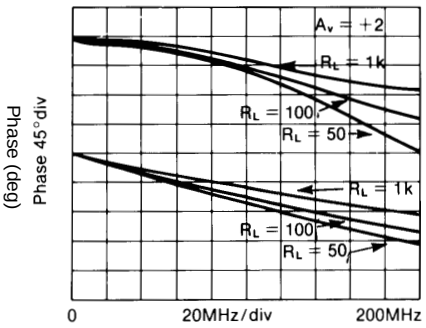
Non-Inverting Frequency Response



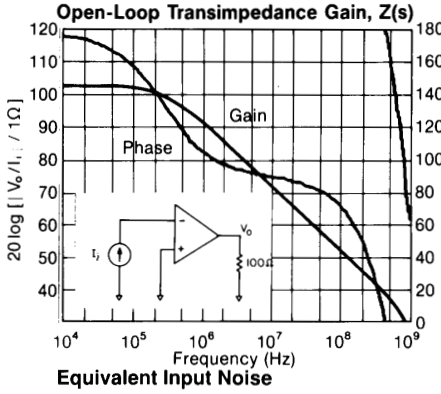
Non-Inverting Frequency Response



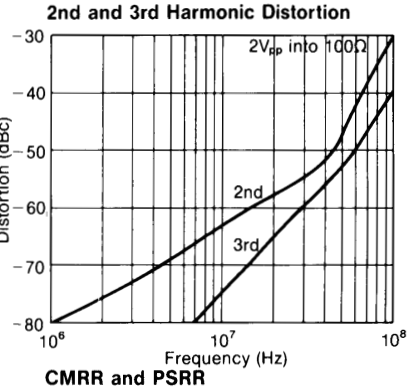
Frequency Response for Various R_Ls



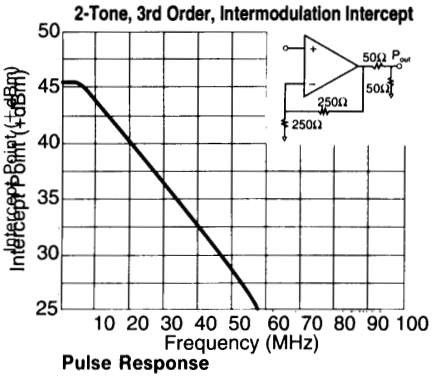
Open-Loop Transimpedance Gain, Z(s)



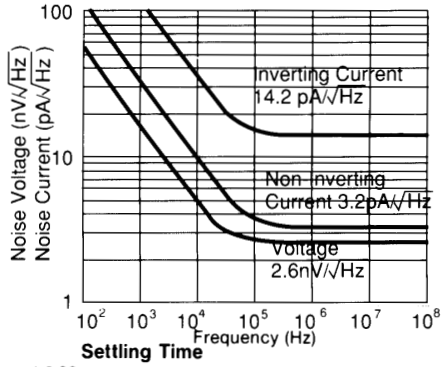
2nd and 3rd Harmonic Distortion



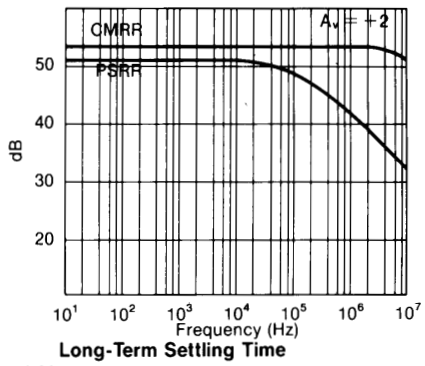
2-Tone, 3rd Order, Intermodulation Intercept



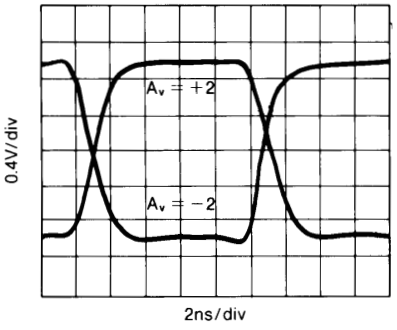
Equivalent Input Noise



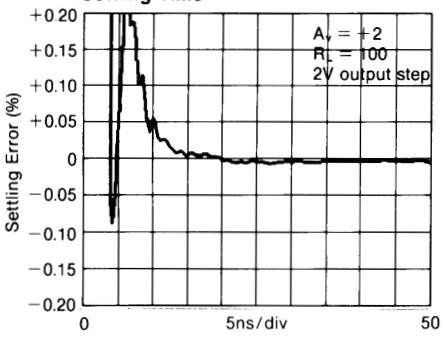
CMRR and PSRR



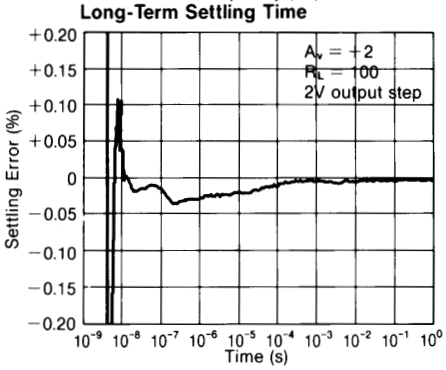
Pulse Response



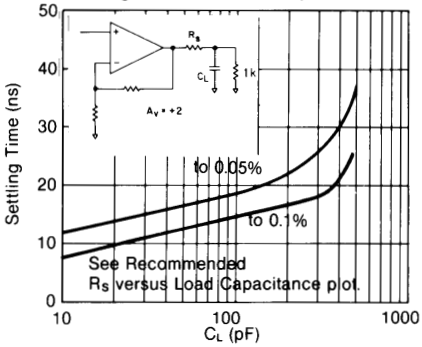
Settling Time



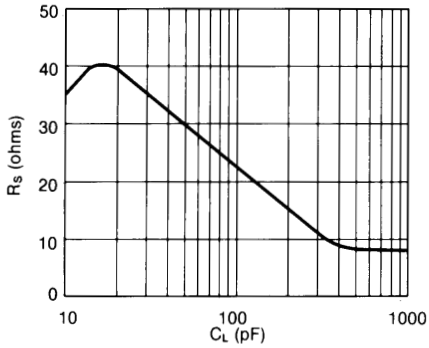
Long-Term Settling Time



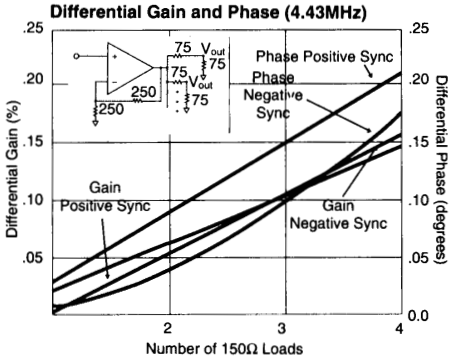
Settling Time vs. Load Capacitance



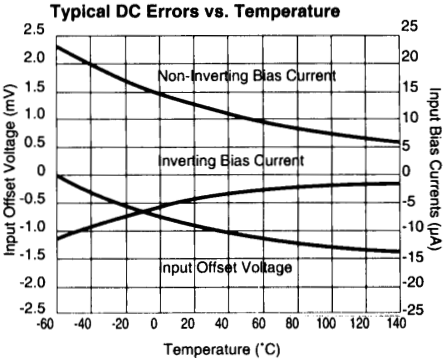
Recommended R_S vs. Load Capacitance



Differential Gain and Phase (4.43MHz)



Typical DC Errors vs. Temperature



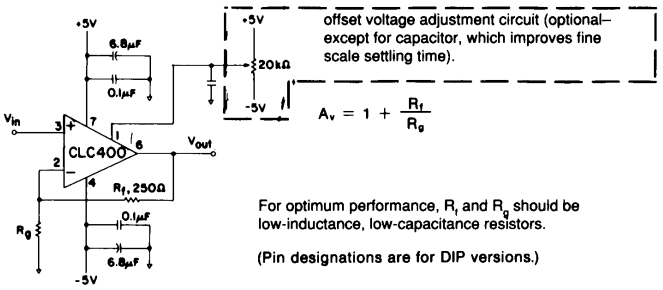


Figure 1: recommended non-inverting gain circuit

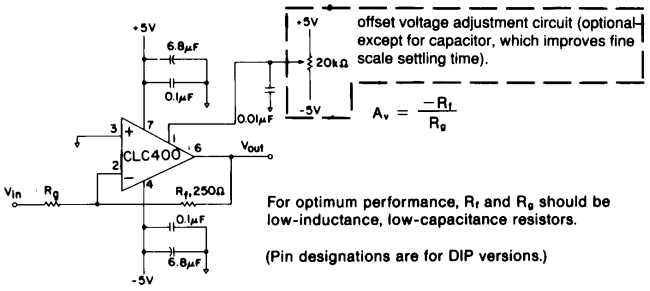


Figure 2: recommended inverting gain circuit

Understanding the Loop Gain

Referring to the equivalent circuit of Figure 3, any current flowing in the inverting input is amplified to a voltage at the output through the transimpedance gain shown on the plots on page 3. This Z(s) is analogous to the open-loop gain of a voltage feedback amplifier.

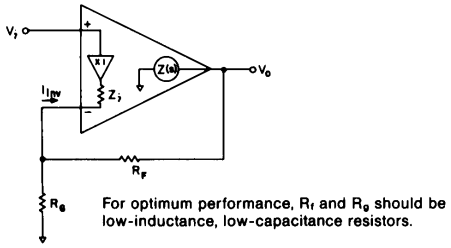


Figure 3: current feedback topology

Developing the non-inverting frequency response for the topology of Figure 3 yields:

$$\frac{V_o}{V_i} = \frac{1 + R_f/R_g}{1 - 1/LG} \qquad \text{Eq. (1)}$$

where LG is the loop gain defined by,

$$LG = \frac{Z(s)}{R_f} \times \frac{1}{1 + Z_i/(R_f \,||\, R_g)} \qquad \text{Eq. (2)}$$

Equation 1 has a form identical to that for a voltage feedback amplifier with the differences occurring in the LG expression, Equation 2. For an idealized treatment, set $Z_i = 0$ which results in a very simple $LG = Z(s)/R_f$ (Derivation of the transfer function for the case where $Z_i = 0$ is given in Application Note AN300-1). Using the Z(s) (open-loop transimpedance gain) plot shown on the previous page and dividing by the recommended $R_f = 250\Omega$, yields a large loop gain at DC. As a result, Equation 1 shows that the closed-loop gain at DC is very close to $(1 + R_f/R_g)$.

At higher frequencies, the roll-off of Z(s) determines the closed-loop frequency response which, ideally, is dependent only on R_f. **The specifications reported on the previous pages are therefore valid only for the specified $R_f = 250\Omega$.** Increasing R_f from 250Ω will decrease the loop gain and bandwidth, while decreasing it will increase the loop gain possibly leading to inadequate phase margin and closed-loop peaking. Conversely, fixing R_f will hold the frequency response constant while the closed-loop gain can be adjusted using R_g.

The CLC400 departs from this idealized analysis to the extent that the inverting input impedance is finite. With the low quiescent power of the CLC400, $Z_i = 50\Omega$ leading to a drop in loop gain and bandwidth at high gain settings, as given by Equation 2. The second term in Equation 2 accounts for the division in feedback current that occurs between Z_i and $R_f||R_g$ at the inverting node of the CLC400. This decrease in bandwidth can be circumvented as described in "Increasing Bandwidth at High Gains."

DC Accuracy and Noise

Since the two inputs for the CLC400 are quite dissimilar, the noise and offset error performance differs somewhat from that of a standard differential input amplifier. Specifically, the inverting input current noise is much larger than the non-inverting current noise. Also the two input bias currents are physically unrelated rendering bias current cancellation through matching of the inverting and non-inverting pin resistors ineffective.

In Equation 3, the output offset is the algebraic sum of the equivalent input voltage and current sources that influence DC operation. Output noise is determined similarly except that a root-sum-of-squares replaces the algebraic sum. R_s is the non-inverting pin resistance.

$$\text{Output Offset } V_o = \pm IBN \times R_s (1 + R_f/R_g) \pm VIO\,(1 + R_f/R_g) \pm IBI \times R_f \qquad \text{Eq. (3)}$$

An important observation is that for fixed R_f, offsets as referred to the input improve as the gain is increased (divide all terms by $1 + R_f/R_g$). A similar result is obtained for noise where noise figure improves as gain increases.

Selecting Between the CLC400 or CLC401

The CLC400 is intended for gains of ±1 to ±8 while the CLC401 is designed for gains of ±7 to ±50. Optimum performance is achieved with a feedback resistor of 250Ω with the CLC400 and 1.5kΩ with the CLC401—this distinction may be important in transimpedance applications such as D/A buffering. Although the CLC400 can be used at higher gains, the CLC401 will provide a wider bandwidth because loop gain losses due to finite Z_i are lower with the larger CLC401 feedback resistor as explained above. On the other hand, the lower recommended feedback resistance of the CLC400 minimizes the output errors due to inverting input noise and bias currents.

Increasing Bandwidth At High Gains

Bandwidth may be increased at high closed-loop gains by adjusting R_f and R_g to make up for the losses in loop gain that occur at these high gain settings due to current division at the inverting input. An approximate relationship may be obtained by holding the LG expression constant as the gain is changed from the design point used in the specifications (that is, $R_f = 250\Omega$ and $R_g = 250\Omega$). For the CLC400 this gives,

$$R_f = 350 - 50A_v \text{ and } R_g = \frac{350 - 50A_v}{A_v - 1} \qquad \text{Eq. (4)}$$

where A_v is the non-inverting gain. Note that with $A_v = +2$ we get the specified $R_f = 250\Omega$, while at higher gains, a lower value gives stable performance with improved bandwidth.

Capacitive Feedback

Capacitive feedback should not be used with the CLC400 because of the potential for loop instability. See Application Note OA-7 for active filter realizations with the CLC400.

Offset Adjustment Pin

Pin 1 can be connected to a potentiometer as shown in Figure 1 and used to adjust the input offset of the CLC400. Full range adjustment of ±5V on pin 1 will yield a ±10mV input offset adjustment range. Pin 1 should always be bypassed to ground with a ceramic capacitor located close to the package for best settling performance.

Printed Circuit Layout

As with any high frequency device, a good PCB layout will enhance performance. Ground plane construction and good power supply bypassing close to the package are critical to achieving full performance. In the non-inverting configuration, the amplifier is sensitive to stray capacitance to ground at the inverting input. Hence, the inverting node connections should be small with minimal coupling to the ground plane. Shunt capacitance across the feedback resistor should not be used to compensate for this effect.

Parasitic or load capacitance directly on the output will introduce additional phase shift in the loop degrading the loop phase margin and leading to frequency response peaking. A small series resistor before the capacitance effectively decouples this effect. The graphs on the preceding page illustrate the required resistor value and resulting performance vs. capacitance.

Precision buffed resistors (PRP8351 series from Precision Resistive Products) with low parasitic reactances were used to develop the data sheet specifications. Precision carbon composition resistors will also yield excellent results. Standard spirally-trimmed RN55D metal film resistors will work with a slight decrease in bandwidth due to their reactive nature at high frequencies.

Evaluation PC boards (part no. 730013 for through-hole and 730027 for SOIC) for the CLC400 are available.

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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