National Semiconductor

MICROCIRCUIT DATA SHEET

MNCLC425A-X REV 1A0

Original Creation Date: 02/27/03
Last Update Date: 08/15/03
Last Major Revision Date: 08/13/03

ULTRA LOW NOISE WIDEBAND OP AMP

General Description

The Comlinear CLC425 combines a wide bandwidth (1.9GHz GBW) with very low input noise (1.05nV/SqRtHz, 1.6pA/SqRtHz) and low dc errors (100uV Vos, 2uV/ C drift) to provide a very precise, wide dynamic-range op amp offering closed-loop gains of $\geq$ 10.

Singularly suited for very wideband high-gain operation, the CLC425 employs a traditional voltage-feedback topology providing all the benefits of balanced inputs, such as low offsets and drifts, as well as a 96dB open-loop gain, a 100dB CMRR and a 95dB PSRR.

The CLC425 also offers great flexibility with its externally adjustable supply current, allowing designers to easily choose the optimum set of power, bandwidth, noise and distortion performance. Operating from $\pm$5V power supplies, the CLC425 defaults to a 15mA quiescent current, or by adding one external resistor, the supply current can be adjusted to less than 5mA.

The CLC425's combination of ultra-low noise, wide gain-band-width, high slew rate and low dc errors will enable applications in areas such as medical diagnostic ultrasound, magnetic tape & disk storage, communications and opto-electronics to achieve maximum high-frequency signal-to-noise ratios.

Industry Part Number

CLC425A

NS Part Numbers

CLC425AJ-MLS
CLC425AJ-QML

Prime Die

UB1703B

Controlling Document

SEE FEATURES SECTION

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883, Method 5005

Subgrp	Description	Temp (^{O}C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

Features

- 1.9GHz gain-bandwidth product
- 1.05nV/SqRtHz input voltage noise
- 0.8pA/SqRtHz @ Icc ≤ 5mA
- 100uV input offset voltage, 2uV/ C drift
- 350V/us slew rate
- 15mA to 5mA adjustable supply current
- Gain range ±10 to ±1,000V/V
- 0.9dB NF @ Rs = 700ohm

CONTROLLING DOCUMENT:

CLC425AJ-QML 5962-9325901MPA

Applications

- Instrumentation sense amplifiers
- Ultrasound pre-amps
- Magnetic tape & disk pre-amps
- Photo-diode transimpedance amplifiers
- Wide band active filters
- Low noise figure RF amplifiers
- Professional audio systems
- Low-noise loop filters for PLLs

(Absolute Maximum Ratings)
(Note 1)

Supply Voltage (Vs)	±7 Vdc
Output Current (Iout)	96mA
Common Mode Input Voltage (Vcm)	±Vs
Differential Input Current(Iid)	±25mA
Maximum Power Dissipation (Pd) (Note 2)	262mW
Lead Temperature (Soldering, 10 seconds)	+300 C
Junction Temperature (Tj)	+175 C
Storage Temperature Range	-65 C ≤ Ta ≤ +150 C
Thermal Resistance	
ThetaJa	
Junction-to-ambient	
Ceramic Dip	
(Still Air Flow)	TBD
(500LF/Min Air Flow)	TBD
ThetaJC	
Ceramic Dip	TBD
Package Weight (Typical)	
CERAMIC DIP	TBD
ESD Tolerance (Note 3)	
ESD Rating	1000 V

Note 1: Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated within the listed test conditions.

Note 2: The maximum power dissipation must be derated at elevated temperatures and is dictated by Tjmax (maximum junction temperature), ThetaJA (package junction to ambient thermal resistance), and TA (ambient temperature). The maximum allowable power dissipation at any temperature is Pdmax = (Tjmax - TA) / ThetaJA or the number given in the Absolute Maximum Ratings, whichever is lower.

Note 3: Human body model, 100 pF discharged through 1.5K Ohms.

Recommended Operating Conditions

Supply Voltage (Vs)	±5Vdc
Gain Range (Av)	±10 to ±1000V/V
Ambient Operating Temperature Range (TA)	-55 C ≤ Ta ≤ +125 C

Electrical Characteristics

DC PARAMETERS: Static and DC Tests

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Vs = ±5 Vdc, Av = +20, load resistance (Rl = 100 Ohms), feedback resistance (Rf) = 500 Ohms, and gain setting resistance (Rg) = 26.1 Ohms. -55 C ≤ Ta ≤ +125 C (Note 3).

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Iin	Input Bias Current				-20	20	uA	1, 2
					-40	40	uA	3
Iio	Input Offset Current		1		-2.0	+2.0	uA	1, 2
			1		-3.4	+3.4	uA	3
Vio	Input Offset Voltage				-0.8	+0.8	mV	1
					-1	+1	mV	2, 3
Tc (Iin)	Average Input Bias Current Drift		1		-120	0	nA/C	2
			1		-250	0	nA/C	3
Tc (Vio)	Average Input Offset Voltage Drift	Ta = +125 C, -55 C	1		-4	+4	uV/C	2
			1		-8	+8	uV/C	3
Tc (Iio)	Average Input Offset Current Drift	Ta = +125 C, -55 C	1		-25	+25	nA/C	2
			1		-50	+50	nA/C	3
Is	Supply Current	Rl = infinite				16	mA	1, 2
						18	mA	3
PSRR	Power Supply Rejection Ratio	+Vs = +4.0V to +5.0V, -Vs = -4.0V to -5.0V			88		dB	1
					86		dB	2
					82		dB	3
CMRR	Common Mode Rejection Ratio	Vcm = ±1V	1		92		dB	4
			1		90		dB	5
			1		88		dB	6
AOL	Open Loop Gain				86		dB	4, 5
					77		dB	6

Electrical Characteristics

AC PARAMETERS: Frequency Domain Tests

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: Vs = ±5 Vdc, Av = +20, load resistance (Rl = 100 Ohms), feedback resistance (Rf) = 500 Ohms, and gain setting resistance (Rg) = 26.1 Ohms. -55 C ≤ Ta ≤ +125 C (Note 3).

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
SSBW	Small Signal Bandwidth	-3 dB bandwidth, Vout < 0.4 Vpp			75		MHz	4
					50		MHz	5
					75		MHz	6
LSBW	Large Signal Bandwidth	-3 dB bandwidth, Vout < 5.0 Vpp	1		30		MHz	4, 6
			1		20		MHz	5
GFP	Gain Flatness Peaking Low	0.1 MHz to 30 MHz, Vout ≤ 0.4 Vpp				0.5	dB	4
						0.7	dB	5, 6
GFR	Gain Flatness Rolloff	0.1 MHz to 30 MHz, Vout ≤ 0.4 Vpp				0.5	dB	4
						0.7	dB	5, 6
Lpd	Linear Phase Deviation	0.1 MHz to 30 MHz, Vout ≤ 0.4 Vpp	1		1.5		Deg.	4, 6
			1		2.5		Deg.	5

Electrical Characteristics

AC PARAMETERS: Distortion and Noise Tests

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: Vs = ±5 Vdc, Av = +20, load resistance (Rl = 100 Ohms), feedback resistance (Rf) = 500 Ohms, and gain setting resistance (Rg) = 26.1 Ohms. -55 C ≤ Ta ≤ +125 C (Note 3).

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
HD2	2nd Harmonic Distortion	1 Vpp at 10 MHz				-48	dBc	4
						-46	dBc	5
						-48	dBc	6
HD3	3rd Harmonic Distortion	1 Vpp at 10 MHz				-65	dBc	4
						-60	dBc	5
						-65	dBc	6
SNF	Noise Floor	At 1 MHz to 100 MHz	1			-165	dBm 1Hz	4, 6
			1			-162	dBm 1Hz	5
INV	Integrated Noise	At 1 MHz to 100 MHz	1			13	uV	4
			1			18	uV	5
			1			13	uV	6
VN	Input Noise Voltage	At 1 MHz to 100 MHz	1			1.25	nV/Sq RtHz	4, 6
			1			1.8	nV/Sq RtHz	5
Icn	Input Noise Current	At 1 MHz to 100 MHz	1			2.5	pA/Sq RtHz	4, 5
			1			4.0	pA/Sq RtHz	6

AC PARAMETERS: Timing Tests

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: Vs = ±5 Vdc, Av = +20, load resistance (Rl = 100 Ohms), feedback resistance (Rf) = 500 Ohms, and gain setting resistance (Rg) = 26.1 Ohms. -55 C ≤ Ta ≤ +125 C (Note 3).

Tr, Tf	Rise and Fall Time	0.4V step	1			4.7	nS	9, 11
			1			7.0	nS	10
SR	Slew Rate	Measured ±1V with 5V step, Av = +20	1		250		V/uS	4, 6
			1		200		V/uS	5
Ts	Settling Time	2V step at 0.2% of the fixed value	1			30	nS	9, 11
			1			40	nS	10
OS	Overshoot	0.4V step	1			10	%	9
			1			12	%	10, 11

Electrical Characteristics

DC PARAMETERS: Perfomance Tests

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Vs = ±5 Vdc, Av = +20, load resistance (Rl = 100 Ohms), feedback resistance (Rf) = 500 Ohms, and gain setting resistance (Rg) = 26.1 Ohms. -55 C ≤ Ta ≤ +125 C (Note 3).

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Rinc	Common Mode Input Resistance		1		1.6		MOhm	1, 2
			1		0.6		MOhm	3
Rind	Differential Mode Input Resistance		1		3		KOhm	1, 2
			1		1		KOhm	3
Cinc	Common Mode Input Capacitance		1		3		pF	1, 2, 3
Rout	Closed Loop Output Resistance		1		10		MOhm	1, 2
			1		50		MOhm	3
Vout	Output Voltage Range	Rl = infinite	1		-3.7	+3.7	V	1, 2
			1		-3.5	+3.5	V	3
Vout Low	Output Voltage Range	Rl = 100 Ohms	1		-3.2	+3.2	V	1, 2
			1		-2.8	+2.8	V	3
CMIR	Common Mode Input Voltage Range		1		-3.5	+3.5	V	1, 2
			1		-3.4	+3.4	V	3
Iout	Output Current	Source	1		70		mA	1, 2
			1		60		mA	3
		Sink	1		55		mA	1, 2
			1		40		mA	3

DC PARAMETERS: DRIFT VALUES

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: "Deltas not required on B-Level product. Deltas required for S-Level product at Group B5 ONLY, or as specified on the Internal Processing Instructions (IPI), (Note 3).

Iin	Input Bias Current		1		-2	+2	uA	1
Vio	Input Offset Voltage		1		-0.1	0.1	mV	1
Is	Supply Current		1		-0.8	+0.8	mA	1

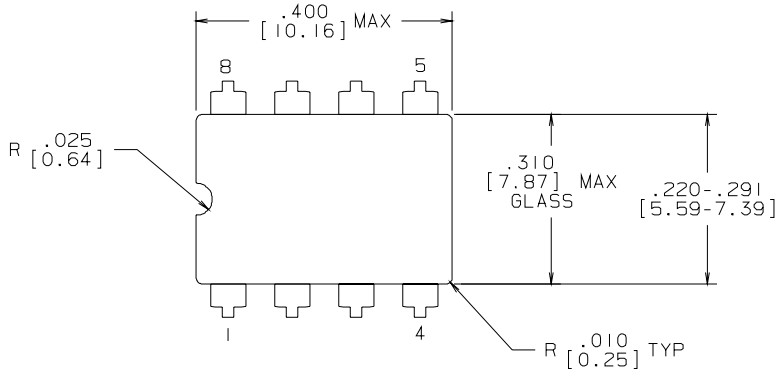
Note 1: If not tested, shall be guaranteed to the limits specified in table I herein.
Note 2: Group A testing only.
Note 3: The algebraic convention, whereby the most negative value is a minimum and most positive is a maximum, is used in this table. Negative current shall be defined as convential current flow out of a device terminal.

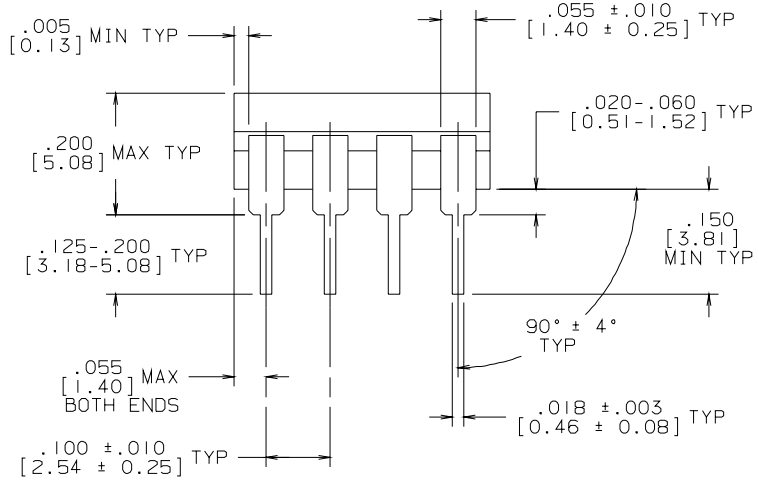
Graphics and Diagrams

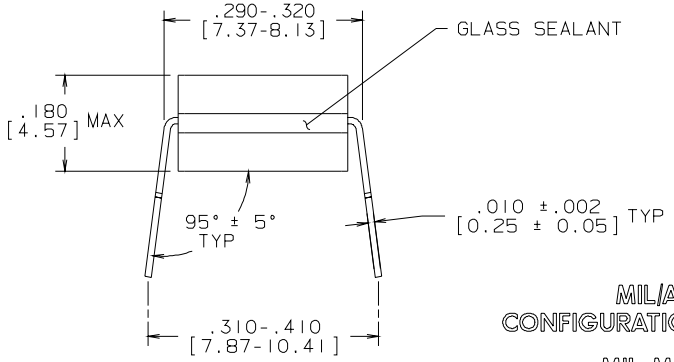
GRAPHICS#	DESCRIPTION
07089HRA2	CERDIP (J), 8 LEAD (B/I CKT)
J08ARL	CERDIP (J), 8 LEAD (P/P DWG)
P000397A	CERDIP (J), 8 LEAD (PINOUT)

See attached graphics following this page.

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
L	REVISE PER CURRENT STD; REDRAW	10002	09/21/93	TL/







MIL/AERO
CONFIGURATION CONTROL

MIL-M-38510
CONFIGURATION CONTROL

NOTES: UNLESS OTHERWISE SPECIFIED

1. LEAD FINISH TO BE 200 MICROINCHES / 5.08 MICROMETERS MINIMUM SOLDER MEASURED AT THE CREST OF THE MAJOR FLATS.
2. JEDEC REGISTRATION MO-036, VARIATION AA, DATED 04/1981.

CONTROLLING DIMENSION: INCH

APPROVALS	DATE
DRAWN T. LEQUANG	09/21/93
DFTG. CHK.	
ENGR. CHK.	
APPROVAL	

PROJECTION

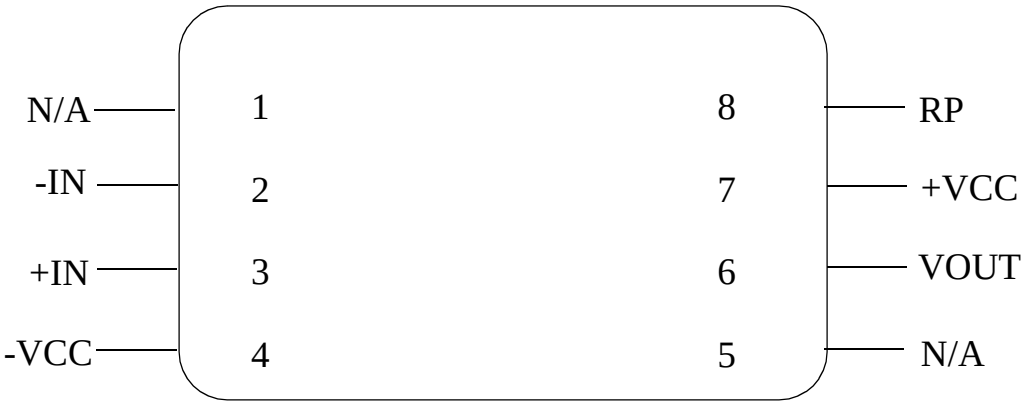
INCH
[MM]

NATIONAL SEMICONDUCTOR CORPORATION
2900 Semiconductor Drive, Santa Clara, CA 95052-8090

CERDIP (J), 8 LEAD

SCALE	SIZE	DRAWING NUMBER	REV
N/A	B	MKT-J08A	L

DO NOT SCALE DRAWING | SHEET 1 OF 1



CLC425J

8 - LEAD DIP

CONNECTION DIAGRAM

TOP VIEW

P000397A

National Semiconductor™
MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050

Revision History

Rev	ECN #	Rel Date	Originator	Changes
0A0	M0004133	08/15/03	Rose Malone	Initial MDS Release: MNCLC425A-X, Rev. 0A0. Conversion from Comlinear data sheet.
1A0	M0004261	08/15/03	Rose Malone	Update MDS: MNCLC425A-X, Rev. 0A0 to MNCLC425A-X, Rev. 1A0. Following Electrical Parameters in Drift Values Section changed for Iin from -10min % - +10max % TO -2min uA - +2max uA and for Is from -5min % - +5max % TO -0.8min uA - +0.8max uA.