

# DS90LV011A

## 3V LVDS Single High Speed Differential Driver

### General Description

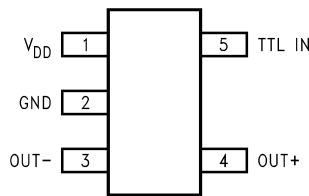
The DS90LV011A is a single LVDS driver device optimized for high data rate and low power applications. The DS90LV011A is a current mode driver allowing power dissipation to remain low even at high frequency. In addition, the short circuit fault current is also minimized. The device is designed to support data rates in excess of 400Mbps (200MHz) utilizing Low Voltage Differential Signaling (LVDS) technology.

The device is in both a 5-lead small outline transistor package and a new LLP-8 package with a 3mm x 3mm body size. The LVDS outputs have been arranged for easy PCB layout. The differential driver outputs provide low EMI with its typical low output swing of 350 mV. The DS90LV011A can be paired with its companion single line receiver, the DS90LV012A, or with any of National's LVDS receivers, to provide a high-speed LVDS interface.

### Features

- Conforms to TIA/EIA-644-A Standard
- >400Mbps (200MHz) switching rates
- 700 ps (100 ps typical) maximum differential skew
- 1.5 ns maximum propagation delay
- Single 3.3V power supply
- ±350 mV differential signaling
- Power Off Protection (outputs in TRI-STATE)
- Pinout simplifies PCB layout
- Low power dissipation (23 mW @ 3.3V typical)
- SOT-23 5-lead package
- Leadless LLP-8 package (3x3 mm body size)
- SOT-23 version pin compatible with SN65LVDS1
- Fabricated with advanced CMOS process technology
- Industrial temperature operating range (-40°C to +85°C)

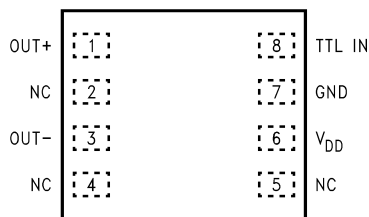
### Connection Diagrams



20014922

(Top View)

Order Number DS90LV011ATMF  
See NS Package Number MF05A

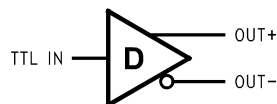


20014923

(Top View)

Order Number DS90LV011ATLD  
See NS Package Number LDA08A

### Functional Diagram



20014902

## Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ( $V_{DD}$ )	-0.3V to +4V
LVC MOS input voltage (TTL IN)	-0.3V to +3.6V
LVDS output voltage ( $OUT_{\pm}$ )	-0.3V to +3.9V
LVDS output short circuit current	24mA
Maximum Package Power Dissipation @ +25°C	
LDA Package	2.26 W
Derate LDA Package	18.1 mW/°C above +25°C
Thermal resistance ( $\theta_{JA}$ )	55.3°C/Watt
MF Package	902 mW
Derate MF Package	7.22 mW/°C above +25°C
Thermal resistance ( $\theta_{JA}$ )	138.5°C/Watt
Storage Temperature	-65°C to +150°C

Lead Temperature Range Soldering

(4 sec.)

+260°C

Maximum Junction Temperature

+150°C

ESD Ratings

HBM (1.5 k $\Omega$ , 100 pF)

≥ 9kV

EIAJ (0  $\Omega$ , 200 pF)

≥ 900V

CDM (0  $\Omega$ , 0 pF)

≥ 2000V

IEC direct (330  $\Omega$ , 150 pF)

≥ 4kV

## Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage ( $V_{DD}$ )	3.0	3.3	3.6	V
Temperature ( $T_A$ )	-40	+25	+85	°C

## Electrical Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified. (Notes 2, 3, 8)

Symbol	Parameter	Conditions	Pin	Min	Typ	Max	Units	
$ V_{OD} $	Output Differential Voltage	$R_L = 100\Omega$	OUT+, OUT-	250	350	450	mV	
$\Delta V_{OD}$	$V_{OD}$ Magnitude Change	(Figure 1 and Figure 2)				3	35	mV
$V_{OS}$	Offset Voltage	$R_L = 100\Omega$		1.125	1.22	1.375	V	
$\Delta V_{OS}$	Offset Magnitude Change	(Figure 1)		0	1	25	mV	
$I_{OFF}$	Power-off Leakage	$V_{OUT} = 3.6V$ or GND, $V_{DD} = 0V$			±1	±10	µA	
$I_{OS}$	Output Short Circuit Current (Note 4)	$V_{OUT+}$ and $V_{OUT-} = 0V$			-6	-24	mA	
$I_{OSD}$	Differential Output Short Circuit Current (Note 4)	$V_{OD} = 0V$			-5	-12	mA	
$C_{OUT}$	Output Capacitance				3		pF	
$V_{IH}$	Input High Voltage		TTL IN	2.0		$V_{DD}$	V	
$V_{IL}$	Input Low Voltage			GND		0.8	V	
$I_{IH}$	Input High Current	$V_{IN} = 3.3V$ or 2.4V				±2	±10	µA
$I_{IL}$	Input Low Current	$V_{IN} = GND$ or 0.5V				±1	±10	µA
$V_{CL}$	Input Clamp Voltage	$I_{CL} = -18$ mA			-1.5	-0.6		V
$C_{IN}$	Input Capacitance					3		pF
$I_{DD}$	Power Supply Current	No Load		$V_{IN} = V_{DD}$ or GND	$V_{DD}$		5	8
		$R_L = 100\Omega$				7	10	mA

## Switching Characteristics

Over Supply Voltage and Operating Temperature Ranges, unless otherwise specified. (Notes 3, 5, 6, 7)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$t_{PHLD}$	Differential Propagation Delay High to Low	$R_L = 100\Omega$ , $C_L = 15$ pF (Figure 3 and Figure 4)	0.3	1.0	1.5	ns
$t_{PLHD}$	Differential Propagation Delay Low to High		0.3	1.1	1.5	ns
$t_{SKD1}$	Differential Pulse Skew $ t_{PHLD} - t_{PLHD} $ (Note 9)		0	0.1	0.7	ns
$t_{SKD3}$	Differential Part to Part Skew (Note 10)		0	0.2	1.0	ns
$t_{SKD4}$	Differential Part to Part Skew (Note 11)		0	0.4	1.2	ns
$t_{TLH}$	Transition Low to High Time		0.2	0.5	1.0	ns
$t_{THL}$	Transition High to Low Time		0.2	0.5	1.0	ns
$f_{MAX}$	Maximum Operating Frequency (Note 12)		200	250		MHz

## Switching Characteristics (Continued)

**Note 1:** "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" specifies conditions of device operation.

**Note 2:** Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground except  $V_{OD}$ .

**Note 3:** All typicals are given for:  $V_{DD} = +3.3V$  and  $T_A = +25^\circ C$ .

**Note 4:** Output short circuit current ( $I_{OS}$ ) is specified as magnitude only, minus sign indicates direction only.

**Note 5:** These parameters are guaranteed by design. The limits are based on statistical analysis of the device performance over PVT (process, voltage, temperature) ranges.

**Note 6:**  $C_L$  includes probe and fixture capacitance.

**Note 7:** Generator waveform for all tests unless otherwise specified:  $f = 1\text{ MHz}$ ,  $Z_O = 50\Omega$ ,  $t_r \leq 1\text{ ns}$ ,  $t_f \leq 1\text{ ns}$  (10%-90%).

**Note 8:** The DS90LV011A is a current mode device and only function with datasheet specification when a resistive load is applied to the drivers outputs.

**Note 9:**  $t_{SKD1}$ ,  $|t_{PHLD} - t_{PLHD}|$ , is the magnitude difference in differential propagation delay time between the positive going edge and the negative going edge of the same channel.

**Note 10:**  $t_{SKD3}$ , Differential Part to Part Skew, is defined as the difference between the minimum and maximum specified differential propagation delays. This specification applies to devices at the same  $V_{DD}$  and within  $5^\circ C$  of each other within the operating temperature range.

**Note 11:**  $t_{SKD4}$ , part to part skew, is the differential channel to channel skew of any event between devices. This specification applies to devices over recommended operating temperature and voltage ranges, and across process distribution.  $t_{SKD4}$  is defined as  $I_{Max} - I_{Min}$  differential propagation delay.

**Note 12:**  $f_{MAX}$  generator input conditions:  $t_r = t_f < 1\text{ ns}$  (0% to 100%), 50% duty cycle, 0V to 3V. Output criteria: duty cycle = 45%/55%,  $V_{OD} > 250mV$ . The parameter is guaranteed by design. The limit is based on the statistical analysis of the device over the PVT range by the transitions times ( $t_{TLH}$  and  $t_{THL}$ ).

## Parameter Measurement Information

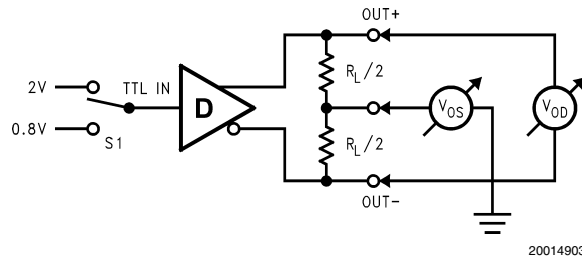


FIGURE 1. Differential Driver DC Test Circuit

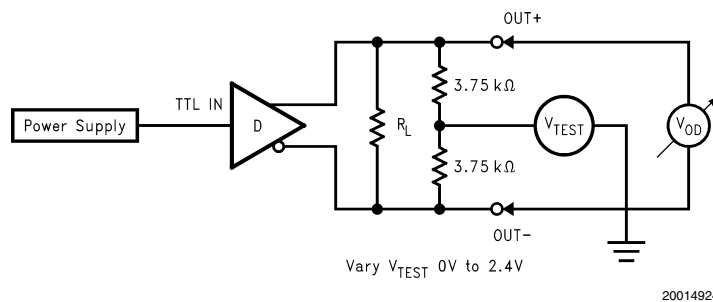


FIGURE 2. Differential Driver Full Load DC Test Circuit

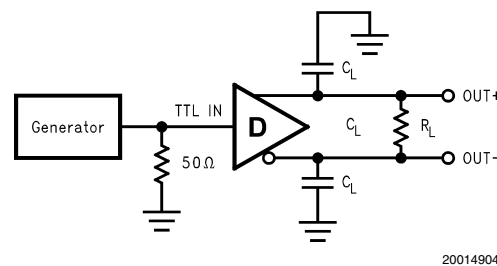


FIGURE 3. Differential Driver Propagation Delay and Transition Time Test Circuit

## Parameter Measurement Information (Continued)

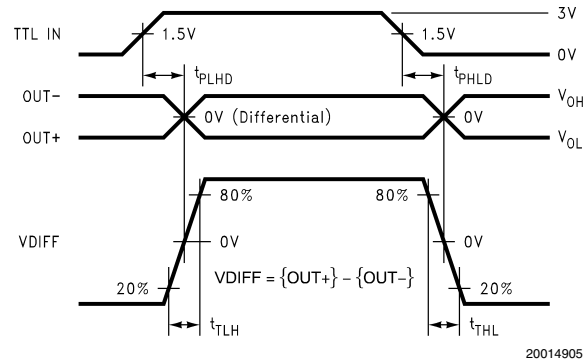


FIGURE 4. Differential Driver Propagation Delay and Transition Time Waveforms

## Application Information

TABLE 1. Device Pin Descriptions

Package Pin Number		Pin Name	Description
SOT23	LLP		
5	8	TTL IN	LVTTTL/LVCMOS driver input pins
4	1	OUT+	Non-inverting driver output pin
3	3	OUT-	Inverting driver output pin
2	7	GND	Ground pin
1	6	V <sub>DD</sub>	Power supply pin, +3.3V ± 0.3V
	2, 4, 5	NC	No connect

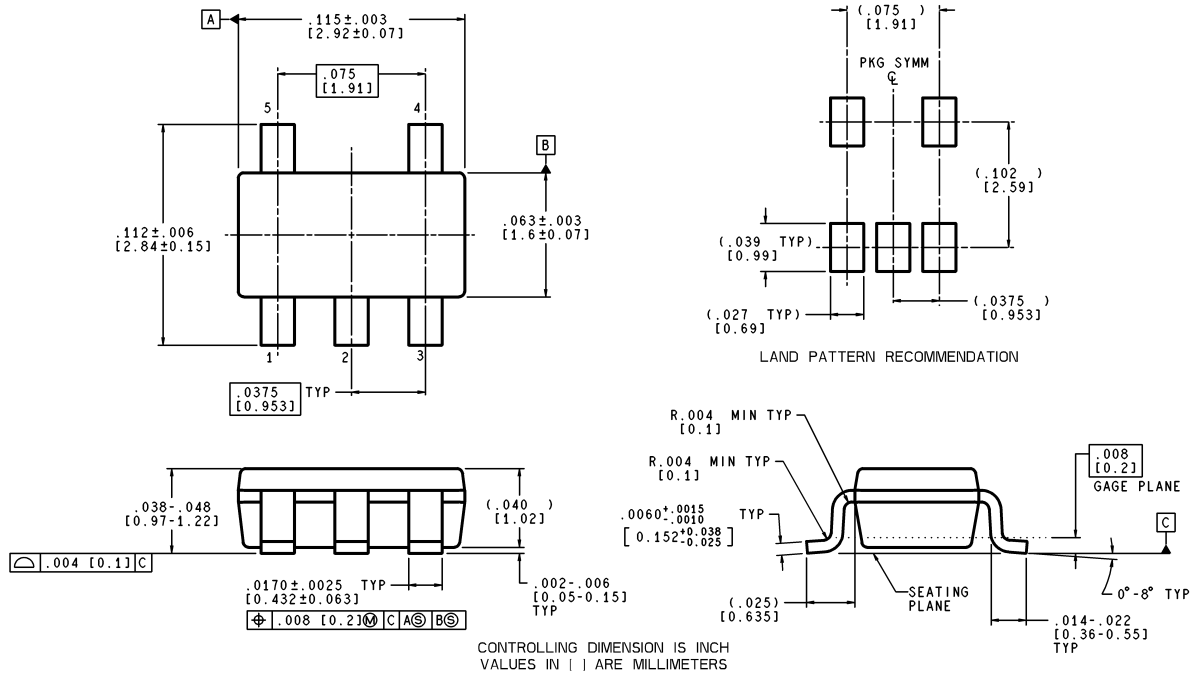
### PC Board Considerations:

For PC board considerations for the LLP package, please refer to application note AN-1187 "Leadless Leadframe Package." It is important to note that to optimize signal integrity (minimize jitter and noise coupling), the LLP thermal

land pad, which is a metal (normally copper) rectangular region located under the package, should be attached to ground and match the dimensions of the exposed pad on the PCB (1:1 ratio).

**Physical Dimensions** inches (millimeters)

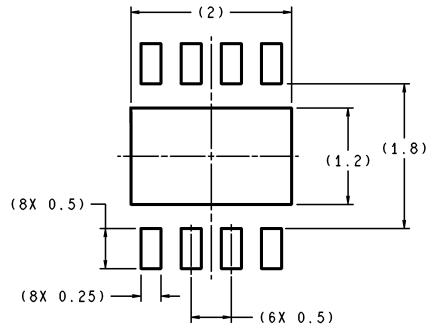
unless otherwise noted



MF05A (Rev A)

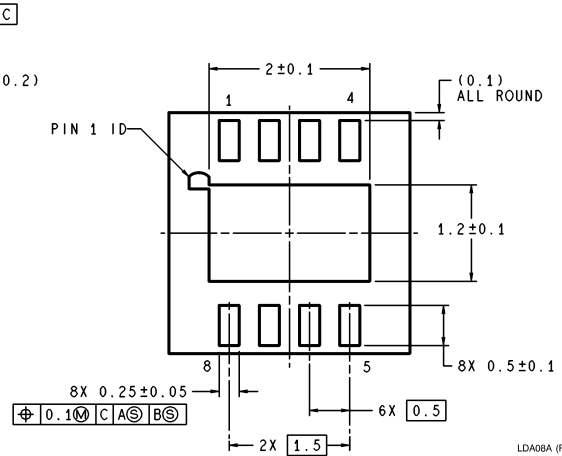
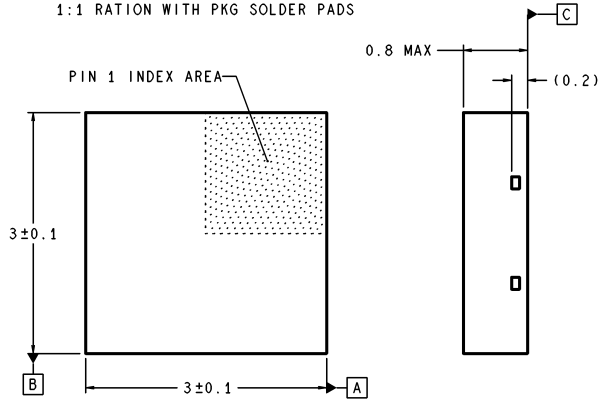
**5-Lead SOT23, JEDEC MO-178, 1.6mm  
Order Number DS90LV011ATMF  
NS Package Number MF05A**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



DIMENSIONS ARE IN MILLIMETERS

RECOMMENDED LAND PATTERN  
1:1 RATION WITH PKG SOLDER PADS



LDA08A (Rev B)

**LLP-8, 3mm x 3mm Body**  
**Order Number DS90LV011ATLD**  
**NS Package Number LDA08A**

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