National Semiconductor

February 1996

DS96176
RS-485/RS-422 Differential Bus Transceiver

General Description

The DS96176 Differential Bus Transceiver is a monolithic integrated circuit designed for bidirectional data communication on balanced multipoint bus transmission lines. The transceiver meets EIA Standard RS-485 as well as RS-422A.

The DS96176 combines a TRI-STATE® differential line driver and a differential input line receiver, both of which operate from a single 5.0V power supply. The driver and receiver have an active Enable that can be externally connected to function as a direction control. The driver differential outputs and the receiver differential inputs are internally connected to form differential input/output (I/O) bus ports that are designed to offer minimum loading to the bus whenever the driver is disabled or when $V_{CC} = 0V$. These ports feature wide positive and negative common mode voltage ranges, making the device suitable for multipoint applications in noisy environments.

The driver is designed to handle loads up to 60 mA of sink or source current. The driver features positive and negative current-limiting and thermal shutdown for protection from line fault conditions. Thermal shutdown is designed to occur at junction temperature of approximately 160°C. The receiver features a typical input impedance of 15 kΩ, an input sensitivity of ±200 mV, and a typical input hysteresis of 50 mV.

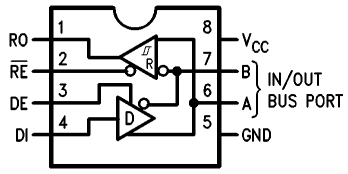
The DS96176 can be used in transmission line applications employing the DS96172 and the DS96174 quad differential line drivers and the DS96173 and DS96175 quad differential line receivers.

Features

- Bidirectional transceiver
- Meets EIA Standard RS-422A and RS-485
- Designed for multipoint transmission
- TRI-STATE driver and receiver enables
- Individual driver and receiver enables
- Wide positive and negative input/output bus voltage ranges
- Driver output capability ±60 mA Maximum
- Thermal shutdown protection
- Driver positive and Negative current-limiting
- High impedance receiver input
- Receiver input sensitivity of ±200 mV
- Receiver input hysteresis of 50 mV typical
- Operates from single 5.0V supply
- Low power requirements

Connection Diagram

8-Lead DIP



TL/F/9630–1

Top View

Order Number DS96176CJ or DS96176CN
See NS Package Number J08E or N08E

Function Table

Driver

Input	Enable	Outputs	
DI	**DE**	**A**	**B**
H	H	H	L
L	H	L	H
X	L	Z	Z

Receiver

Differential Inputs	Enable	Output
A-B	**$\overline{RE}$**	**R**
$V_{ID} \geq 0.2V$	L	H
$V_{ID} \leq -0.2V$	L	L
X	H	Z

H = High Level
L = Low Level
X = Immaterial
Z = High Impedance (off)

TRI-STATE® is a registered trademark of National Semiconductor Corporation.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature Range	
Ceramic DIP	−65°C to +175°C
Molded DIP	−65°C to +150°C
Lead Temperature	
Ceramic DIP (soldering, 60 sec.)	300°C
Molded DIP (soldering, 10 sec.)	265°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1300 mW
Molded Package	930 mW
Supply Voltage	7.0V
Differential Input Voltage	+15V/−10V
Enable Input Voltage	5.5V

*Derate cavity package 8.7 mW/°C above 25°C; derate molded DIP package 7.5 mW/°C above 25°C.

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage (V_{CC})	4.75	5.0	5.25	V
Voltage at Any Bus Terminal (Separately or Common Mode)	−7.0		12	V
Differential Input Voltage (V_{ID})			±12	V
Output Current HIGH (I_{OH})				
Driver			−60	mA
Receiver			−400	μA
Output Current LOW (I_{OL})				
Driver			60	mA
Receiver			16	mA
Operating Temperature (T_A)	0	25	70	°C

Electrical Characteristics

Over recommended temperature, common mode input voltage, and supply voltage ranges, unless otherwise specified (Notes 2 and 3)

DRIVER SECTION

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IH}	Input Voltage HIGH			2.0			V
V_{IL}	Input Voltage LOW					0.8	V
V_{OH}	Output Voltage HIGH	I_{OH} = −20 mA			3.1		V
V_{OL}	Output Voltage LOW	I_{OL} = 20 mA			0.85		V
V_{IC}	Input Clamp Voltage	I_I = −18 mA				−1.5	V
$\|V_{OD1}\|$	Differential Output Voltage	I_O = 0 mA				6.0	V
$\|V_{OD2}\|$	Differential Output Voltage	R_L = 100Ω, *Figure 1*		2.0	2.25		V
		R_L = 54Ω, *Figure 1* and *2*		1.5	2.0		
$\Delta\|V_{OD2}\|$	Change in Magnitude of Differential Output Voltage (Note 4)	R_L = 54Ω, V_{CM} = 0V *Figure 1* and *2*				±0.2	V
		R_L = 100Ω *Figure 1*					
V_{OC}	Common Mode Output Voltage (Note 5)	R_L = 54Ω or 100Ω, *Figure 1*				3.0	V
$\Delta\|V_{OC}\|$	Change in Magnitude of Common Mode Output Voltage (Note 4)					±0.2	V
I_O	Output Current (Note 4) (Includes Receiver I_I)	Output Disabled	V_O = 12V			1.0	mA
			V_O = −7.0V			−0.8	
I_{IH}	Input Current HIGH	V_I = 2.4V				20	μA
I_{IL}	Input Current LOW	V_I = 0.4V				−100	μA
I_{OS}	Short Circuit Output Current (Note 9)	V_O = −7.0V				−250	mA
		V_O = 0V				−150	
		V_O = V_{CC}				150	
		V_O = 12V				250	
I_{CC}	Supply Current	No Load	Outputs Enabled			35	mA
			Outputs Disabled			40	

Electrical Characteristics (Continued)

Over recommended temperature, common mode input voltage, and supply voltage ranges, unless otherwise specified

RECEIVER SECTION

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{TH}	Differential Input High Threshold Voltage	$V_O = 2.7V$, $I_O = -0.4$ mA				0.2	V
V_{TL}	Differential Input Low Threshold Voltage (Note 6)	$V_O = 0.5V$, $I_O = 8.0$ mA		−0.2			V
$V_{T+} - V_{T-}$	Hysteresis (Note 7)	$V_{CM} = 0V$			50		mV
V_{IH}	Enable Input Voltage HIGH			2.0			V
V_{IL}	Enable Input Voltage LOW					0.8	V
V_{IC}	Enable Input Clamp Voltage	$I_I = -18$ mA				−1.5	V
V_{OH}	Output Voltage HIGH	$V_{ID} = 200$ mV, $I_{OH} = -400$ μA, *Figure 3*		2.7			V
V_{OL}	Output Voltage LOW	$V_{ID} = -200$ mV, *Figure 3*	$I_{OL} = 8{,}0$ mA			0.45	V
			$I_{OL} = 16$ mA			0.50	
I_{OZ}	High Impedance State Output	$V_O = 0.45V$ to 2.4V				±20	μA
I_I	Line Input Current (Note 8)	Other Input = 0V	$V_I = 12V$			1.0	mA
			$V_I = -7.0V$			0.8	
I_{IH}	Enable Input Current HIGH	$V_{IH} = 2.7V$				20	μA
I_{IL}	Enable Input Current LOW	$V_{IL} = 0.4V$				−100	μA
R_I	Input Resistance				12		kΩ
I_{OS}	Short Circuit Output Current	(Note 9)		−15		−85	mA
I_{CC}	Supply Current (Total Package)	No Load	Outputs Enabled			40	mA
			Outputs Disabled				

Driver Switching Characteristics $V_{CC} = 5V$, $T_A = 25°C$

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{DD}	Differential Output Delay Time	$R_L = 60\Omega$, *Figure 4*		15	25	ns
t_{TD}	Differential Output Transition Time	$R_L = 60\Omega$, *Figure 4*		15	25	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	$R_L = 27\Omega$, *Figure 5*		12	20	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	$R_L = 27\Omega$, *Figure 5*		12	20	ns
t_{PZH}	Output Enable Time to High Level	$R_L = 110\Omega$, *Figure 6*		25	35	ns
t_{PZL}	Output Enable Time to Low Level	$R_L = 110\Omega$, *Figure 7*		25	35	ns
t_{PHZ}	Output Disable Time from High Level	$R_L = 110\Omega$, *Figure 6*		20	25	ns
t_{PLZ}	Output Disable Time from Low Level	$R_L = 110\Omega$, *Figure 7*		29	35	ns

Receiver Switching Characteristics $V_{CC} = 5.0V, T_A = 25°C$

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	V_{ID} = 0V to 3.0V, C_L = 15 pF, *Figure 8*		16	25	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output			16	25	ns
t_{PZH}	Output Enable Time to High Level	C_L = 15 pF, *Figure 9*		15	22	ns
t_{PZL}	Output Enable Time to Low Level			15	22	ns
t_{PHZ}	Output Disable Time from High Level	C_L = 5.0 pF, *Figure 9*		14	30	ns
t_{PLZ}	Output Disable Time from Low Level			24	40	ns

Note 1: ''Absolute Maximum Ratings'' are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of ''Electrical Characteristics'' provide conditions for actual operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C range for the DS96176. All typicals are given for V_{CC} = 5V and T_A = 25°C.

Note 3: All currents into the device pins are positive; all currents out of the device pins are negative. All voltages are referenced to ground unless otherwise specified.

Note 4: $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.

Note 5: In EIA Standards RS-422A and RS-485, V_{OC}, which is the average of the two output voltages with respect to ground, is called output offset voltage, V_{OS}.

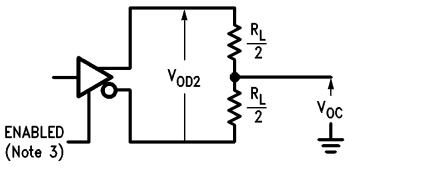
Note 6: The algebraic convention, where the less positive (more negative) limit is designated minimum, is used in this data sheet for common mode input voltage and threshold voltage levels only.

Note 7: Hysteresis is the difference between the positive-going input threshold voltage V_{T+}, and the negative-going input threshold voltage, V_{T-}.

Note 8: Refer to EIA Standard RS-485 for exact conditions.

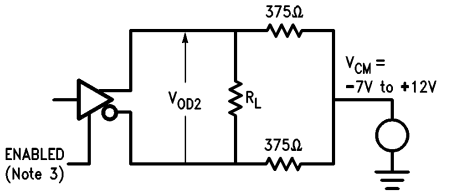
Note 9: Only one output at a time should be shorted.

Parameter Measurement Information



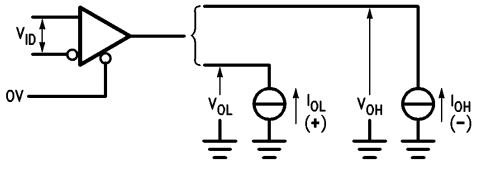
TL/F/9630–2

FIGURE 1. Driver V_{OD} and V_{OC}



TL/F/9630–3

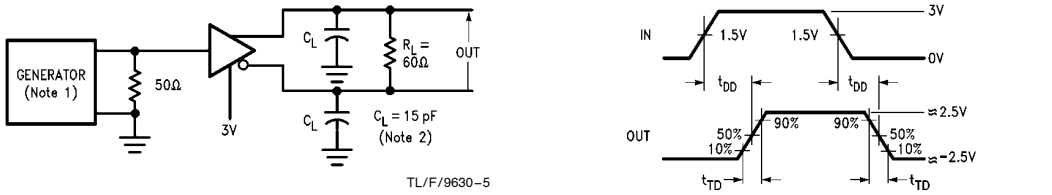
FIGURE 2. Driver V_{OD} with Varying Common Mode Voltage



TL/F/9630–4

FIGURE 3. Receiver V_{OH} and V_{OL}

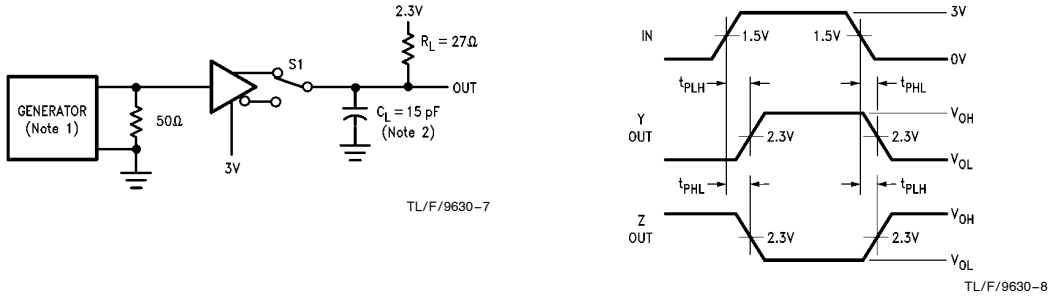
Parameter Measurement Information (Continued)



TL/F/9630–5

TL/F/9630–6

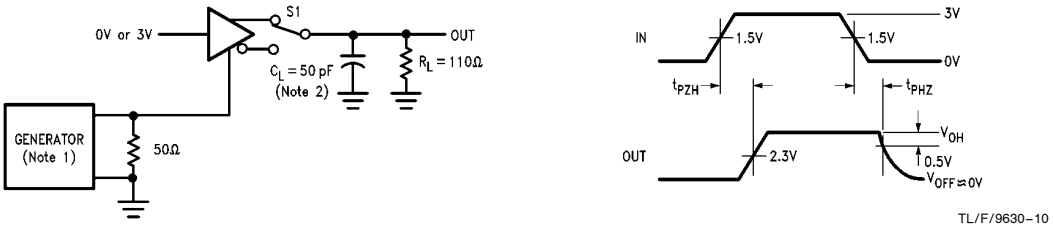
FIGURE 4. Driver Differential Output Delay and Transition Times



TL/F/9630–7

TL/F/9630–8

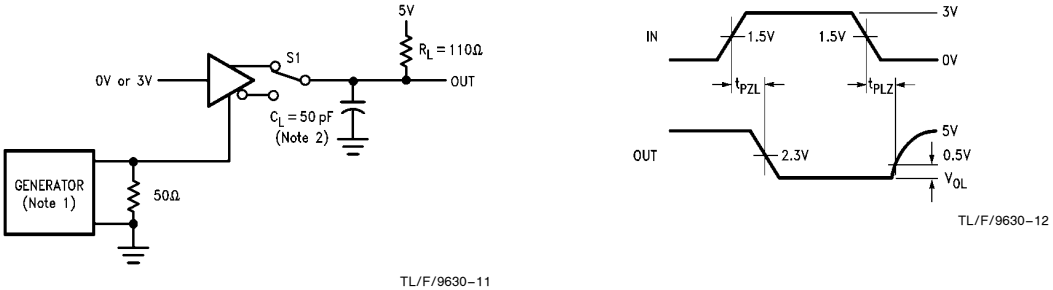
FIGURE 5. Driver Propagation Times



TL/F/9630–9

TL/F/9630–10

FIGURE 6. Driver Enable and Disable Times (t_{PZH}, t_{PHZ})

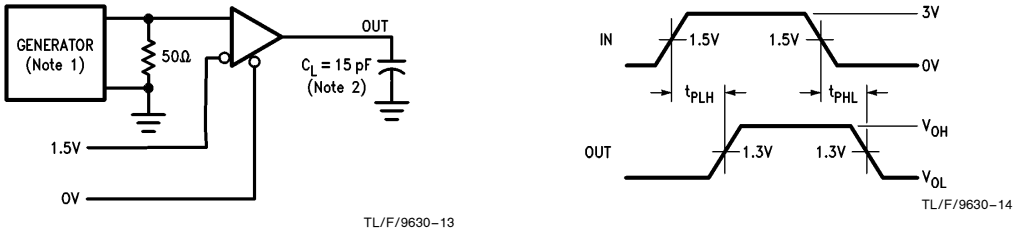


TL/F/9630–11

TL/F/9630–12

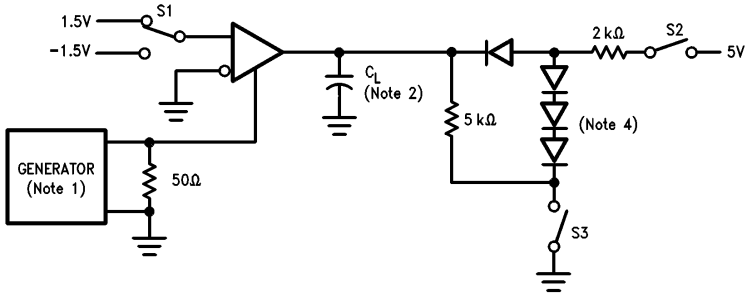
FIGURE 7. Driver Enable and Disable Times (t_{PZL}, t_{PLZ})

Parameter Measurement Information (Continued)

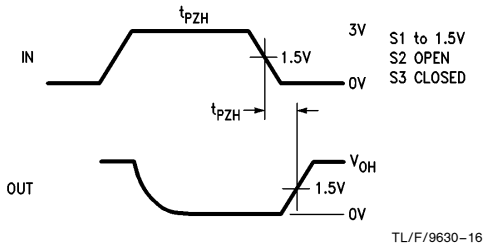


TL/F/9630–13 TL/F/9630–14

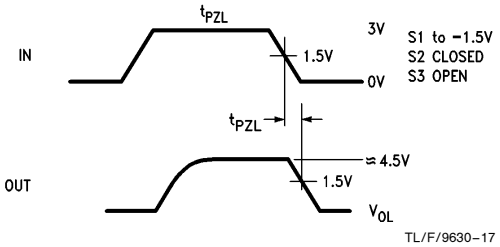
FIGURE 8. Receiver Propagation Delay Times



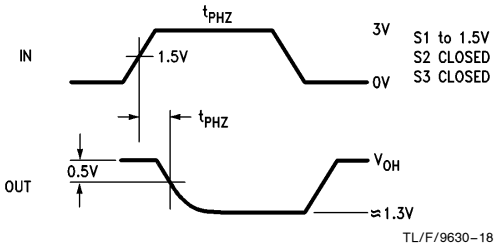
TL/F/9630–15



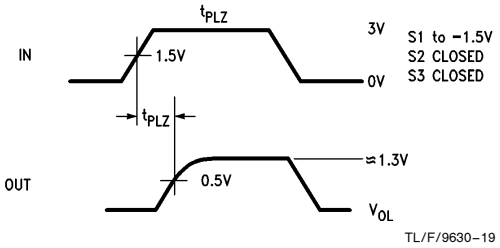
TL/F/9630–16



TL/F/9630–17



TL/F/9630–18



TL/F/9630–19

FIGURE 9. Receiver Enable and Disable Times

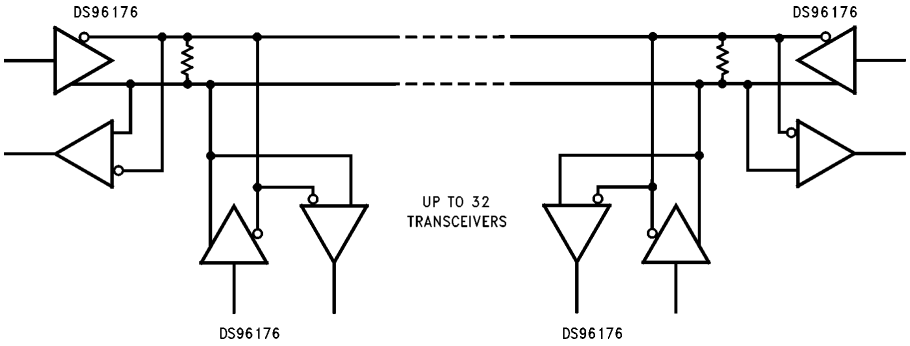
Note 1: The input pulse is supplied by a generator having the following characteristics: PRR = 1.0 MHz, 50% duty cycle, $t_r \leq 6.0$ ns, $Z_O = 50\Omega$.

Note 2: C_L includes probe and stray capacitance.

Note 3: DS96176 Driver enable is Active-High.

Note 4: All diodes are 1N916 or equivalent.

Typical Application



TL/F/9630–20

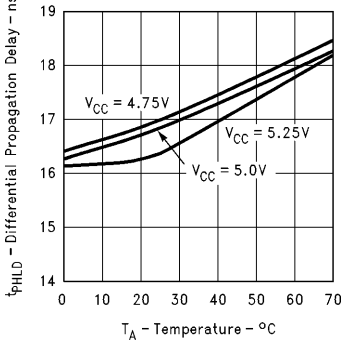
FIGURE 10

Note:

The line length should be terminated at both ends of its characteristic impedance.
Stub lengths off the main line should be kept as short as possible.

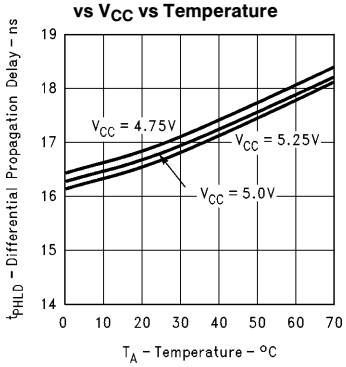
Typical Performance Characteristics

Driver Differential Propagation Delay vs V_{CC} vs Temperature



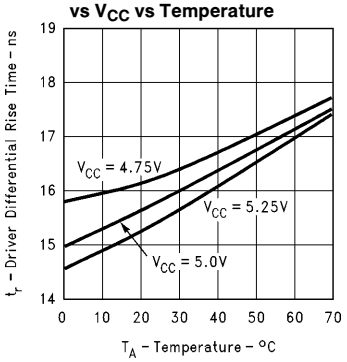
TL/F/9630–22

Driver Differential Propagation Delay vs V_{CC} vs Temperature



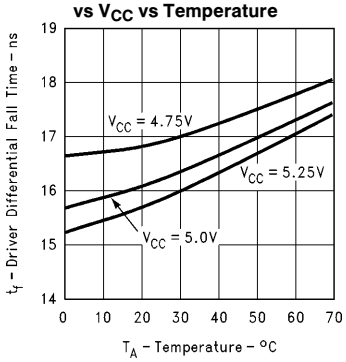
TL/F/9630–23

Driver Differential Rise Time vs V_{CC} vs Temperature



TL/F/9630–24

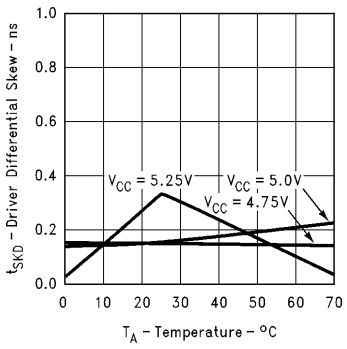
Driver Differential Fall Time vs V_{CC} vs Temperature



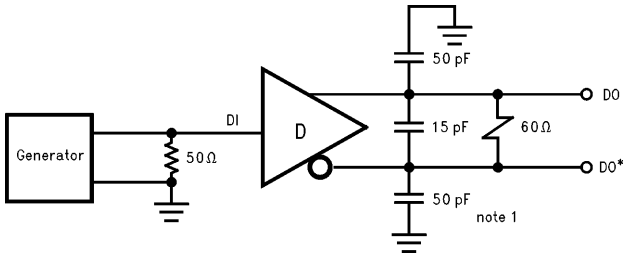
TL/F/9630–25

Typical Performance Characteristics (Continued)

Driver Skew vs V_{CC} vs Temperature ($|t_{PLDH}-t_{PHLD}|$)

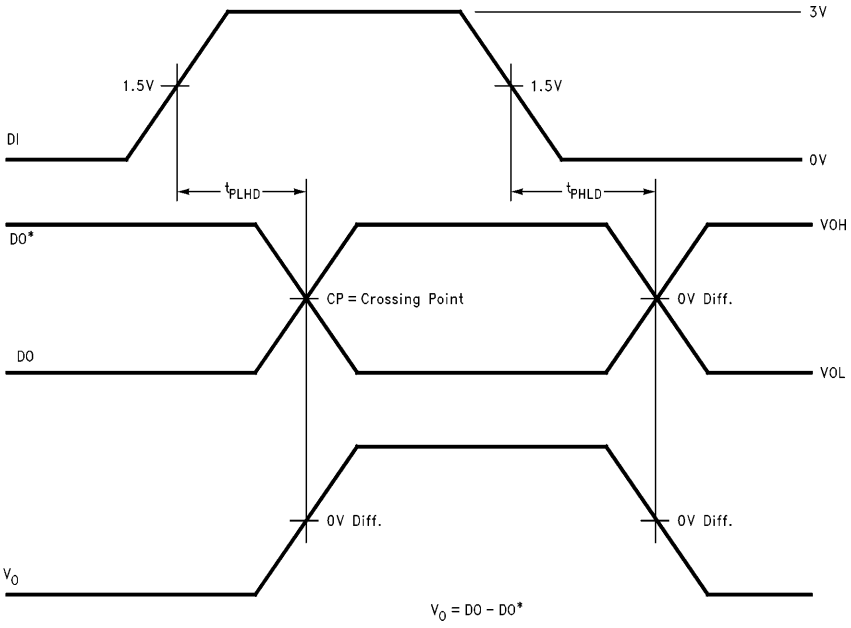


TL/F/9630–26



TL/F/9630–27

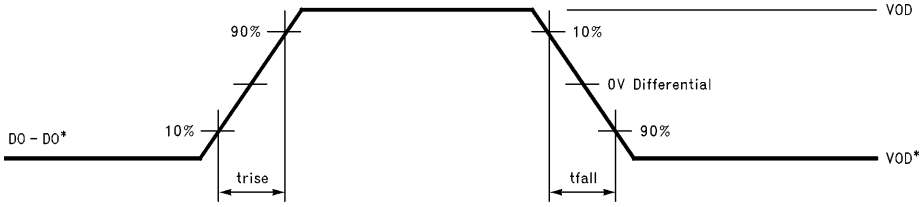
FIGURE 11. Typical Curve Driver Propagation Delay Test Circuit



TL/F/9630–28

FIGURE 12. Typical Curve Driver Differential Propagation Delay Timing

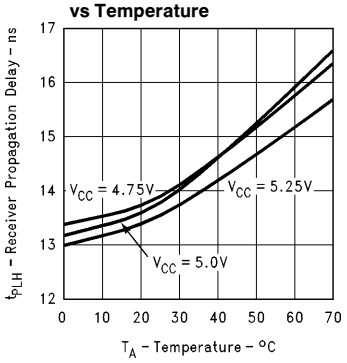
Typical Performance Curves



TL/F/9630–29

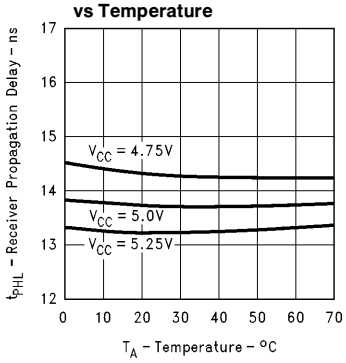
FIGURE 13. Typical Curve Driver Differential Rise and Fall Times

Receiver Propagation Delay vs V_{CC} vs Temperature



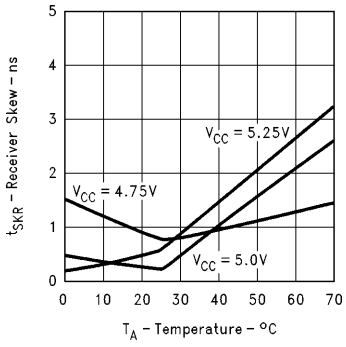
TL/F/9630–30

Receiver Propagation Delay vs V_{CC} vs Temperature



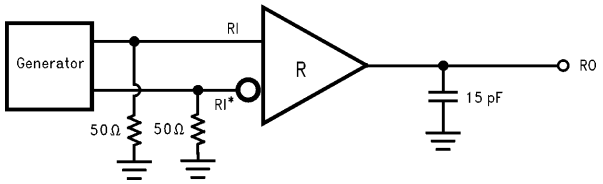
TL/F/9630–31

Receiver Skew vs V_{CC} vs Temperature ($|t_{PLH}-t_{PHL}|$)



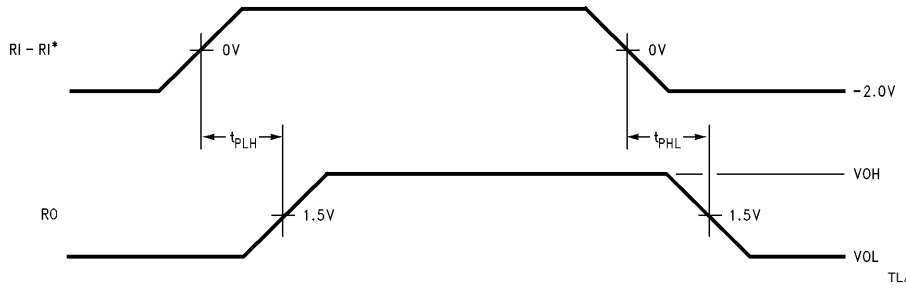
TL/F/9630–32

Typical Performance Curves (Continued)



TL/F/9630–33

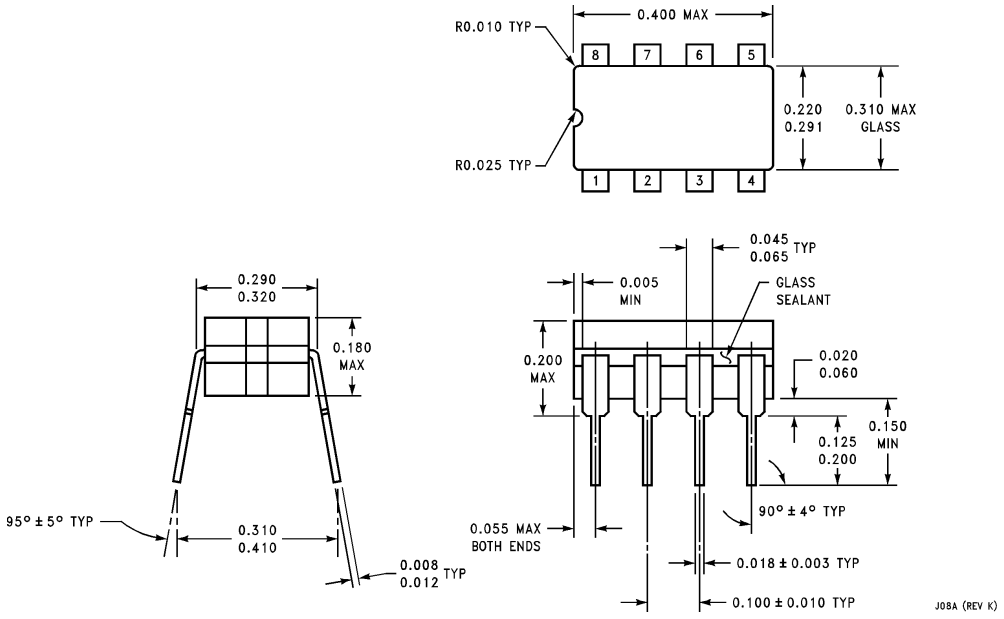
FIGURE 14. Typical Curve Receiver Differential Propagation Delay Test Circuit



TL/F/9630–34

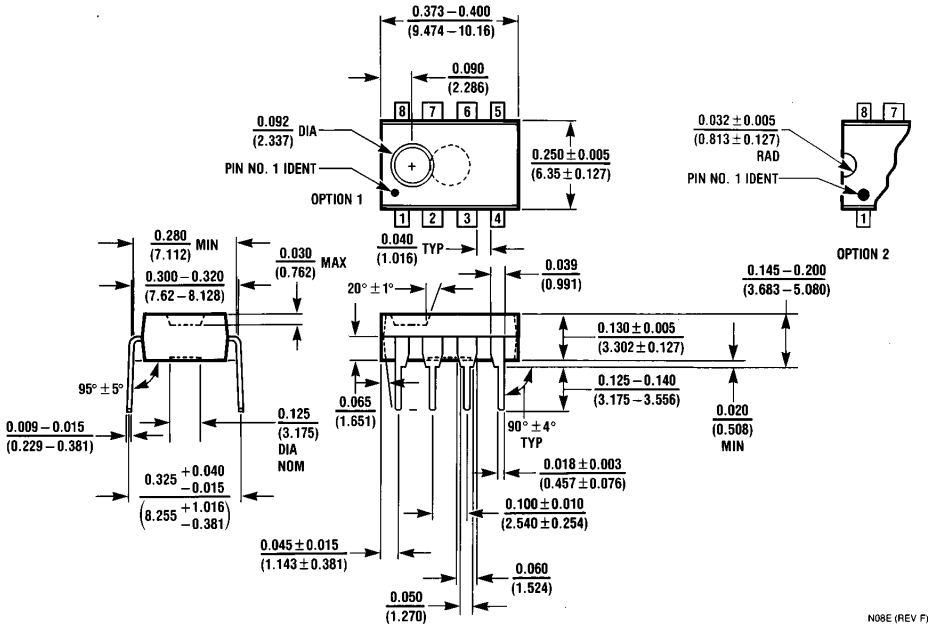
FIGURE 15. Typical Curve Receiver Propagation Delay Timing

Physical Dimensions inches (millimeters)



Ceramic Dual-In-Line Package (J)
Order Number DS96176CJ
NS Package Number J08A

Physical Dimensions inches (millimeters) (Continued)



Molded Dual-In-Line Package (N)
Order Number DS96176CN
NS Package Number N08E

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

National Semiconductor Corporation
1111 West Bardin Road
Arlington, TX 76017
Tel: 1(800) 272-9959
Fax: 1(800) 737-7018

http://www.national.com

National Semiconductor Europe
Fax: +49 (0) 180-530 85 86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 180-530 85 85
English Tel: +49 (0) 180-532 78 32
Français Tel: +49 (0) 180-532 93 58
Italiano Tel: +49 (0) 180-534 16 80

National Semiconductor Hong Kong Ltd.
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 2737-1600
Fax: (852) 2736-9960

National Semiconductor Japan Ltd.
Tel: 81-043-299-2308
Fax: 81-043-299-2408