

F100151 Hex D Flip-Flop

General Description

The F100151 contains six D-type edge-triggered, master/slave flip-flops with true and complement outputs, a pair of common Clock inputs (CP_a and CP_b) and common Master Reset (MR) input. Data enters a master when both CP_a and CP_b are LOW and transfers to the slave when CP_a and CP_b (or both) go HIGH. The MR input overrides all other inputs

and makes the Q outputs LOW. All inputs have 50 k Ω pull-down resistors.

Refer to the F100351 datasheet for:

PCC packaging

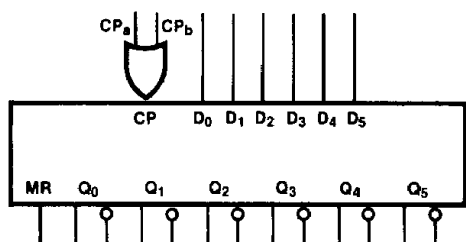
Lower power

Military versions

Extended voltage specs (–4.2V to –5.7V)

Ordering Code: See Section 8

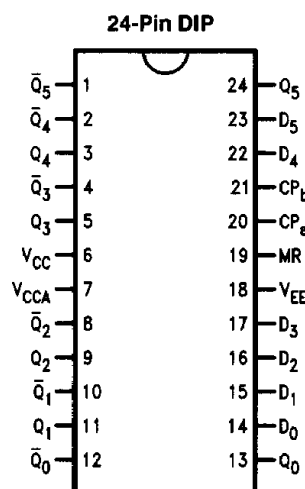
Logic Symbol



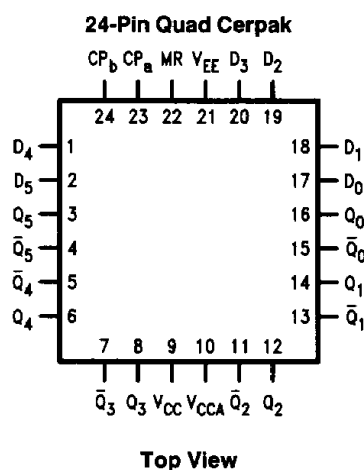
TL/F/9859-3

Pin Names	Description
D_0 – D_5	Data Inputs
CP_a , CP_b	Common Clock Inputs
MR	Asynchronous Master Reset Input
Q_0 – Q_5	Data Outputs
$\bar{Q}_0$ – $\bar{Q}_5$	Complementary Data Outputs

Connection Diagrams

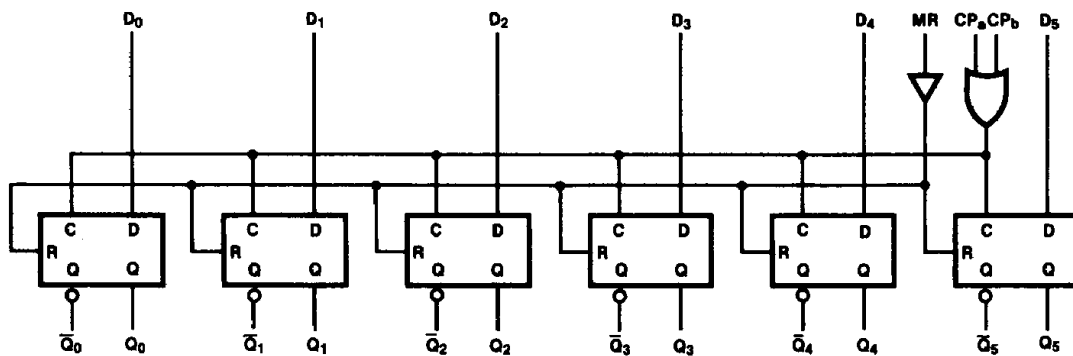


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Logic Diagram



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Truth Table (Each Flip-flop)

Synchronous Operation

Inputs				Outputs
D_n	CP_a	CP_b	MR	$Q_n(t+1)$
L	↗	L	L	L
H	↗	L	L	H
L	L	↗	L	L
H	L	↗	L	H
X	H	↗	L	$Q_n(t)$
X	↗	H	L	$Q_n(t)$
X	L	L	L	$Q_n(t)$

Asynchronous Operation

Inputs				Outputs
D_n	CP_a	CP_b	MR	$Q_n(t+1)$
X	X	X	H	L

H = HIGH Voltage Level

L = LOW Voltage Level

X = Don't Care

t = Time before CP positive transition

t+1 = Time after CP positive transition

↗ = LOW-to-HIGH transition

Absolute Maximum Ratings

Above which the useful life may be impaired. (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature -65°C to $+150^{\circ}\text{C}$

Maximum Junction Temperature (T_J) $+150^{\circ}\text{C}$

Case Temperature under Bias (T_C) 0°C to $+85^{\circ}\text{C}$

V_{EE} Pin Potential to Ground Pin -7.0V to $+0.5\text{V}$

Input Voltage (DC) V_{EE} to $+0.5\text{V}$

Output Current (DC Output HIGH) -50 mA

Operating Range (Note 2) -5.7V to -4.2V

DC Electrical Characteristics

$V_{EE} = -4.5\text{V}$, $V_{CC} = V_{CCA} = \text{GND}$, $T_C = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V _{OH}	Output HIGH Voltage	−1025	−955	−880	mV	V _{IN} = V _{IH} (Max) or V _{IL} (Min)	Loading with 50Ω to −2.0V
V _{OL}	Output LOW Voltage	−1810	−1705	−1620			
V _{OHC}	Output HIGH Voltage	−1035			mV	V _{IN} = V _{IH} (Min) or V _{IL} (Max)	Loading with 50Ω to −2.0V
V _{OLC}	Output LOW Voltage			−1610			
V _{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V _{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I _{IL}	Input LOW Current	0.50			μA	V _{IN} = V _{IL} (Min)	

DC Electrical Characteristics

$V_{EE} = -4.2\text{V}$, $V_{CC} = V_{CCA} = \text{GND}$, $T_C = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V _{OH}	Output HIGH Voltage	−1020		−870	mV	V _{IN} = V _{IH} (Max) or V _{IL} (Min)	Loading with 50Ω to −2.0V
V _{OL}	Output LOW Voltage	−1810		−1605			
V _{OHC}	Output HIGH Voltage	−1030			mV	V _{IN} = V _{IH} (Min) or V _{IL} (Max)	Loading with 50Ω to −2.0V
V _{OLC}	Output LOW Voltage			−1595			
V _{IH}	Input HIGH Voltage	−1150		−870	mV	Guaranteed HIGH Signal for All Inputs	
V _{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I _{IL}	Input LOW Current	0.50			μA	V _{IN} = V _{IL} (Min)	

DC Electrical Characteristics

$V_{EE} = -4.8\text{V}$, $V_{CC} = V_{CCA} = \text{GND}$, $T_C = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V _{OH}	Output HIGH Voltage	−1035		−880	mV	V _{IN} = V _{IH} (Max) or V _{IL} (Min)	Loading with 50Ω to −2.0V
V _{OL}	Output LOW Voltage	−1830		−1620			
V _{OHC}	Output HIGH Voltage	−1045			mV	V _{IN} = V _{IH} (Min) or V _{IL} (Max)	Loading with 50Ω to −2.0V
V _{OLC}	Output LOW Voltage			−1610			
V _{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V _{IL}	Input LOW Voltage	−1830		−1490	mV	Guaranteed LOW Signal for All Inputs	
I _{IL}	Input LOW Current	0.50			μA	V _{IN} = V _{IL} (Min)	

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Parametric values specified at -4.2V to -4.8V .

Note 3: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 4: Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DC Electrical Characteristics
 $V_{EE} = -4.2V$ to $-4.8V$ unless otherwise specified, $V_{CC} = V_{CCA} = GND$, $T_C = 0^\circ C$ to $+85^\circ C$

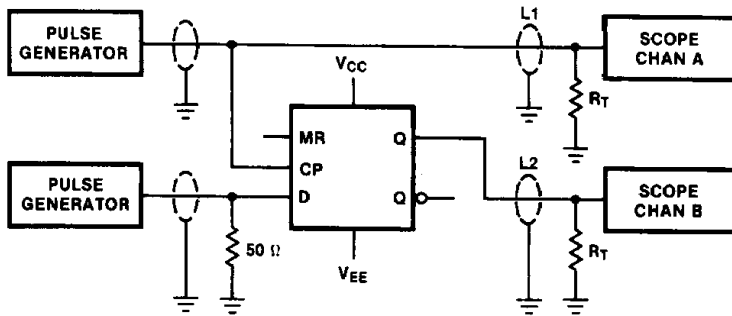
Symbol	Parameter	Min	Typ	Max	Units	Conditions
I_{IH}	Input HIGH Current MR D_0-D_5 CP_a, CP_b			450 225 520	μA	$V_{IN} = V_{IH} (Max)$
I_{EE}	Power Supply Current	-210	-155	-98	mA	Inputs Open

Ceramic Dual-In-Line Package AC Electrical Characteristics
 $V_{EE} = -4.2V$ to $-4.8V$, $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_C = 0^\circ C$		$T_C = +25^\circ C$		$T_C = +85^\circ C$		Units	Conditions
		Min	Max	Min	Max	Min	Max		
f_{max}	Toggle Frequency	375		375		375		MHz	Figures 2 and 3
t_{PLH} t_{PHL}	Propagation Delay CP_a, CP_b to Output	0.80	2.20	0.80	2.20	0.90	2.40	ns	Figures 1 and 3
t_{PLH} t_{PHL}	Propagation Delay MR to Output	1.20	2.90	1.30	3.00	1.20	3.10	ns	Figures 1 and 4
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.80	0.45	1.70	0.45	1.80	ns	Figures 1 and 3
t_s	Setup Time D_0-D_5 MR (Release Time)	0.70		0.70		0.70		ns	Figure 5
		2.30		2.30		2.60			Figure 4
t_h	Hold Time D_0-D_5	0.70		0.70		0.70		ns	Figure 5
$t_{pw(H)}$	Pulse Width HIGH CP_a, CP_b, MR	2.00		2.00		2.00		ns	Figures 3 and 4

Cerpak AC Electrical Characteristics
 $V_{EE} = -4.2V$ to $-4.8V$, $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_C = 0^\circ C$		$T_C = +25^\circ C$		$T_C = +85^\circ C$		Units	Conditions
		Min	Max	Min	Max	Min	Max		
f_{max}	Toggle Frequency	375		375		375		MHz	Figures 2 and 3
t_{PLH} t_{PHL}	Propagation Delay CP_a, CP_b to Output	0.80	2.00	0.80	2.00	0.90	2.20	ns	Figures 1 and 3
t_{PLH} t_{PHL}	Propagation Delay MR to Output	1.20	2.70	1.30	2.80	1.20	2.90	ns	Figures 1 and 4
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.70	0.45	1.60	0.45	1.70	ns	Figures 1 and 3
t_s	Setup Time D_0-D_5 MR (Release Time)	0.60		0.60		0.60		ns	Figure 5
		2.20		2.20		2.50			Figure 4
t_h	Hold Time D_0-D_5	0.60		0.60		0.60		ns	Figure 5
$t_{pw(H)}$	Pulse Width HIGH CP_a, CP_b, MR	2.00		2.00		2.00		ns	Figures 3 and 4

**Notes:**

$V_{CC}, V_{CCA} = +2V, V_{EE} = -2.5V$

$L1$ and $L2$ = equal length 50Ω impedance lines

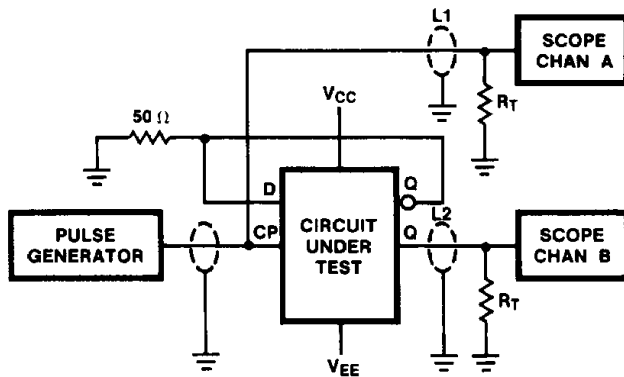
$R_T = 50\Omega$ terminator internal to scope

Decoupling $0.1 \mu F$ from GND to V_{CC} and V_{EE}

All unused outputs are loaded with 50Ω to GND

C_L = Fixture and stray capacitance ≤ 3 pF

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FIGURE 1. AC Test Circuit**Notes:**

$V_{CC}, V_{CCA} = +2V, V_{EE} = -2.5V$

$L1$ and $L2$ = equal length 50Ω impedance lines

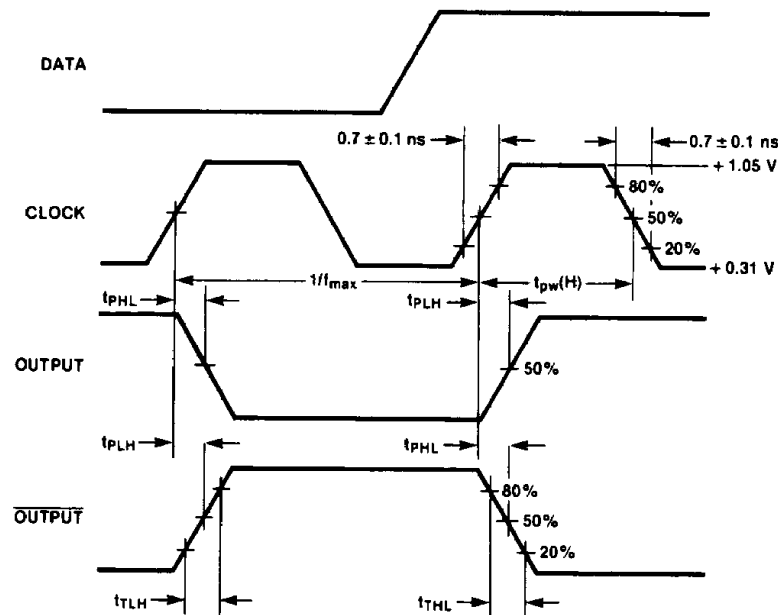
$R_T = 50\Omega$ terminator internal to scope

Decoupling $0.1 \mu F$ from GND to V_{CC} and V_{EE}

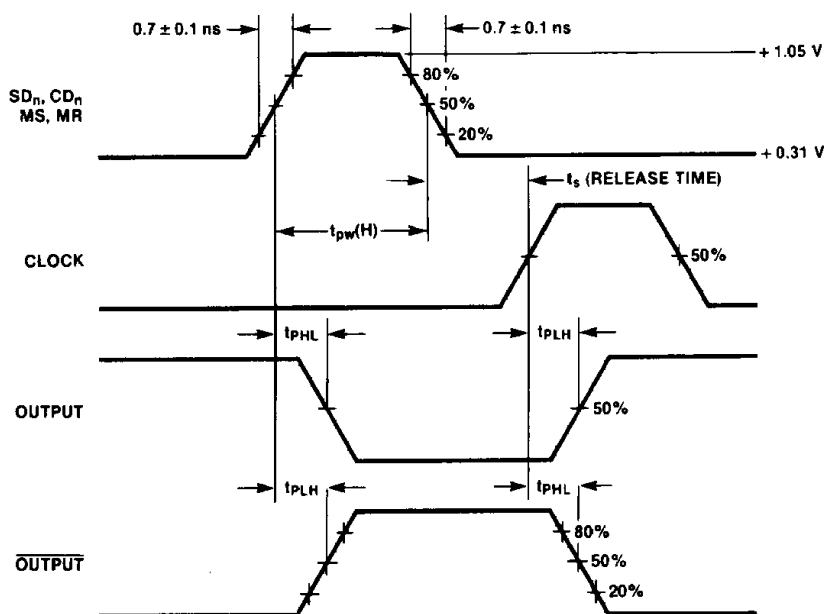
All unused outputs are loaded with 50Ω to GND

C_L = Jig and stray capacitance ≤ 3 pF

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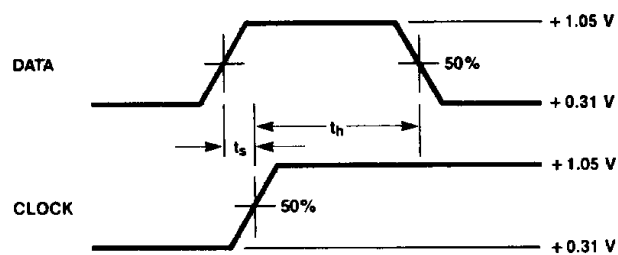
FIGURE 2. Toggle Frequency Test Circuit**FIGURE 3. Propagation Delay (Clock) and Transition Times**

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FIGURE 4. Propagation Delay (Reset)



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Notes:

t_s is the minimum time before the transition of the clock that information must be present at the data input.

t_h is the minimum time after the transition of the clock that information must remain unchanged at the data input.

FIGURE 5. Setup and Hold Time