National Semiconductor

F100156
Mask-Merge/Latch

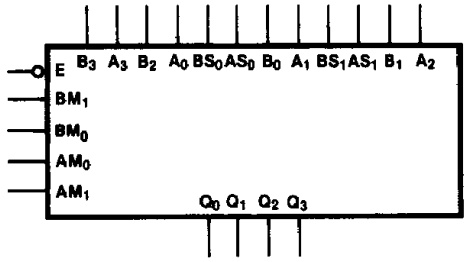
General Description

The F100156 merges two 4-bit words to form a 4-bit output word. The AM_n enable allows the merge of A into B by one, two or three places (per the AS_n value) from the left. The BM_n enable similarly allows the merge of B into A from the left (per the BS_n value). The B merge overrides the A merge when both are enabled. This means A first merges into B and B then merges into the A merge. If the B address is equal to or greater than the A address, then outputs are forced to B.

The merge outputs feed four latches, which have a common enable ($\overline{E}$) input. All inputs have a 50 kΩ (typical) pull-down resistor tied to V_{EE}.

Ordering Code: See Section 8

Logic Symbol



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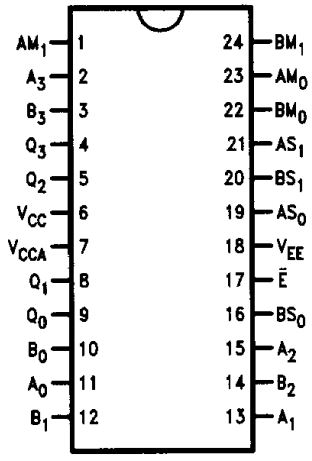
Pin Names	Description
$\overline{E}$	Latch Enable Input (Active LOW)
A_0–A_3	A Data Inputs
B_0–B_3	B Data Inputs
AM_0, AM_1	A Merge Enable Inputs
BM_0, BM_1	B Merge Enable Inputs
AS_0, AS_1	A Address Inputs
BS_0, BS_1	B Address Inputs
Q_0–Q_3	Data Outputs

Note:
When $\overline{E}$ is HIGH, Q_n outputs do not change.
When $\overline{E}$ is LOW, Q_n = A or B depending on which is selected.

Connection Diagrams

24-Pin DIP



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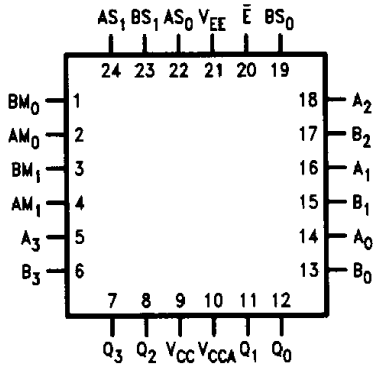
24-Pin Quad Cerpak



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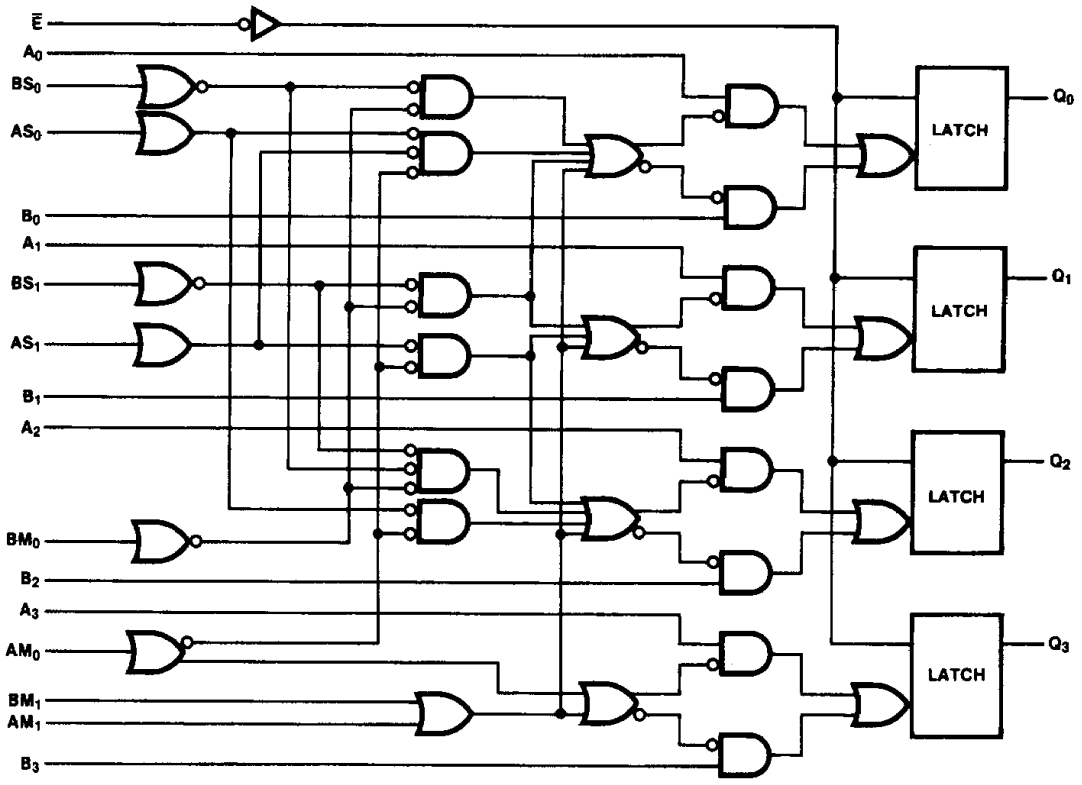
Logic Diagram



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Truth Table

Inputs									Outputs				Remarks
Merge Enables				Addresses									
BM_1	BM_0	AM_1	AM_0	BS_1	BS_0	AS_1	AS_0	$\overline{E}$	Q_0	Q_1	Q_2	Q_3	
X	X	H	X	X	X	X	X	L	B_0	B_1	B_2	B_3	Select B
H	X	X	X	X	X	X	X	L	B_0	B_1	B_2	B_3	
L	L	L	L	X	X	X	X	L	A_0	A_1	A_2	A_3	Select A
L	L	L	H	X	X	L	L	L	B_0	B_1	B_2	B_3	Merge A → B
L	L	L	H	X	X	L	H	L	A_0	B_1	B_2	B_3	
L	L	L	H	X	X	H	L	L	A_0	A_1	B_2	B_3	
L	L	L	H	X	X	H	H	L	A_0	A_1	A_2	B_3	
L	H	L	L	L	L	X	X	L	A_0	A_1	A_2	A_3	Merge B → A
L	H	L	L	L	H	X	X	L	B_0	A_1	A_2	A_3	
L	H	L	L	H	L	X	X	L	B_0	B_1	A_2	A_3	
L	H	L	L	H	H	X	X	L	B_0	B_1	B_2	A_3	
L	H	L	H	L	L	L	H	L	A_0	B_1	B_2	B_3	Merge A → B
L	H	L	H	L	L	H	L	L	A_0	A_1	B_2	B_3	
L	H	L	H	L	L	H	H	L	A_0	A_1	A_2	B_3	
L	H	L	H	L	H	H	L	L	B_0	A_1	B_2	B_3	Merge A → B then Merge B → A
L	H	L	H	L	H	H	H	L	B_0	A_1	A_2	B_3	
L	H	L	H	H	L	H	H	L	B_0	B_1	A_2	B_3	
L	H	L	H	H	H	H	H	L	B_0	B_1	B_2	B_3	B Address ≥ A Address
L	H	L	H	H	H	H	L	L	B_0	B_1	B_2	B_3	
L	H	L	H	H	H	L	H	L	B_0	B_1	B_2	B_3	
L	H	L	H	H	H	L	L	L	B_0	B_1	B_2	B_3	
L	H	L	H	H	L	H	L	L	B_0	B_1	B_2	B_3	
L	H	L	H	H	L	L	H	L	B_0	B_1	B_2	B_3	
L	H	L	H	H	L	L	L	L	B_0	B_1	B_2	B_3	
L	H	L	H	L	H	L	H	L	B_0	B_1	B_2	B_3	
L	H	L	H	L	H	L	L	L	B_0	B_1	B_2	B_3	
L	H	L	H	L	L	L	L	L	B_0	B_1	B_2	B_3	
X	X	X	X	X	X	X	X	H	Q_0	Q_1	Q_2	Q_3	Latch

Before Start	At Start	After End	At End

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

Absolute Maximum Ratings

Above which the useful life may be impaired. (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Maximum Junction Temperature (T_J)	+150°C
Case Temperature under Bias (T_C)	0°C to +85°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current (DC Output HIGH)	−50 mA
Operating Range (Note 2)	−5.7V to −4.2V

DC Electrical Characteristics

V_{EE} = −4.5V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1025	−955	−880	mV	V_{IN} = V_{IH} (Max) or V_{IL} (Min)	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1810	−1705	−1620			
V_{OHC}	Output HIGH Voltage	−1035			mV	V_{IN} = V_{IH} (Min) or V_{IL} (Max)	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610			
V_{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = V_{IL} (Min)	

DC Electrical Characteristics

V_{EE} = −4.2V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1020		−870	mV	V_{IN} = V_{IH} (Max) or V_{IL} (Min)	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1810		−1605			
V_{OHC}	Output HIGH Voltage	−1030			mV	V_{IN} = V_{IH} (Min) or V_{IL} (Max)	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1595			
V_{IH}	Input HIGH Voltage	−1150		−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = V_{IL} (Min)	

DC Electrical Characteristics

V_{EE} = −4.8V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1035		−880	mV	V_{IN} = V_{IH} (Max) or V_{IL} (Min)	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830		−1620			
V_{OHC}	Output HIGH Voltage	−1045			mV	V_{IN} = V_{IH} (Min) or V_{IL} (Max)	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610			
V_{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1830		−1490	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = V_{IL} (Min)	

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Parametric values specified at −4.2V to −4.8V.

Note 3: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 4: Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DC Electrical Characteristics

V_{EE} = −4.2V to −4.8V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C

Symbol	Parameter	Min	Typ	Max	Units	Conditions
I_{IH}	Input HIGH Current A_n, B_n, BM_n, AM_n, BS_n, AS_n, $\overline{E}$			265	μA	V_{IN} = $V_{IH\ (Max)}$
I_{EE}	Power Supply Current	−235	−161	−107	mA	Inputs Open

Ceramic Dual-In-Line Package AC Electrical Characteristics

V_{EE} = −4.2V to −4.8V, V_{CC} = V_{CCA} = GND

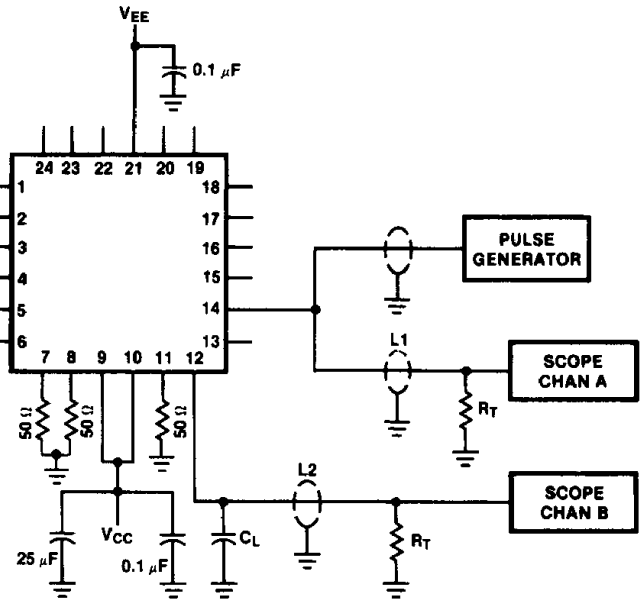
Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay A_n, B_n to Outputs (Transparent Mode)	0.45	1.90	0.50	1.80	0.50	2.00	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to Outputs	1.00	2.50	1.00	2.40	1.00	2.50	ns	
t_{PLH} t_{PHL}	Propagation Delay AM_n, BM_n, AS_n, BS_n to Outputs (Transparent Mode)	1.20	3.70	1.20	3.70	1.20	3.80	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.90	0.45	1.80	0.45	1.90	ns	
t_S	Setup Time A_n, B_n AM_n, BM_n, AS_n, BS_n	0.80 2.90		0.80 2.90		0.80 2.90		ns	*Figure 3*
t_H	Hold Time A_n, B_n AM_n, BM_n, AS_n, BS_n	2.10 0.80		2.10 0.80		2.10 0.80		ns	
$t_{pw}(L)$	Pulse Width LOW $\overline{E}$	2.00		2.00		2.00		ns	*Figure 2*

Cerpak AC Electrical Characteristics

V_{EE} = −4.2V to −4.8V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay A_n, B_n to Outputs (Transparent Mode)	0.45	1.70	0.50	1.60	0.50	1.80	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to Outputs	1.00	2.30	1.00	2.20	1.00	2.30	ns	
t_{PLH} t_{PHL}	Propagation Delay AM_n, BM_n, AS_n, BS_n to Outputs (Transparent Mode)	1.20	3.50	1.20	3.50	1.20	3.60	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.80	0.45	1.70	0.45	1.80	ns	
t_S	Setup Time A_n, B_n AM_n, BM_n, AS_n, BS_n	0.70 2.80		0.70 2.80		0.70 2.80		ns	*Figure 3*
t_H	Hold Time A_n, B_n AM_n, BM_n, AS_n, BS_n	2.00 0.70		2.00 0.70		2.00 0.70		ns	
$t_{pw}(L)$	Pulse Width LOW $\overline{E}$	2.00		2.00		2.00		ns	*Figure 2*

3



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Notes:
V_{CC}, V_{CCA} = +2V, V_{EE} = −2.5V
L1 and L2 = equal length 50Ω impedance lines
R_T = 50Ω terminator internal to scope
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 50Ω to GND
C_L = Fixture and stray capacitance ≤ 3 pF
Pin numbers shown are for flatpak; for DIP see logic symbol

FIGURE 1. AC Test Circuit

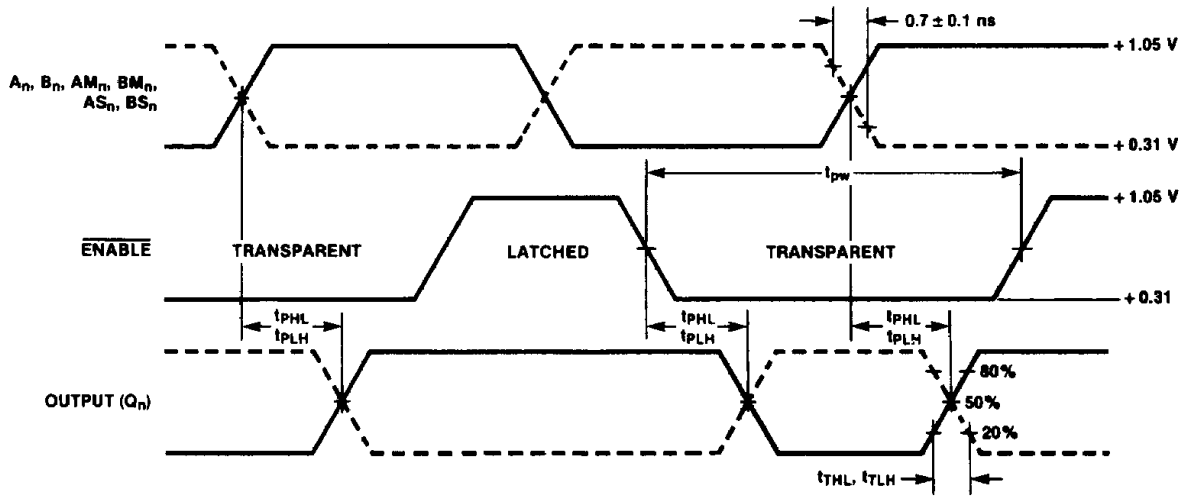

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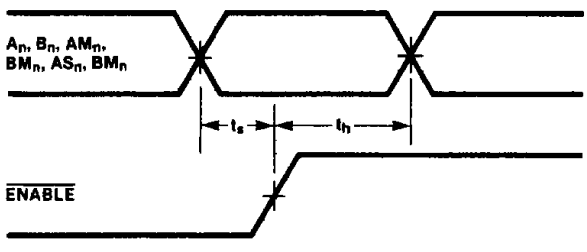
FIGURE 2. Enable Timing



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Notes:
t_s is the minimum time before the transition of the enable that information must be present at the designated input.
t_h is the minimum time after the transition of the enable that information must remain unchanged at the designated input.

FIGURE 3. Data Setup and Hold Times