National Semiconductor

ADVANCE INFORMATION

F100311
Low Skew 1:9 Differential Clock Driver

General Description

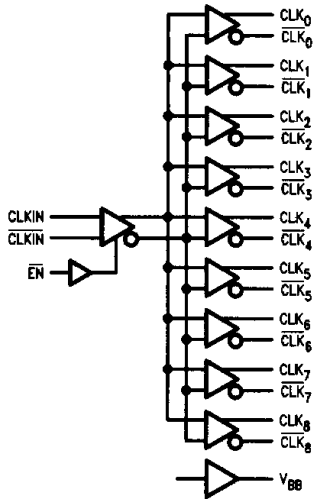
The F100311 contains nine low skew differential drivers, designed for generation of multiple, minimum skew differential clocks from a single differential input (CLKIN, $\overline{CLKIN}$). If a single-ended input is desired, the V_{BB} output pin may be used to drive the remaining input line. A HIGH on the enable pin ($\overline{EN}$) will force a LOW on all of the CLK_n outputs and a HIGH on all of the $\overline{CLK}_n$ output pins. A LOW on $\overline{EN}$ will return control of the $CLK_n/\overline{CLK}_n$ outputs back to the CLKIN/$\overline{CLKIN}$ inputs.

The skew specifications on the F100311 are fully tested and guaranteed.

Features

- Low output to output skew (≤ 75 ps)
- 2000V ESD protection
- 1:9 low skew clock driver
- Differential inputs and outputs

Logic Symbol



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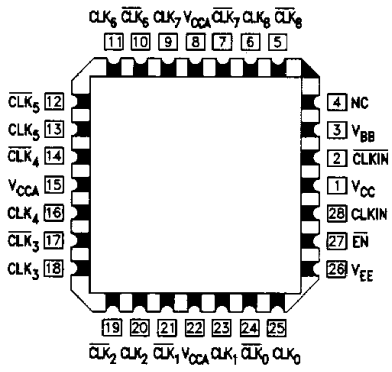
Pin Names	Description
CLKIN, $\overline{CLKIN}$	Differential Clock Inputs
$\overline{EN}$	Enable
CLK_{0-8}, $\overline{CLK}_{0-8}$	Differential Clock Outputs
V_{BB}	V_{BB} Output
NC	No Connect

Truth Table

CLKIN	$\overline{CLKIN}$	$\overline{EN}$	CLK_n	$\overline{CLK}_n$
L	H	L	L	H
H	L	L	H	L
X	X	H	L	H

Connection Diagram

28-Pin PCC



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