National Semiconductor

F100353
Low Power 8-Bit Register

General Description

The F100353 contains eight D-type edge triggered, master/slave flip-flops with individual inputs (D_n), true outputs (Q_n), a clock input (CP), and a common clock enable pin ($\overline{CEN}$). Data enters the master when CP is LOW and transfers to the slave when CP goes HIGH. When the $\overline{CEN}$ input goes HIGH it overrides all other inputs, disables the clock, and the Q outputs maintain the last state.

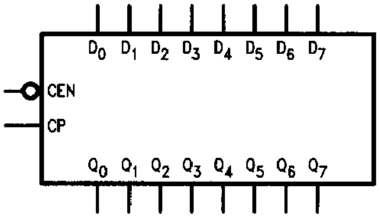
The F100353 output drivers are designed to drive 50Ω termination to −2.0V. All inputs have 50 kΩ pull-down resistors.

Features

- Low power operation
- 2000V ESD protection
- Voltage compensated operating range = −4.2V to −5.7V

Ordering Code: See Section 8

Logic Symbol



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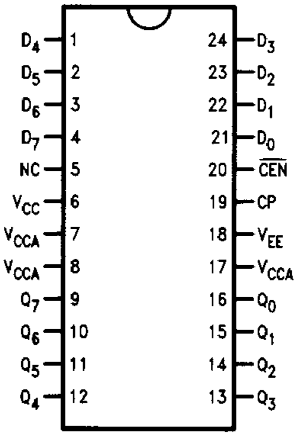
Pin Names	Description
D_0–D_7	Data Inputs
$\overline{CEN}$	Clock Enable Input
CP	Clock Input (Active Rising Edge)
Q_0–Q_7	Data Outputs
NC	No Connect

Connection Diagrams

24-Pin DIP



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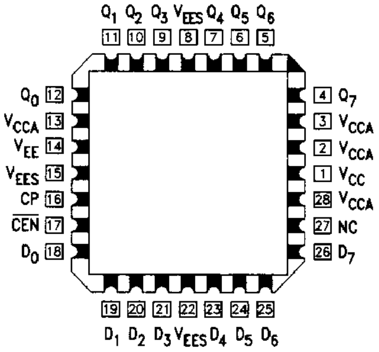
28-Pin PCC



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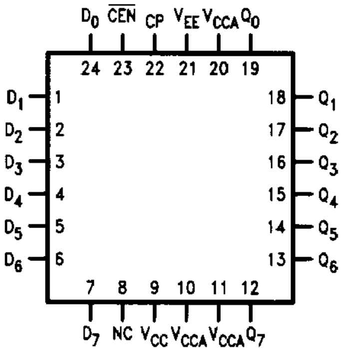
24-Pin Quad Cerpak



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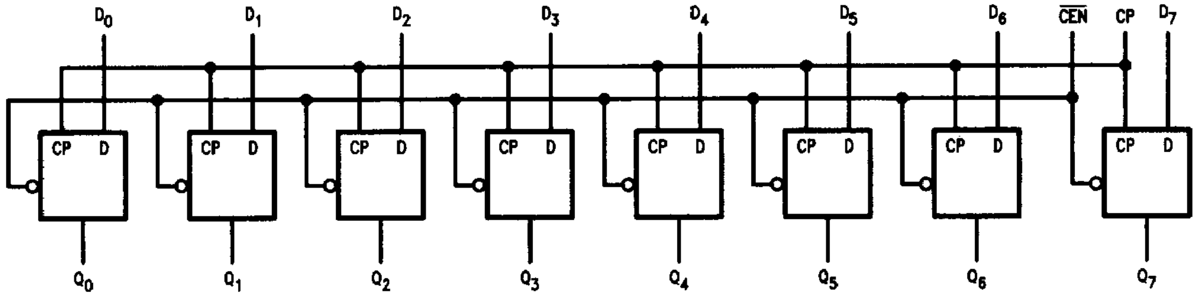
Logic Diagram



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Truth Table

Inputs			Outputs
D_n	$\overline{CEN}$	CP	Q_n
L	L	_/‾	L
H	L	_/‾	H
X	X	L	NC
X	X	H	NC
X	H	X	NC

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
NC = No Change
_/‾ = LOW to HIGH Transition

Absolute Maximum Ratings

Above which the useful life may be impared (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature (T_{STG})	−65°C to +150°C
Maximum Junction Temperature (T_J)	
Ceramic	+175°C
Plastic	+150°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} to + 0.5V
Output Current (DC Output HIGH)	−50 mA
ESD (Note 2)	≥2000V

Recommended Operating Conditions

Case Temperature (T_C)	
Commercial	0°C to +85°C
Military	−55°C to +125°C
Supply Voltage (V_{EE})	
Commercial	−5.7V to −4.2V
Military	−5.7V to −4.2V

Commercial Version

DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions	
V_{OH}	Output HIGH Voltage	−1025	−955	−870	mV	V_{IN} = V_{IH} (Max) or V_{IL} (Min)	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830	−1705	−1620	mV		
V_{OHC}	Output HIGH Voltage	−1035			mV	V_{IN} = V_{IH} (Min) or V_{IL} (Max)	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610	mV		
V_{IH}	Input HIGH Voltage	−1165		−870	mV	Guaranteed HIGH Signal for all Inputs	
V_{IL}	Input LOW Voltage	−1830		−1475	mV	Guaranteed LOW Signal for all Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = V_{IL} (Min)	
I_{IH}	Input HIGH Current			240	μA	V_{IN} = V_{IH}(Max)	
I_{EE}	Power Supply Current	 −119 −122		 −61 −61	mA	Inputs Open V_{EE} = −4.2V to −4.8V V_{EE} = −4.2V to −5.7V	

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: ESD testing conforms to MIL-STD-883, Method 3015.

Note 3: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

Ceramic Dual-In-Line Package AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
f_{max}	Toggle Frequency	425		425		425		MHz	*Figures 2, 3*
t_{PLH} t_{PHL}	Propagation Delay CP to Output	1.40	3.00	1.40	3.00	1.50	3.10	ns	*Figures 1, 3* (Note 1)
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	2.00	0.45	2.00	0.45	2.00	ns	*Figures 1, 3*
t_s	Setup Time D_n $\overline{CEN}$ (Disable Time) $\overline{CEN}$ (Release Time)	 1.10 0.40 1.10		 1.10 0.40 1.10		 1.10 0.40 1.10		ns	*Figures 1, 4*
t_h	Hold Time D_n	0.10		0.10		0.10		ns	*Figures 1, 5*
t_{pw}(H)	Pulse Width HIGH CP	2.00		2.00		2.00		ns	*Figures 1, 3*

Note 1: The propagation delay specified is for single output switching. Delays may vary up to 300 ps with multiple outputs switching.

Commercial Version (Continued)

PCC and Cerpack AC Electrical Characteristics

$V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} =$ GND

Symbol	Parameter	$T_C = 0°C$		$T_C = +25°C$		$T_C = +85°C$		Units	Conditions
		Min	Max	Min	Max	Min	Max		
f_{max}	Toggle Frequency	425		425		425		MHz	*Figures 2, 3*
t_{PLH} t_{PHL}	Propagation Delay CP to Output	1.40	2.80	1.40	2.80	1.50	2.90	ns	*Figures 1, 3* (Note 2)
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.90	0.45	1.90	0.45	1.90	ns	*Figures 1, 3*
t_s	Setup Time D_n $\overline{CEN}$ (Disable Time) $\overline{CEN}$ (Release Time)	 1.00 0.30 1.00		 1.00 0.30 1.00		 1.00 0.30 1.00		ns	*Figures 1, 4*
t_h	Hold Time D_n	0		0		0		ns	*Figures 1, 5*
$t_{pw}(H)$	Pulse Width HIGH CP	2.00		2.00		2.00		ns	*Figures 1, 3*
$t_{S, G\text{-}G}$	Skew, Gate to Gate		TBD		TBD		TBD	ps	PCC Only (Note 1)

Note 1: Gate to gate skew is defined as the difference in propagation delays between each of the outputs.

Note 2: The propagation delay specified is for single output switching. Delays may vary up to 300 ps with multiple outputs switching.

Military Version—Preliminary

DC Electrical Characteristics

$V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} =$ GND, $T_C = -55°C$ to $+125°C$

Symbol	Parameter	Min	Max	Units	T_C	Conditions		Notes
V_{OH}	Output HIGH Voltage	−1025	−870	mV	0°C to +125°C	$V_{IN} = V_{IH}$ (Max) or V_{IL} (Min)	Loading with 50Ω to −2.0V	1, 2, 3
		−1085	−870	mV	−55°C			
V_{OL}	Output LOW Voltage	−1830	−1620	mV	0°C to +125°C			
		−1830	−1555	mV	−55°C			
V_{OHC}	Output HIGH Voltage	−1035		mV	0°C to +125°C	$V_{IN} = V_{IH}$ (Min) or V_{IL} (Max)	Loading with 50Ω to −2.0V	1, 2, 3
		−1085		mV	−55°C			
V_{OLC}	Output LOW Voltage		−1610	mV	0°C to +125°C			
			−1555	mV	−55°C			
V_{IH}	Input HIGH Voltage	−1165	−870	mV	−55°C to +125°C	Guaranteed HIGH Signal for all Inputs		1, 2, 3, 4
V_{IL}	Input LOW Voltage	−1830	−1475	mV	−55°C to +125°C	Guaranteed LOW Signal for all Inputs		1, 2, 3, 4
I_{IL}	Input LOW Current	0.50		μA	−55°C to +125°C	$V_{EE} = -4.2V$ $V_{IN} = V_{IL}$ (Min)		1, 2, 3

Military Version—Preliminary (Continued)

DC Electrical Characteristics (Continued)

$V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$, $T_C = -55°C$ to $+125°C$

Symbol	Parameter	Min	Max	Units	T_C	Conditions	Notes
I_{IH}	Input HIGH Current		240	μA	0°C to +125°C	$V_{EE} = -5.7V$ $V_{IN} = V_{IH}$ (Max)	1, 2, 3
			340	μA	−55°C		
I_{EE}	Power Supply Current	 −125 −130	−50	mA	−55°C to +125°C	Inputs Open $V_{EE} = -4.2V$ to $-4.8V$ $V_{EE} = -4.2V$ to $-5.7V$	1, 2, 3

Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals −55°C), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 2: Screen tested 100% on each device at −55°C, +25°C, and +125°C, Subgroups 1, 2, 3, 7, and 8.

Note 3: Sample tested (Method 5005, Table I) on each manufactured lot at −55°C, +25°C, and +125°C, Subgroups A1, 2, 3, 7, and 8.

Note 4: Guaranteed by applying specified input condition and testing V_{OH}/V_{OL}.

Ceramic Dual-In-Line Package AC Electrical Characteristics

$V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_C = -55°C$		$T_C = +25°C$		$T_C = +125°C$		Units	Conditions	Notes
		Min	Max	Min	Max	Min	Max			
f_{max}	Toggle Frequency	400		400		400		MHz	*Figures 2, 3*	4
t_{PLH} t_{PHL}	Propagation Delay CP to Output	0.70	3.30	0.80	3.10	0.80	3.80	ns	*Figures 1, 3*	1, 2, 3, 5
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.40	2.50	0.40	2.40	0.40	2.70	ns		4
t_s	Setup Time D_n $\overline{CEN}$ (Disable Time) $\overline{CEN}$ (Release Time)	 0.60 0.90 1.40		 0.60 0.70 1.40		 0.60 0.90 2.10		ns	*Figures 1, 4*	4
t_h	Hold Time D_n	0.30		0.30		0.30		ns	*Figures 1, 5*	4
$t_{pw}(H)$	Pulse Width HIGH CP	2.00		2.00		2.00		ns	*Figures 1, 3*	4

Cerpak AC Electrical Characteristics

$V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_C = -55°C$		$T_C = +25°C$		$T_C = +125°C$		Units	Conditions	Notes
		Min	Max	Min	Max	Min	Max			
f_{max}	Toggle Frequency	425		425		425		MHz	*Figures 2, 3*	4
t_{PLH} t_{PHL}	Propagation Delay CP to Output	1.30	3.20	1.30	3.20	1.40	3.30	ns	*Figures 1, 3*	1, 2, 3, 5
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	2.00	0.45	2.00	0.45	2.00	ns		4
t_s	Setup Time D_n $\overline{CEN}$ (Disable Time) $\overline{CEN}$ (Release Time)	 1.30 0.60 1.30		 1.30 0.60 1.30		 1.30 0.60 1.30		ns	*Figures 1, 4*	4
t_h	Hold Time D_n	0.30		0.30		0.30		ns	*Figures 1, 5*	4
$t_{pw}(H)$	Pulse Width HIGH CP	2.00		2.00		2.00		ns	*Figures 1, 3*	4

Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals −55°C), then testing immediately after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

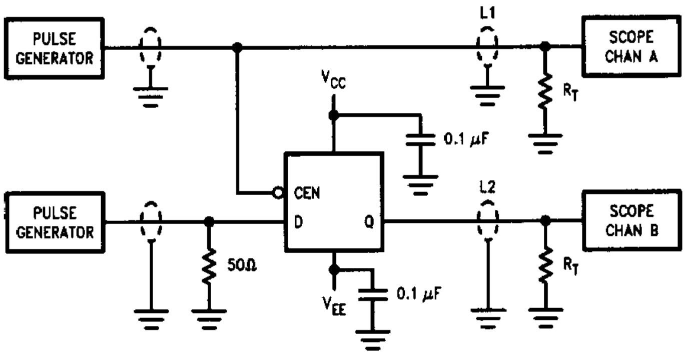
Note 2: Screen tested 100% on each device at +25°C temperature only, Subgroup A9.

Note 3: Sample tested (Method 5005, Table I) on each manufactured lot at +25°C, Subgroup A9, and at +125°C and −55°C, temperatures, Subgroups A10 and A11.

Note 4: Not tested at +25°C, +125°C, and −55°C temperature (design characterization data).

Note 5: The propagation delay specified is for single output switching. Delays may vary up to 300 ps with multiple outputs switching.

Test Circuitry



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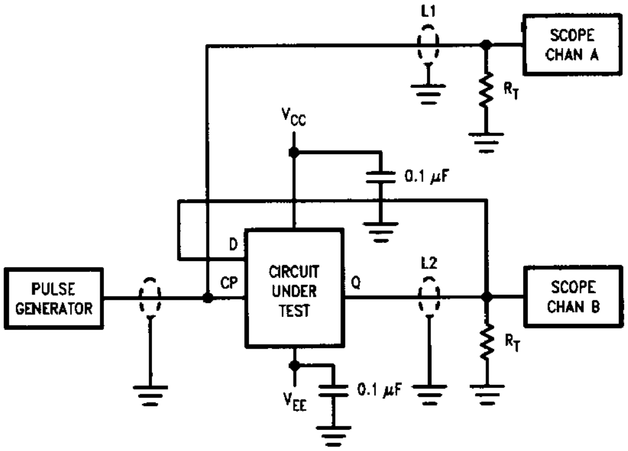
Notes:

FIGURE 1. AC Test Circuit

V_{CC}, V_{CCA} = +2V, V_{EE} = −2.5V
L1 and L2 = equal length 50Ω impedance lines
R_T = 50Ω terminator internal to scope
Decoupling 0.1 µF from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 50Ω to GND
C_L = Fixture and stray capacitance ≤ 3 pF



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Notes:

FIGURE 2. Toggle Frequency Test Circuit

V_{CC}, V_{CCA} = +2V, V_{EE} = −2.5V
L1 and L2 = equal length 50Ω impedance lines
R_T = 50Ω terminator internal to scope
Decoupling 0.1 µF from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 50Ω to GND
C_L = Jig and stray capacitance ≤ 3 pF

Switching Waveforms

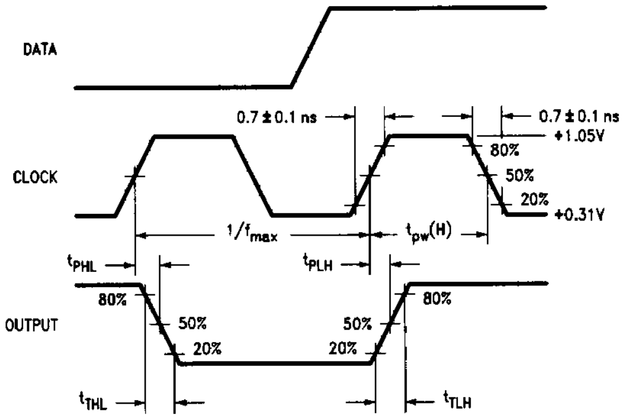

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FIGURE 3. Propagation Delay (Clock) and Transition Times

Switching Waveforms (Continued)

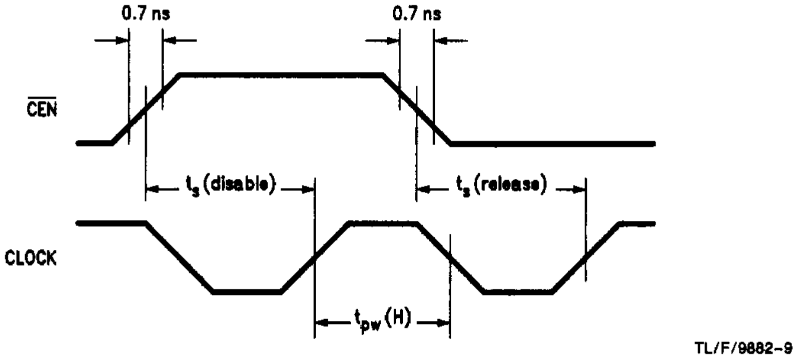

FIGURE 4. Setup and Pulse Width Times

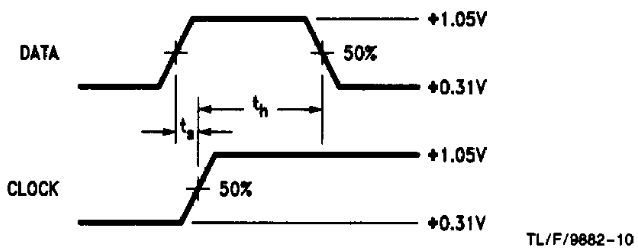

FIGURE 5. Data Setup and Hold Time

Note 1: t_s is the minimum time before the transition of the clock that information must be present at the data input.

Note 2: t_h is the minimum time after the transition of the clock that information must remain unchanged at the data input.