

F100355

Low Power Quad Multiplexer/Latch

General Description

The F100355 contains four transparent latches, each of which can accept and store data from two sources. When both Enable (E_n) inputs are LOW, the data that appears at an output is controlled by the Select (S_n) inputs, as shown in the Operating Mode table. In addition to routing data from either D_0 or D_1 , the Select inputs can force the outputs LOW for the case where the latch is transparent (both Enables are LOW) and can steer a HIGH signal from either D_0 or D_1 to an output. The Select inputs can be tied together for applications requiring only that data be steered from either D_0 or D_1 . A positive-going signal on either Enable input

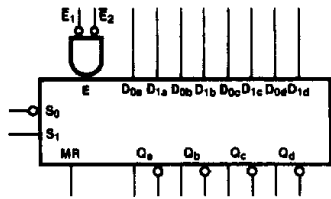
latches the outputs. A HIGH signal on the Master Reset (MR) input overrides all the other inputs and forces the Q outputs LOW. All inputs have 50 k Ω pulldown resistors.

Features

- Greater than 40% power reduction of the F100155
- 2000V ESD protection
- Pin/function compatible with F100155
- Voltage compensated operating range = $-4.2V$ to $-5.7V$

Ordering Code: See Section 8

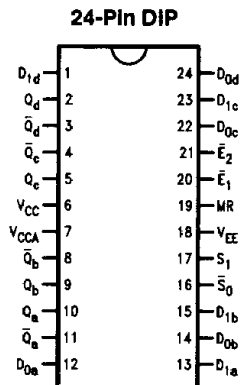
Logic Symbol



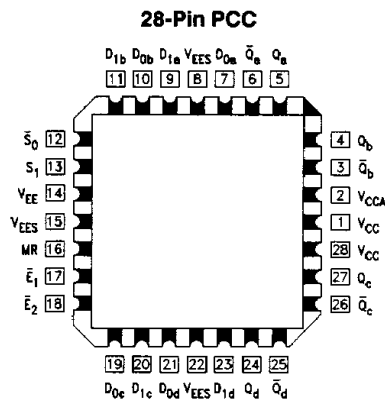
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Pin Names	Description
E_1, E_2	Enable Inputs (Active LOW)
\bar{S}_0, S_1	Select Inputs
MR	Master Reset
$D_{na}-D_{nd}$	Data Inputs
Q_a-Q_d	Data Outputs
$\bar{Q}_a-\bar{Q}_d$	Complementary Data Outputs

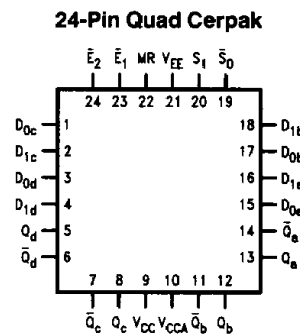
Connection Diagrams



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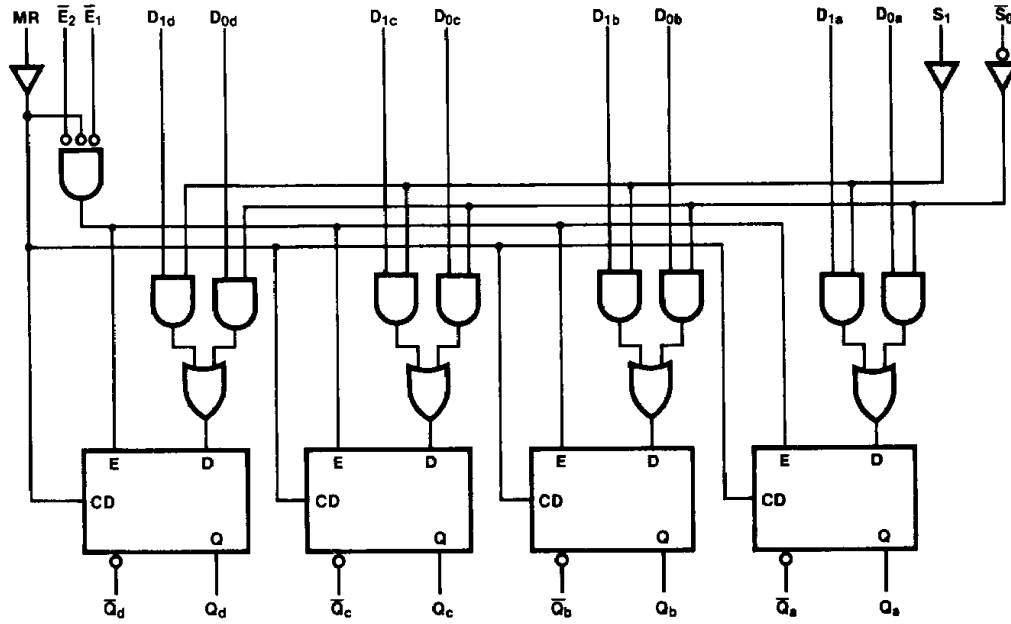
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Logic Diagram



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Operating Mode Table

Controls				Outputs
\bar{E}_1	\bar{E}_2	S_1	\bar{S}_0	Q_n
H	X	X	X	Latched*
X	H	X	X	Latched*
L	L	L	L	D_{0x}
L	L	H	L	$D_{0x} + D_{1x}$
L	L	L	H	L
L	L	H	H	D_{1x}

*Stores data present before \bar{E} went HIGH
 H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Don't Care

Truth Table

Inputs							Outputs	
MR	\bar{E}_1	\bar{E}_2	S_1	\bar{S}_0	D_{1x}	D_{0x}	\bar{Q}_x	Q_x
H	X	X	X	X	X	X	H	L
L	L	L	H	H	H	X	L	H
L	L	L	H	H	L	X	H	L
L	L	L	L	L	X	H	L	H
L	L	L	L	L	X	L	H	L
L	L	L	L	H	X	X	H	L
L	L	L	H	L	H	X	L	H
L	L	L	H	L	X	H	L	H
L	L	L	H	L	L	L	H	L
L	H	X	X	X	X	X	Latched*	Latched*
L	X	H	X	X	X	X	Latched*	Latched*

Absolute Maximum Ratings

Above which the useful life may be impaired. (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature (T_{STG})	-65°C to +150°C
Maximum Junction Temperature (T_J)	
Ceramic	+175°C
Plastic	+150°C
V_{EE} Pin Potential to Ground Pin	-7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current (DC Output HIGH)	-50 mA
ESD (Note 2)	≥2000V

Recommended Operating Conditions

Case Temperature (T_C)	
Commercial	0°C to +85°C
Military	-55°C to +125°C
Supply Voltage (V_{EE})	
Commercial	-5.7V to -4.2V
Military	-5.7V to -4.2V

Commercial Version

DC Electrical Characteristics

$V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$, $T_C = 0°C$ to $+85°C$ (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{OH}	Output HIGH Voltage	-1025	-955	-870	mV	$V_{IN} = V_{IH} (Max)$ or $V_{IL} (Min)$
V_{OL}	Output LOW Voltage	-1830	-1705	-1620	mV	
V_{OHC}	Output HIGH Voltage	-1035			mV	$V_{IN} = V_{IH} (Min)$ or $V_{IL} (Max)$
V_{OLC}	Output LOW Voltage			-1610	mV	
V_{IH}	Input HIGH Voltage	-1165		-870	mV	Guaranteed HIGH Signal for ALL Inputs
V_{IL}	Input LOW Voltage	-1830		-1475	mV	Guaranteed LOW Signal for ALL Inputs
I_{IL}	Input LOW Current	0.50			μA	$V_{IN} = V_{IL} (Min)$
I_{IH}	Input HIGH Current \bar{S}_0, S_1 \bar{E}_1, \bar{E}_2 $D_{na} - D_{nd}$ MR			220 350 340 430	μA	$V_{IN} = V_{IH} (Max)$
I_{EE}	Power Supply Current	-87		-40	mA	Inputs Open

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: ESD testing conforms to MIL-STD-883, Method 3015.

Note 3: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

Commercial Version (Continued)**Ceramic Dual-In-Line Package AC Electrical Characteristics** $V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_C = 0^\circ C$		$T_C = +25^\circ C$		$T_C = +85^\circ C$		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay $D_{na}-D_{nd}$ to Output (Transparent Mode)	0.60	1.90	0.60	1.90	0.70	2.00	ns	<i>Figures 1 and 2</i>
t_{PLH} t_{PHL}	Propagation Delay \bar{S}_0, S_1 to Output (Transparent Mode)	1.00	2.60	1.00	2.60	1.20	2.70	ns	
t_{PLH} t_{PHL}	Propagation Delay \bar{E}_1, \bar{E}_2 to Output	0.80	2.00	0.80	2.00	0.80	2.10	ns	
t_{PLH} t_{PHL}	Propagation Delay MR to Output	0.80	2.30	0.80	2.30	0.80	2.30	ns	<i>Figures 1 and 3</i>
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.60	1.40	0.60	1.40	0.60	1.40	ns	<i>Figures 1 and 2</i>
t_S	Setup Time $D_{na}-D_{nd}$	0.90		0.90		0.90		ns	<i>Figure 4</i>
	\bar{S}_0, S_1	1.70		1.70		1.70			
	MR (Release Time)	1.50		1.50		1.50			<i>Figure 3</i>
t_H	Hold Time $D_{na}-D_{nd}$	0.40		0.40		0.40		ns	<i>Figure 4</i>
	\bar{S}_0, S_1	0.00		0.00		0.00			
$t_{pw} (L)$	Pulse Width LOW \bar{E}_1, \bar{E}_2	2.00		2.00		2.00		ns	<i>Figure 2</i>
$t_{pw} (H)$	Pulse Width HIGH MR	2.00		2.00		2.00		ns	<i>Figure 3</i>

Commercial Version (Continued)**PCC and Cerpak AC Electrical Characteristics** $V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_C = 0^\circ C$		$T_C = +25^\circ C$		$T_C = +85^\circ C$		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay $D_{na}-D_{nd}$ to Output (Transparent Mode)	0.60	1.70	0.60	1.70	0.70	1.80	ns	Figures 1 and 2
t_{PLH} t_{PHL}	Propagation Delay \bar{S}_0, S_1 to Output (Transparent Mode)	1.00	2.40	1.00	2.40	1.20	2.50	ns	
t_{PLH} t_{PHL}	Propagation Delay \bar{E}_1, \bar{E}_2 to Output	0.80	1.80	0.80	1.80	0.80	1.90	ns	
t_{PLH} t_{PHL}	Propagation Delay MR to Output	0.80	2.10	0.80	2.10	0.80	2.10	ns	Figures 1 and 3
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.60	1.30	0.60	1.30	0.60	1.30	ns	Figures 1 and 2
t_S	Setup Time $D_{na}-D_{nd}$	0.80		0.80		0.80		ns	Figure 4
	\bar{S}_0, S_1	1.60		1.60		1.60			Figure 3
	MR (Release Time)	1.40		1.40		1.40			
t_H	Hold Time $D_{na}-D_{nd}$	0.30		0.30		0.30		ns	Figure 4
	\bar{S}_0, S_1	-0.10		-0.10		-0.10			
$t_{pw}(L)$	Pulse Width LOW \bar{E}_1, \bar{E}_2	2.00		2.00		2.00		ns	Figure 2
$t_{pw}(H)$	Pulse Width HIGH MR	2.00		2.00		2.00		ns	Figure 3
$t_{S\ G-G}$	Skew Gate to Gate		TBD		TBD		TBD	ps	PCC Only (Note 1)

Note 1: Gate to gate skew is defined as the difference in the propagation delays between each of the outputs.

Military Version — Preliminary**DC Electrical Characteristics** $V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$, $T_C = -55^{\circ}C$ to $+125^{\circ}C$

Symbol	Parameter	Min	Max	Units	T_C	Conditions	Notes		
V_{OH}	Output HIGH Voltage	-1025	-870	mV	$0^{\circ}C$ to $+125^{\circ}C$	$V_{IN} = V_{IH} (Max)$ or $V_{IL} (Min)$	Loading with 50Ω to $-2.0V$	1,2,3	
		-1085	-870	mV	$-55^{\circ}C$				
V_{OL}	Output LOW Voltage	-1830	-1620	mV	$0^{\circ}C$ to $+125^{\circ}C$				
		-1830	-1555	mV	$-55^{\circ}C$				
V_{OHC}	Output HIGH Voltage	-1035		mV	$0^{\circ}C$ to $+125^{\circ}C$	$V_{IN} = V_{IH} (Min)$ or $V_{IL} (Max)$	Loading with 50Ω to $-2.0V$	1,2,3	
		-1085		mV	$-55^{\circ}C$				
V_{OLC}	Output LOW Voltage		-1610	mV	$0^{\circ}C$ to $+125^{\circ}C$				
			-1555	mV	$-55^{\circ}C$				
V_{IH}	Input HIGH Voltage	-1165	-870	mV	$-55^{\circ}C$ to $+125^{\circ}C$	Guaranteed HIGH Signal for ALL Inputs	1,2,3,4		
V_{IL}	Input LOW Voltage	-1830	-1475	mV	$-55^{\circ}C$ to $+125^{\circ}C$	Guaranteed LOW Signal for ALL Inputs	1,2,3,4		
I_{IL}	Input LOW Current	0.50		μA	$-55^{\circ}C$ to $+125^{\circ}C$	$V_{EE} = -4.2V$ $V_{IN} = V_{IL} (Min)$	1,2,3		
I_{IH}	Input HIGH Current \bar{S}_0, S_1 E_1, E_2 $D_{na}-D_{nd}$ MR		220 350 340 430	μA	$0^{\circ}C$ to $+125^{\circ}C$	$V_{EE} = -5.7V$ $V_{IN} = V_{IH} (Max)$	1,2,3		
			320 500 490 630		$-55^{\circ}C$				
I_{EE}	Power Supply Current	-95	-32	mA	$-55^{\circ}C$ to $+125^{\circ}C$			Inputs Open	1,2,3

Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals $-55^{\circ}C$), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 2: Screen tested 100% on each device at $-55^{\circ}C$, $+25^{\circ}C$, and $+125^{\circ}C$ Temp., Subgroups 1, 2, 3, 7, and 8.

Note 3: Sample tested (Method 5005, Table 1) on each Mfg. lot at $+25^{\circ}$, $+125^{\circ}C$, and $-55^{\circ}C$ Temp., Subgroups 1, 2, 3, 7, and 8.

Note 4: Guaranteed by applying specified input condition and testing V_{OH}/V_{OL} .

Military Version — Preliminary (Continued)**Ceramic Dual-In-Line Package AC Electrical Characteristics** $V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_C = -55^\circ C$		$T_C = +25^\circ C$		$T_C = +125^\circ C$		Units	Conditions	Notes
		Min	Max	Min	Max	Min	Max			
t_{PLH} t_{PHL}	Propagation Delay $D_{na}-D_{nd}$ to Output (Transparent Mode)	0.40	2.30	0.50	2.20	0.50	2.60	ns	Figures 1 and 2	1,2,3
t_{PLH} t_{PHL}	Propagation Delay \bar{S}_0, S_1 to Output (Transparent Mode)	0.60	3.00	0.80	2.70	0.80	3.20	ns		
t_{PLH} t_{PHL}	Propagation Delay \bar{E}_1, \bar{E}_2 to Output	0.50	2.60	0.60	2.30	0.70	2.70	ns		
t_{PLH} t_{PHL}	Propagation Delay MR to Output	0.60	2.80	0.70	2.60	0.70	2.90	ns	Figures 1 and 3	1,2,3
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.40	1.90	0.40	1.90	0.40	1.90	ns	Figures 1 and 2	4
t_S	Setup Time $D_{na}-D_{nd}$ \bar{S}_0, S_1 MR (Release Time)	0.90		0.90		0.90		ns	Figure 4	4
		2.40		2.40		2.40			Figure 3	
		1.50		1.50		1.50				
t_H	Hold Time $D_{na}-D_{nd}$ \bar{S}_0, S_1	0.40		0.40		0.40		ns	Figure 4	4
		0.00		0.00		0.00				
$t_{pw}(L)$	Pulse Width LOW \bar{E}_1, \bar{E}_2	2.00		2.00		2.00		ns	Figure 2	4
$t_{pw}(H)$	Pulse Width HIGH MR	2.00		2.00		2.00		ns	Figure 3	4

Cerpak AC Electrical Characteristics $V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_C = -55^\circ C$		$T_C = +25^\circ C$		$T_C = +125^\circ C$		Units	Conditions	Notes
		Min	Max	Min	Max	Min	Max			
t_{PLH} t_{PHL}	Propagation Delay $D_{na}-D_{nd}$ to Output (Transparent Mode)	0.40	2.30	0.50	2.20	0.50	2.60	ns	Figures 1 and 2	1,2,3
t_{PLH} t_{PHL}	Propagation Delay \bar{S}_0, S_1 to Output (Transparent Mode)	0.60	3.00	0.80	2.70	0.80	3.20	ns		
t_{PLH} t_{PHL}	Propagation Delay \bar{E}_1, \bar{E}_2 to Output	0.50	2.60	0.60	2.30	0.70	2.70	ns		

Military Version — Preliminary (Continued)**Cerpak AC Electrical Characteristics** $V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_C = -55^\circ C$		$T_C = +25^\circ C$		$T_C = +125^\circ C$		Units	Conditions	Notes
		Min	Max	Min	Max	Min	Max			
t_{PLH} t_{PHL}	Propagation Delay MR to Output	0.60	2.80	0.70	2.60	0.70	2.90	ns	Figures 1 and 3	1,2,3
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.40	1.90	0.40	1.90	0.40	1.90	ns	Figures 1 and 2	4
t_S	Setup Time									
	$D_{na}-D_{nd}$	0.90		0.90		0.90		ns	Figure 4	4
	S_0, S_1 MR (Release Time)	2.40 1.50		2.40 1.50		2.40 1.50			Figure 3	
t_H	Hold Time									
	$D_{na}-D_{nd}$ S_0, S_1	0.40 0.00		0.40 0.00		0.40 0.00		ns	Figure 4	4
$t_{pw}(L)$	Pulse Width LOW \bar{E}_1, \bar{E}_2	2.00		2.00		2.00		ns	Figure 2	4
$t_{pw}(H)$	Pulse Width HIGH MR	2.00		2.00		2.00		ns	Figure 3	4

Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals $-55^\circ C$), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 2: Screen tested 100% on each device at $+25^\circ C$, Temperature only, Subgroup A9.

Note 3: Sample tested (Method 5005, Table 1) on each Mfg. lot at $+25^\circ C$, Subgroup A9, and at $+125^\circ C$, and $-55^\circ C$ Temp., Subgroups A10 & A11.

Note 4: Not tested at $+25^\circ C$, $+125^\circ C$ and $-55^\circ C$ Temperature (design characterization data).

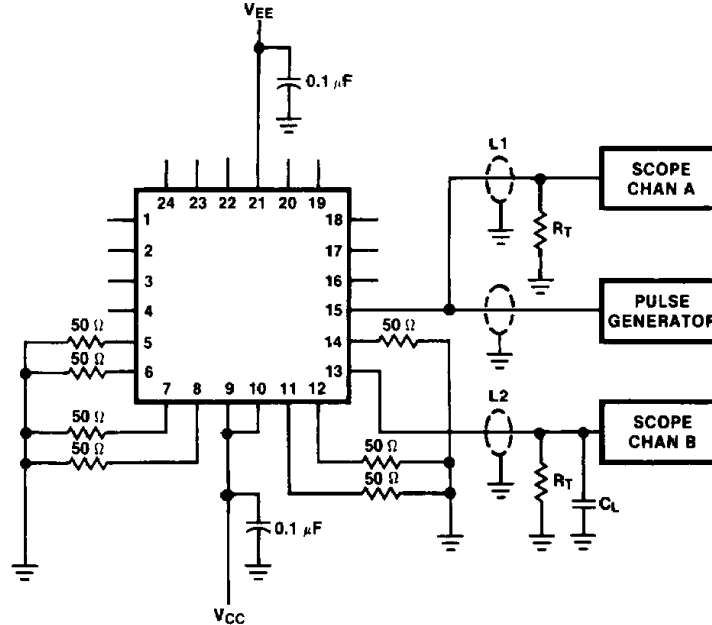
Test Circuit

FIGURE 1. AC Test Circuit
(Using Quad Cerpak)

TL/F/10147-6

Notes:

$V_{CC}, V_{CCA} = +2V$, $V_{EE} = -2.5V$

L1 and L2 = equal length 50Ω impedance lines

$R_T = 50\Omega$ terminator internal to scope

Decoupling 0.1 μF from GND to V_{CC} and V_{EE}

All unused outputs are loaded with 50Ω to GND

$C_L =$ Fixture and stray capacitance ≤ 3 pF

Pin numbers shown are for flatpak; for DIP see logic symbol

Switching Waveforms

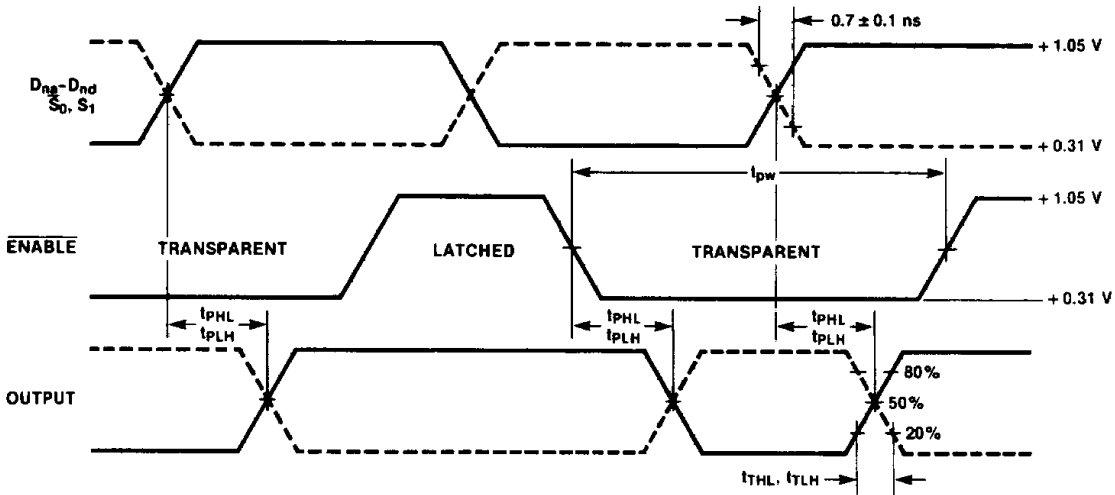


FIGURE 2. Enable Timing

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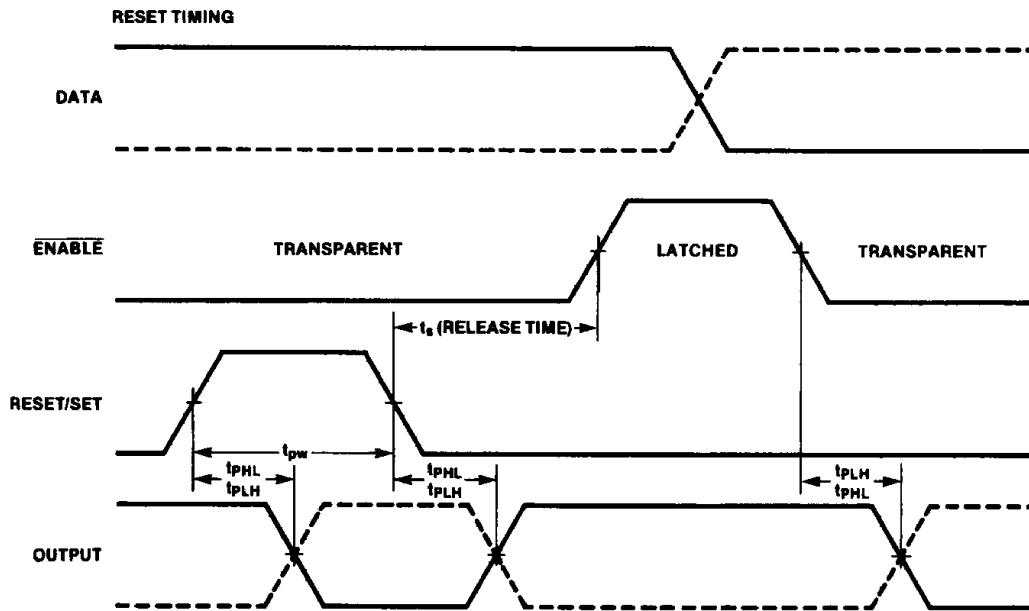
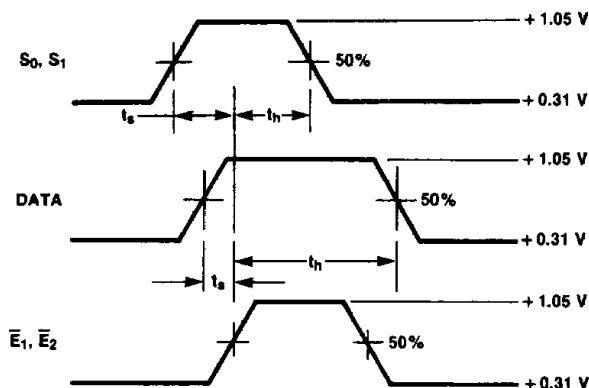


FIGURE 3. Reset Timing

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TL/F/10147-9

FIGURE 4. Data Setup and Hold Times

Notes:

t_s is the minimum time before the transition of the enable that information must be present at the data input.

t_h is the minimum time after the transition of the enable that information must remain unchanged at the data input.