

LM1204 150 MHz RGB Video Amplifier System

General Description

The LM1204 is a triple 150 MHz video amplifier system designed specifically for high resolution RGB video display applications. In addition to three matched video amplifiers, the LM1204 contains a DC operated contrast control, a DC operated drive control for each amplifier, and a dual clamping system for both brightness control and video blanking. The LM1204 also contains a back porch clamp pulse generator which is activated by an externally supplied $\pm H/HV$ sync signal or by an external composite video signal. The $\pm H/HV$ sync input will have priority over the composite video input. A single $-H/HV$ sync output is provided for the automatically selected sync input signal. The back porch clamp pulse width is user adjustable from 0.3 μs to 4 μs .

The LM1204 video output stage will directly drive most Hybrid or discrete CRT amplifier input stages without the need for an external buffer transistor. The device has been designed to operate from a 12V supply with all DC controls operating over a 0V to 4V range providing for an easy interface to serial digital buss controlled monitors.

Features

- Built-in video blanking function
- Built-in sync separator for composite video input
- Includes DC restoration of video signals
- Back porch clamp pulse width user adjustable
- DC control of brightness, contrast, blanking level, drive and cutoff
- DC controls are 0V to 4V for easy interfacing to a digitally controlled system

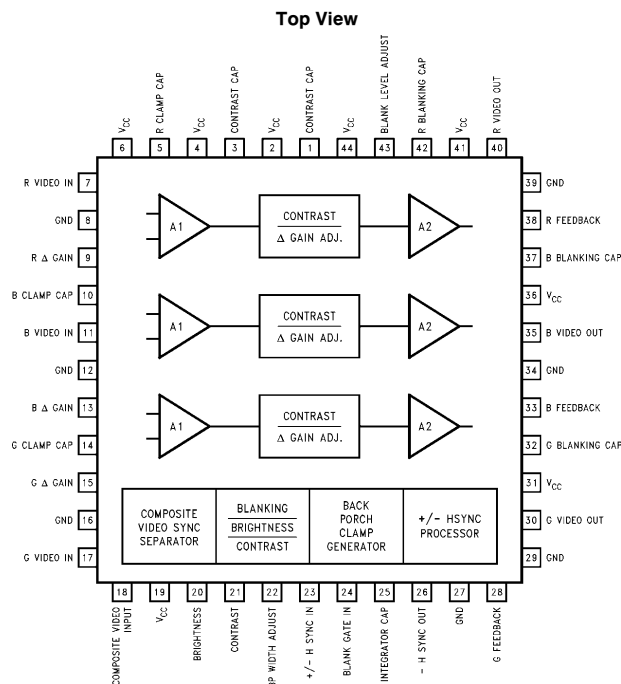
Key Specifications

- 150 MHz large signal bandwidth (typ)
- 2.3 ns rise/fall times (typ)
- 0.1 dB contrast tracking (typ)
- ± 3 dB drive (Δ gain) adjustments on R, G, B channels (typ)

Applications

- High resolution CRT monitors
- Video AGC amplifier
- Wideband amplifier with gain and DC offset control

Block Diagram and Connection Diagram



TL/H/11238-1

Ordering Information
Order Number LM1204V
See NS Package Number V44A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage, V_{CC}	
Pins 2, 4, 6, 19, 31, 41, 44 (Note 3)	13.5V
Peak Video Output Source Current (Any One Amplifier) Pins 30, 35 or 39	30 mA
Voltage at Any Input Pin, V_{IN}	$GND \leq V_{IN} \leq V_{CC}$
Maximum $\pm H$ Sync Input Voltage	5.5 V _{PP}
Power Dissipation, PD (Above 25°C)	
Derate Based on θ_{JA} and T_J)	2.4W

Thermal Resistance, θ_{JA}	52 °C/W
Junction Temperature, T_J	150°C
ESD Susceptibility (Note 4)	2.5 kV
Storage Temperature	– 65°C to 150°C
Lead Temperature	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C

Operating Ratings (Note 2)

Temperature Range	0°C to 70°C
Supply Voltage, V_{CC}	$10.8V \leq V_{CC} \leq 13.2V$

DC Electrical Characteristics (Video Amplifier Section)

The following specifications apply for V_{CC} (pins 2, 4, 6, 19, 31, 36, 41 and 44) = 12V and T_A = 25°C unless otherwise specified. S1 = B, S2 = B, S3, 4, 5 closed, V9, 13, 15 = 2V, V20, 21, 22, 24, 43 = 0.5V unless otherwise specified; see test circuit, Figure 1.

Symbol	Parameter	Conditions	Typical (Note 5)	Limit (Note 6)	Units
I_S	Supply Current	No Video or Sync Input Signals, S1 = A	100	125	mA (Max)
I_B	Input Bias Current (Pin 9, 13, 15, 20, 21 or 22)	S1 = A	0.3	2	μA (Max)
I_{24h}	Blank Gate Input High Current	V24 = 4V	0.01	2	μA (Max)
I_{24l}	Blank Gate Input Low Current	V24 = 0V	2	5	μA (Max)
I_{FB}	Feedback Input Current (Pin 28, 33 or 38)		150		nA
I_{Blank+}	Blank Cap Charge Current	$V_{32,37,42} = 0V$	185	75	μA (Min)
I_{Blank-}	Blank Cap Discharge Current	$V_{32,37,42} = 5V$	– 185	– 75	μA (Min)
I_{BB}	Blank Cap Bias Current (Pins 32, 37, 42)		20		nA
I_{Clamp+}	Clamp Cap Charge Current	$V_{5,10,14} = 0V$	185	75	μA (Min)
I_{Clamp-}	Blank Cap Discharge Current	$V_{5,10,14} = 5V$	– 185	– 75	μA (Min)
I_{CB}	Clamp Cap Bias Current (Pins 5, 10, 14)		20		nA
V _{24h}	Blank Gate High Input Voltage	Input Signal is Not Blanked		2	V (Min)
V _{24l}	Blank Gate Low Input Voltage	Input Signal is Blanked		0.8	V (Max)
	Blank Comparator Offset Voltage	Voltage between V43 and Any One Video Output	2	50	mV (Max)
V _H	Video Output High Voltage (Pins 30, 35, 40)	$R_L = 350\Omega$ V28, 33, 38 = 0V	8.7	7	V (Min)
V _L	Video Output Low Voltage (Pins 30, 35, 40)	$R_L = 350\Omega$ V28, 33, 38 = 4V	0.1	0.5	V (Max)
V _{CM43}	Common Mode Range of Blank Comparator (Pins 43, 28, 33, 38)			0.5	V (Min)
				4	V (Max)

DC Electrical Characteristics (Sync Separator/Processor Section)

The following specifications apply for V_{CC} (Pins 2, 4, 6, 19, 31, 36, 41 and 44) = 12V and T_A = 25°C, unless otherwise specified. S1 = B, S2 = B, S3, 4, 5 closed, V9, 13, 15 = 2V, V20, 21, 22, 24, 43 = 0.5V, unless otherwise specified; see Test Circuit *Figure 1*.

Symbol	Parameter	Conditions	Typical (Note 5)	Limit (Note 6)	Units
$-H V_{OH}$	$-H$ Sync Output Logic High (Pin 26)		4.2	2.4	V(Min)
$-H V_{OL}$	$-H$ Sync Output Logic Low (Pin 26)		0.1	0.4	V(Max)
V_{23}	Quiescent DC Voltage at $\pm H$ Sync Input		3		V

AC Electrical Characteristics (Video Amplifier Section)

The following specifications apply for V_{CC} (Pins 2, 4, 6, 19, 31, 36, 41 and 44) = 12V and T_A = 25°C, unless otherwise specified. S1 = B, S2 = B, S3, 4, 5 closed, V9, 13, 15, 21, 24, 43 = 4V, V20 = 2V, unless otherwise specified; see Test Circuit *Figure 1*.

Symbol	Parameter	Conditions	Typical (Note 5)	Limit (Note 6)	Units
R_{IN}	Video Amplifier Input Resistance		20		k Ω
A_{Vmax}	Maximum Video Amplifier Gain	$f_{IN} = 12$ kHz	10	5.5	V/V(Min)
ΔA_{Vtrack}	Amplifier Gain (Contrast) Tracking (Note 7)		0.1		dB
ΔA_{V2V}	Attenuation at 2V	Ref: A_{Vmax} V21 = 2V	6		dB
$\Delta A_{V0.5V}$	Attenuation at 0.5V	Ref: A_{Vmax} V21 = 0.5V	28	20	dB(Min)
$\Delta Gain$	Δ Gain Range (Pins 9, 13, 15)	V9, 13, 15 = 0V to 4V	± 3		dB
ΔV_O	Max Brightness Tracking Error (Note 8)		100		mV
f_{-3dB}	Video Amplifier Bandwidth (Note 9)	$V_{OUT} = 3.5 V_{PP}$	150		MHz
THD	Video Amplifier Distortion	$V_{OUT} = 1 V_{PP}$, $f = 12$ kHz	0.3		%
t_R	Video Output Rise Time (Note 9)	Square Wave Input $V_{OUT} = 3.5 V_{PP}$, $R_L = 350\Omega$	2.0		ns
t_F	Video Output Fall Time (Note 9)	Square Wave Input $V_{OUT} = 3.5 V_{PP}$, $R_L = 350\Omega$	2.3		ns
$V_{ISO} (1 \text{ MHz})$	Video Amplifier 1 MHz Isolation (Notes 9, 10)		-50		dB
$V_{ISO} (130 \text{ MHz})$	Video Amplifier 130 MHz Isolation (Notes 9, 10)		-10		dB

AC Electrical Characteristics (Sync Separator/Processor Section)

The following specifications apply for V_{CC} (Pins 2, 4, 6, 19, 31, 36, 41 and 44) = 12V and T_A = 25°C, unless otherwise specified. S1 = A, S2 = B, S3, 4, 5 closed, V9, 13, 15, 20, 21, 43 = 2V, unless otherwise specified; see Test Circuit *Figure 1* and Timing Diagram for input waveform.

Symbol	Parameter	Conditions	Typical (Note 5)	Limit (Note 6)	Units
$V_{18(\text{Min})}$	Composite Video Input Voltage (Pin 18)	S2 = A, Input = 10% Duty Cycle, Test for Loss of BP Pulse at Pin 26		0.15	V_{PP} (Min)
$V_{18(\text{Max})}$	Composite Video Input Voltage (Pin 18)			2	V_{PP} (Max)
V_{23}	$\pm$ H Sync Input Voltage (Pin 23)	Input = 10% Duty Cycle		1.6	V_{PP} (Min)
	Back Porch Clamp Pulse Width at $V_{24} = 1V$	S2 = A, Pin 26 = BP Output	1	1.4	μs (Max)
	Back Porch Clamp Pulse Width at $V_{24} = 4V$		300	600	ns (Max)
	Maximum $\pm$ H Sync Input Frequency		600		KHz
D_{HI}	Max Duty Cycle of Active High H Sync (Pin 23)	Test for Loss of Sync at Pin 26	22		%
D_{LO}	Max Duty Cycle of Active Low H Sync (Pin 23)		22		%
t_{pd1}	$\pm$ H Sync Input to $-$ H Sync Output Low Delay	Input = 10% Duty Cycle	100		ns
t_{pdh1}	$\pm$ H Sync Input to $-$ H Sync Output High Delay	Input = 10% Duty Cycle	65		ns
t_{pd1}	$\pm$ H Sync Input Trailing Edge to Back Porch Clamp Output Delay	Input = 10% Duty Cycle, S2 = A	70		ns
t_{pd2}	Composite Video Input to $-$ H Sync Output Low Delay	Input = 10% Duty Cycle	106		ns
t_{pdh2}	Composite Video Input to $-$ H Sync Output High Delay	Input = 10% Duty Cycle	68		ns
t_{pd2}	Composite Video Input Trailing Edge to Back Porch Clamp Output Delay	Input = 10% Duty Cycle S2 = A	78		ns
$t_{pd2} - t_{pd1}$	Composite Video and $\pm$ H Sync Input to $-$ H Sync Output Delta Delay	Input = 10% Duty Cycle	6		ns

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur.

Note 2: Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 3: V_{CC} supply pins 2, 4, 6, 19, 31, 36, 41 and 44 must be externally wired together to prevent internal damage during V_{CC} power on/off cycle.

Note 4: Human body model, 100 pF discharged through a 1.5 k Ω resistor.

Note 5: Typical specifications are specified at +25°C and represent the most likely parametric norm.

Note 6: Tested limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 7: ΔA_V tracking is a measure of the ability of any two amplifiers to track each other and quantifies the matching of the three attenuators. It is the difference in gain change between any two amplifiers with the contrast voltage, V21, at either 4V or 2V measured relative to an A_V max condition V21 = 4V. For example, at A_V max, the three amplifier gains might be 17.4 dB, 16.9 dB and 16.4 dB and change to 7.3 dB, 6.9 dB and 6.5 dB respectively for V21 = 2V. This yields the measured typical ± 0.1 dB channel tracking.

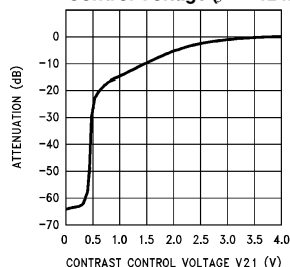
Note 8: Brightness tracking error is measured with all three video channels set for equal gain. The measured value is limited by the resolution of the measurement equipment.

Note 9: When measuring video amplifier bandwidth or pulse rise and fall times, a double sided full ground plane printed circuit board is recommended. Video amplifier isolation tests also require this printed circuit board. The measured rise and fall times are effective rise and fall times, taking into account the rise and fall times of the generator.

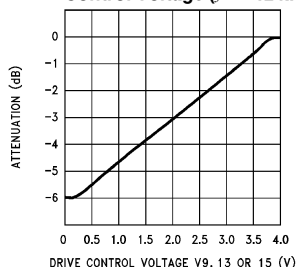
Note 10: Measure output levels of either undriven amplifier relative to the driven amplifier to determine channel isolation. Terminate the undriven amplifier inputs.

Typical Performance Characteristics $V_{CC} = 12V$, $T_A = 25^\circ C$ unless otherwise specified

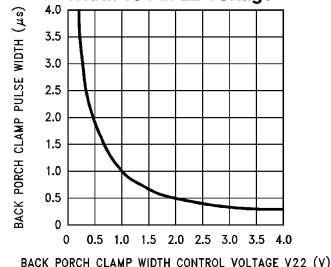
Attenuation vs Contrast Control Voltage ($f = 12\text{ kHz}$)



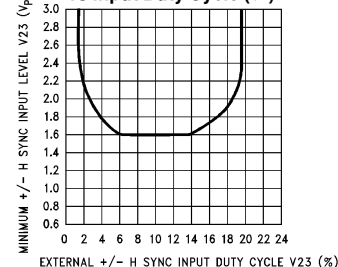
Attenuation vs Drive Control Voltage ($f = 12\text{ kHz}$)



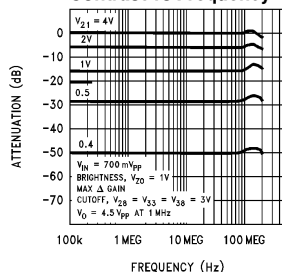
Back Porch Clamp Pulse Width vs Pin 22 Voltage



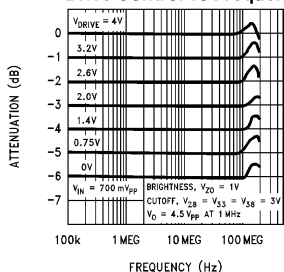
Minimum External $\pm H$ Sync Input Level (V_{pp}) vs Input Duty Cycle (%)



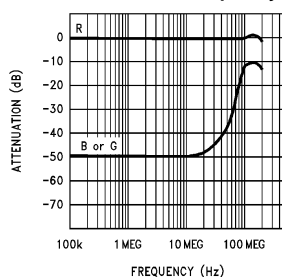
Contrast vs Frequency



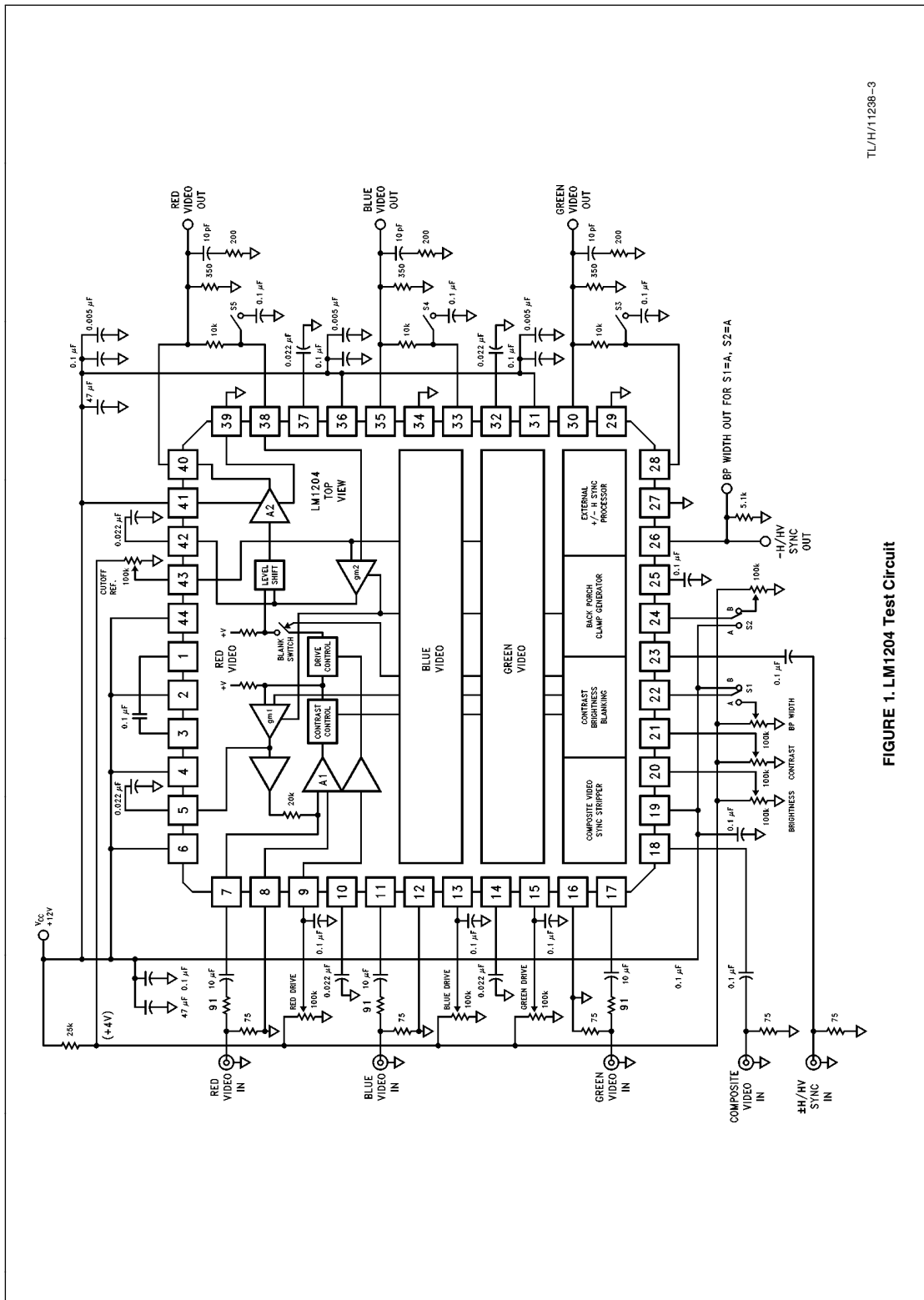
Drive Control vs Frequency



Crosstalk vs Frequency



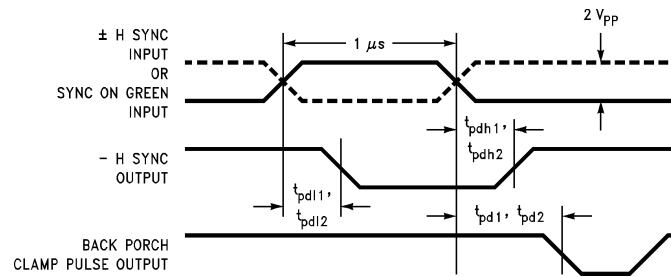
TL/H/11238-2



TL/H/11238-3

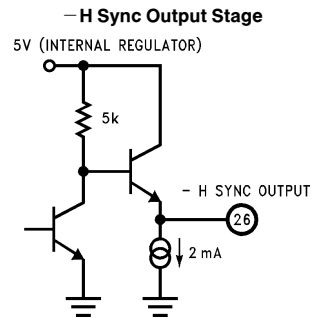
FIGURE 1. LM1204 Test Circuit

Timing Diagram

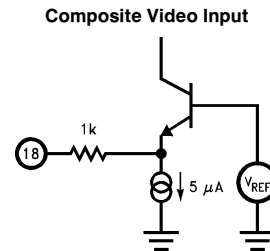


TL/H/11238-4

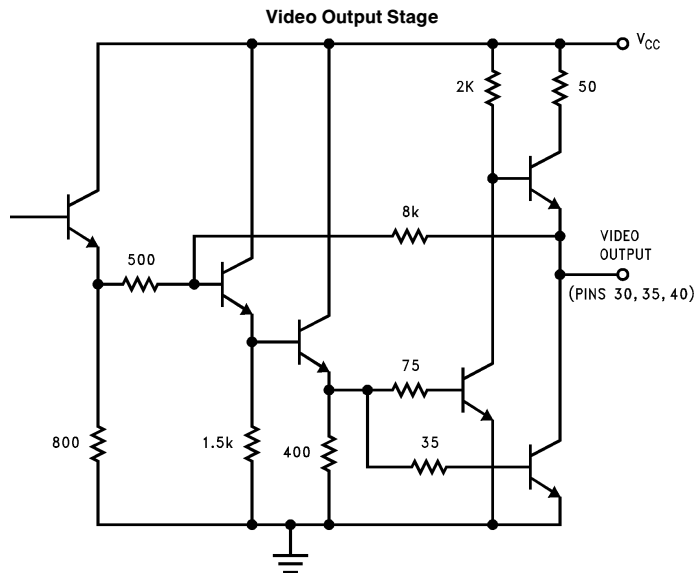
Input/Output Stages



TL/H/11238-5

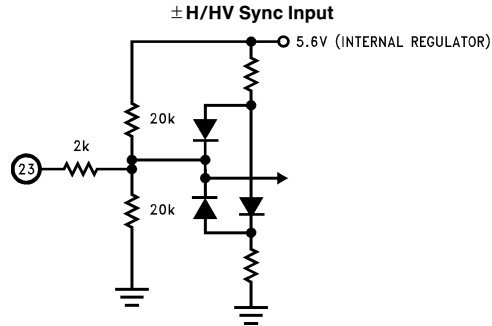


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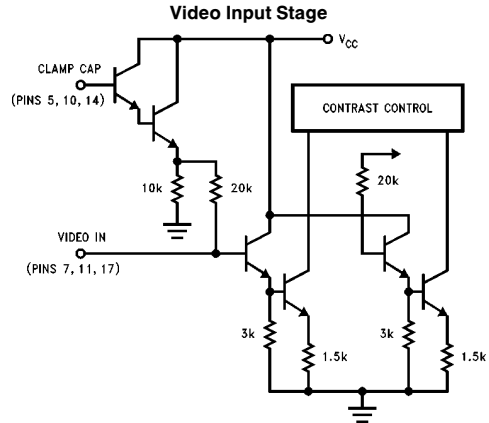


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Input/Output Stages (Continued)



TL/H/11238-7



TL/H/11238-8

Pin Descriptions

V_{CC} (Pins 2, 4, 6, 19, 31, 36, 41, 44)	All V_{CC} pins must be externally wired together. For stable operation, each supply pin should be bypassed with a 0.01 μF and a 0.1 μF capacitor connected as close to the pin as is possible.
Contrast Cap (Pins 1, 3)	An external decoupling capacitor of value 0.1 μF should be connected between pins 1 and 3 for contrast control.
R Clamp Cap (Pin 5)	A 0.022 μF to 0.1 μF capacitor should be connected from this pin to ground. This capacitor allows clamping of the red channel video signal to the reference black level.
B Clamp Cap (Pin 10)	A 0.022 μF to 0.1 μF capacitor should be connected from this pin to ground. This capacitor allows clamping of the blue channel video signal to the reference black level.
G Clamp Cap (Pin 14)	A 0.022 μF to 0.1 μF capacitor should be connected from this pin to ground. This capacitor allows clamping of the green channel video signal to the reference black level.
R Video In (Pin 7)	This is the input for the red channel video signal, the signal should be AC coupled to the input through a 10 μF capacitor.
B Video In (Pin 11)	This is the input for the blue channel video signal, the signal should be AC coupled to the input through a 10 μF capacitor.
G Video In (Pin 17)	This is the input for the green channel video signal, the signal should be AC coupled to the input through a 10 μF capacitor.
R Δ Gain (Pin 9)	This is the gain adjustment pin for the red video channel. A 0V to 4 V_{DC} voltage is applied to this pin to vary the gain of the red channel. Usually, the red channel is set for maximum gain and the gains of the blue and green channels are reduced relative to the red channel until white balance is achieved on the CRT screen.
B Δ Gain (Pin 13)	This is the gain adjustment pin for the blue video channel. A 0V to 4 V_{DC} voltage is applied to this pin to vary the gain of the blue channel.
G Δ Gain (Pin 15)	This is the gain adjustment pin for the green video channel. A 0V to 4 V_{DC} voltage is applied to this pin to vary the gain of the green channel.
Compose Video Input (Pin 18)	This is the sync separator input pin. For Sync on Green systems, the green channel video signal should be AC coupled to pin 18 through a 0.1 μF capacitor.
Brightness Control (Pin 20)	If the LM1204 is used without blanking then this pin should be biased at 2.0 V_{DC} . Brightness control for all three video channels is now controlled by pin 43 (blank level adjust pin). See Figure 4. If the LM1204 is used with blanking then this pin allows the user to simultaneously DC offset the video portion of the output signals of all three channels thus allowing brightness control (See Figure 5).
Contrast Control (Pin 21)	This pin simultaneously controls the gain of all three video channels. A 0V to 4 V_{DC} input voltage is applied to this pin, with 0V corresponding to minimum gain (i.e., maximum attenuation of video signal) and 4V corresponding to maximum gain (i.e., minimum attenuation of the video signal).

Pin Descriptions (Continued)

Back Porch Clamp Width Adjust (Pin 22)	The LM1204 provides DC restoration or clamping during the back porch interval of the video signal. The width of LM1204's internally generated back porch clamp signal can be varied by applying a 0V to 4 V _{DC} voltage to this pin. The back porch clamp signal width can be varied from approximately 0.3 μ s to 4.0 μ s by applying 4V to 0.5V respectively. By connecting the blank gate input pin (pin 24) to V _{CC} , the back porch clamp pulse can be monitored on the $\pm$ H Sync output pin (pin 26). See <i>Figures 4 and 5</i> . By connecting pin 22 to V _{CC} , the LM1204 functions as a non-gated amplifier requiring no clamping. See Section 4 under application hints for further information.
$\pm$ H Sync In (Pin 23)	This is the external sync input pin, it accepts a negative or positive polarity signal, either horizontal sync or a composite sync (1.2 V _{PP} minimum amplitude). The LM1204 also provides a negative polarity (TTL compatible) horizontal sync or composite sync output on pin 26. If the composite video input (pin 18) is not used then an H Sync signal should be AC coupled to this pin through a 0.1 μ F capacitor. The $\pm$ H Sync input has priority over the composite video input if both signals are present.
Blank Gate In (Pin 24)	This is the blank gate input pin. The LM1204 allows video blanking at the preamplifier. If blanking is desired then a TTL compatible, negative polarity blanking signal should be applied to this pin. During the blanking interval, all three video outputs are level shifted to the blank level set by the voltage at pin 43. If blanking is not required then, pin 24 should be biased at 4V. Connecting pin 24 to V _{CC} will cause pin 26 to output the internally generated back porch clamp signal. The user can observe the change in back porch width as the potential at pin 22 is varied (see <i>Figures 4 and 5</i>).
Integrator Cap (Pin 25)	A 0.1 μ F capacitor should be connected from this pin to ground. This capacitor allows the LM1204 to integrate the $\pm$ H Sync input signal and generate the proper polarity switch for $\pm$ H Sync output.
$\pm$ H Sync Out (Pin 26)	This output pin provides a negative polarity horizontal sync signal for other system uses. There is approximately 100 ns delay between the $\pm$ H Sync input signal at pin 23 and the $\pm$ H Sync output signal at pin 26. Connecting pin 24 to V _{CC} will cause pin 26 to output the internally generated back porch clamp signal. The user can observe the change in back porch clamp pulse width as the potential at pin 22 is varied (See <i>Figures 4 and 5</i>).
G Feedback (Pin 28)	This is the cutoff adjustment input for the green video channel. The green video output signal from pin 30 is fed back to this input through a potentiometer thus allowing the user to individually adjust the cutoff (black reference) level for each gun. The signal level at this pin should be between 0.5V and 4V.
B Feedback (Pin 33)	This is the cutoff adjustment input for the blue video channel. The blue video output signal from pin 35 is fed back to this input through a potentiometer thus allowing the user to individually adjust the cutoff (black reference) level for each gun. The signal level at this pin should be between 0.5V and 4V.
R Feedback (Pin 38)	This is the cutoff adjustment input for the red video channel. The red video output signal from pin 40 is fed back to this input through a potentiometer thus allowing the user to individually adjust the cutoff (black reference) level for each gun. The signal level at this pin should be between 0.5V and 4V.
G Video Output (Pin 30)	This is the green channel video output.
B Video Output (Pin 35)	This is the blue channel video output.
R Video Output (Pin 40)	This is the red channel video output.
G Blank Clamp Cap (Pin 32)	A 0.022 μ F to 0.1 μ F capacitor should be connected from this pin to ground. This capacitor allows blanking for the green video channel.
B Blank Clamp Cap (Pin 37)	A 0.022 μ F to 0.1 μ F capacitor should be connected from this pin to ground. This capacitor allows blanking for the blue video channel.
R Blank Clamp Cap (Pin 42)	A 0.022 μ F to 0.1 μ F capacitor should be connected from this pin to ground. This capacitor allows blanking for the red video channel.
Blank Level Adjust (Pin 43)	This pin serves two functions depending on whether the LM1204 is used with blanking or without blanking. If blanking is not selected then pin 20 should be biased at 2.0 V _{DC} and pin 43 assumes the role of brightness control. Varying the potential at pin 43 will simultaneously DC offset the video output signals of all three channels (See <i>Figure 4</i>). If the LM1204 is used with blanking then during the blanking interval, all three video output signals will be level shifted to the blank level. The desired blank level can be set by adjusting the potential at pin 43. Brightness control is now made possible by varying the potential at pin 20. Adjusting the brightness control DC offsets the video portion of the signal relative to the fixed blank level (all channels are affected simultaneously). See <i>Figure 5</i> .
GND (Pins 8, 12 16, 27, 29, 34, 39)	Ground. All ground pins must be connected to the ground plane.

Applications Hints

The LM1204 is a wideband video amplifier system designed specifically for high resolution RGB CRT monitors. The device includes circuitry for DC restoration of video signals and also allows contrast and brightness control. DC restoration is done during the back porch interval of the video signal. An internal sync separator generates a back porch clamp signal either from a "Sync on Green" signal applied to the composite video input (pin 18) or from an externally supplied $\pm H$ Sync signal. The LM1204 first looks at the $\pm H$ Sync input (pin 23), if an external horizontal sync signal is not present then the device syncs off the composite video input. The internally generated back porch clamp pulse width is user adjustable.

A blanking function is also included. This allows the user to cutoff the beam current in the CRT's guns during the blanking interval thereby preventing horizontal retrace lines from being visible. Normally blanking is done by applying a high voltage pulse at the grid. However, blanking at the cathode using the LM1204 leads to ease of design and lowered cost.

Figure 2 shows the block diagram of the green video channel and the control logic. The two modes of operation, with and without blanking, are described below in detail.

1.0 Operation without Blanking

For operation without blanking, the blank gate input (pin 24) should be connected to +4V. This causes the blank comparator to connect switch S2 to position Y (See Figure 2).

Furthermore, the brightness control input pin (pin 20) should be biased at a potential between 1V (Min) and 3.8V (Max), it is best to bias this pin at 2V. The video signal is AC coupled to the input of the LM1204 as shown for the green channel in Figure 2. During the back porch interval of the video signal (See Figure 3), the internally generated back porch clamping pulse goes low, causing switches S1A and S1B to be closed. The closure of S1A causes g_{m1} to charge capacitor C2 to a potential determined by the DC voltage at pin 20. This allows g_{m1} to set up an average DC bias for the AC coupled video signal at the input of A1. When the back porch clamping pulse is high, S1A and S1B are opened. With S1A open, g_{m1} is effectively disconnected from C2, C2 now holds the DC bias voltage. The transconductance stage g_{m1} therefore functions as a sample and hold device and holds the input of A1 at the desired DC bias.

The LM1204 uses black level clamping at the back porch of the video signal to accomplish DC restoration. The transconductance stage g_{m2} is enabled during the back porch clamp period to provide a sample and hold function. During the back porch clamp period, DC feedback from LM1204's video output is compared with the voltage set by potentiometer R9. Depending on A2's output voltage, C6 is either charged or discharged so that the feedback loop consisting of g_{m2} and A2 is stabilized and the output is clamped to the black level. All this occurs during the back porch clamp period. During the video portion of the signal, g_{m2} is disabled and C6 holds the fixed black level reference voltage. The beginning of each new line on the raster always starts from a fixed reference black level thus restoring the DC component of each line.

A2 is a summing amplifier that adds a DC offset component from g_{m2} to the video signal from the multiplier. Adjusting R9 will DC offset the output signals of all three channels thus providing brightness control. Individual cutoff adjust-

ment for each channel is done by varying the feedback voltage at each of the R, G and B feedback inputs (Pins 38, 28 and 33). For example, cutoff adjustment for the green channel is done by potentiometer R8 shown in Figure 2.

Adjusting the contrast control (potentiometer R3 in Figure 2) varies the peak to peak amplitude (includes sync tip if present) of all three video output signals relative to their black reference level. The Δ Gain adjust (pins 9, 15 and 13 for R, G, and B channels respectively) allows the user to individually adjust the AC gain of each channel. For example the AC gain of the green channel is adjusted using potentiometer R5 as shown in Figure 2. Normally the red channel is set for maximum gain and the gains of the blue and green channels are reduced until white balance is achieved on the CRT monitor's screen. Figure 4 shows the adjustments for operation without blanking.

2.0 Operation with Blanking

Much of what was discussed in Section 1.0 also applies when the LM1204 is used with the blanking function. However, there are notable differences as described herein. For operation with blanking, a TTL compatible blanking signal must be applied to the blank gate input (pin 24).

During the blanking period, the blanking comparator connects switch S2 to position X (See Figure 2). This causes the LM1204 to level shift the video output signal to the blank level. Adjusting R9 will adjust the blank level of all three channels. Individual blank level adjustment for each channel is done by varying the feedback voltage at each of the R, G and B feedback inputs (pin 38, 28 and 33). In Figure 2 this is done by adjusting potentiometer R8 for the green channel.

During the video portion of the video signal, S2 is connected to position Y. Brightness control is now accomplished by varying the potential at the brightness control pin (pin 20). Adjusting R6 offsets the video portion of all three output signals relative to the fixed blank level, restoring the DC level of the video signal. Figure 5 shows the adjustments for operation with blanking.

3.0 Stability Considerations

For optimum performance and stable operation, a double sided PC board with adequate ground plane is essential. Moreover, soldering the LM1204 on to the PC board will yield best results. Each supply pin (pins 2, 4, 6, 19, 31, 36, 41 and 44) should be bypassed with a 0.01 μF and a 0.1 μF capacitor connected as close to the supply pin as is possible.

When driving the LM1204 from a 75 Ω video source, the cable is terminated with 75 Ω to minimize reflections caused by transmission line effects. However, the input impedance of LM1204 is capacitive and is also affected by the stray capacitance of the PC board. Thus the input impedance is a function of frequency. This changes the impedance of the cable termination. This can introduce overshoot and ringing in LM1204's pulse response. A 100 Ω resistor in series with the blocking capacitor at the video input will minimize overshoot and ringing (see Figure 8). The value of the resistor is empirically determined. 100 Ω is a good starting value.

Since the LM1204 is a wide bandwidth amplifier with high gain at high frequencies, the device may oscillate when driving a large capacitive/inductive load. To prevent oscillation, the amplifier's gain is rolled off at high frequencies. This is accomplished by an RC network comprised of a resistor in

3.0 Stability Considerations (Continued)

series with a capacitor connected from the video output pin to ground (see Test Circuit, *Figure 1*). A 110Ω to 200Ω resistor in series with 10 pF is quite adequate for most applications. However, if oscillations don't cease then the value of the resistor should be decreased or the value of the capacitor should be increased or a combination of the two.

LM1204

Non-Gated High Frequency Application

By connecting the back porch width adjust pin (pin 22) to V_{CC} , the LM1204 functions as a non-gated amplifier requiring no sync or blanking signals. *Figure 9* shows a triple high frequency amplifier with variable gain and DC offset control. In this mode of operation, filtered DC feedback must be provided to pins 28, 33 and 38 as shown in *Figure 9*.

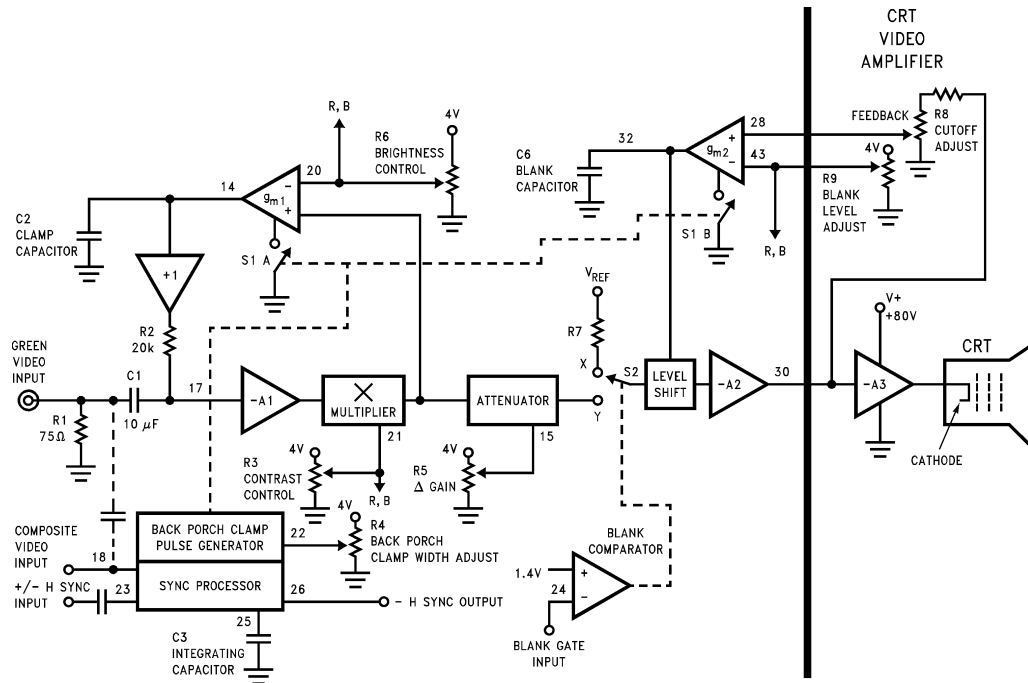


FIGURE 2. Block Diagram Showing Timing Circuitry and Green Video Channel

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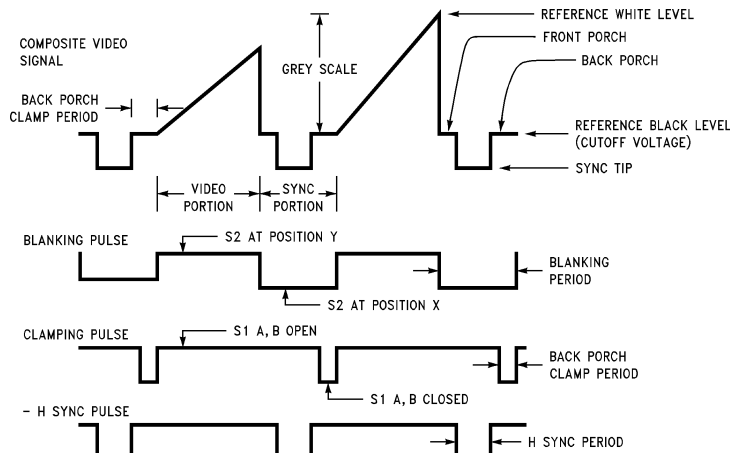
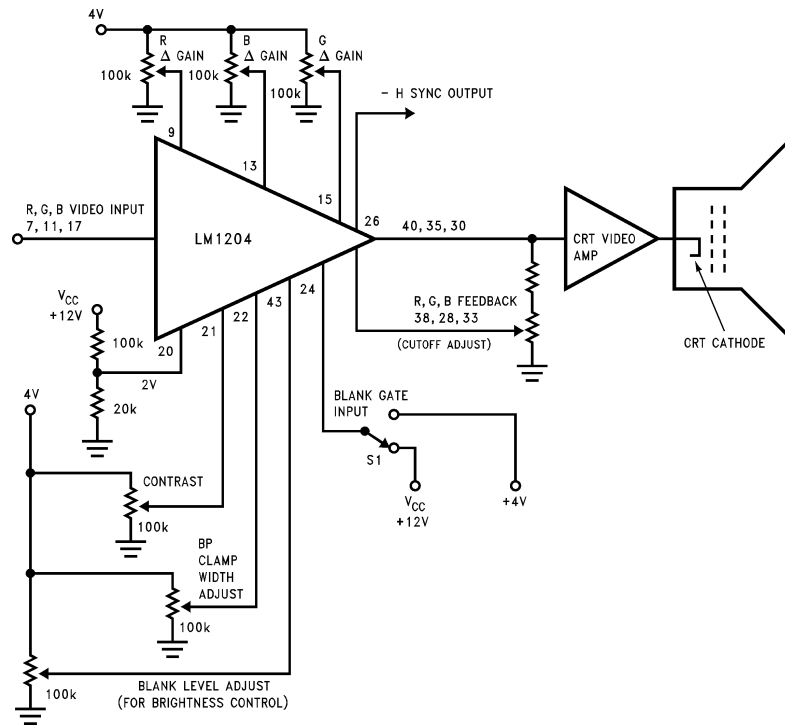
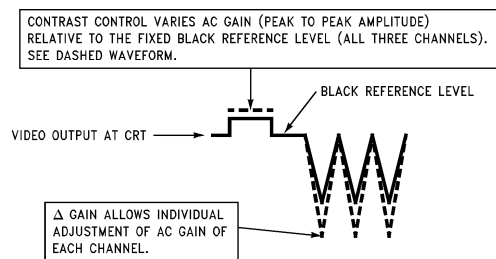


FIGURE 3. Composite Video and Timing Signals

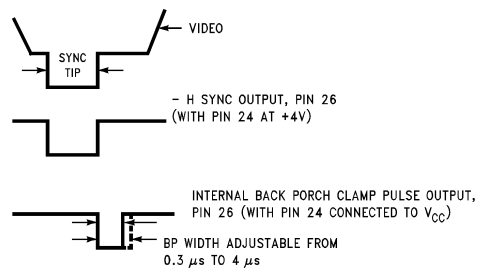
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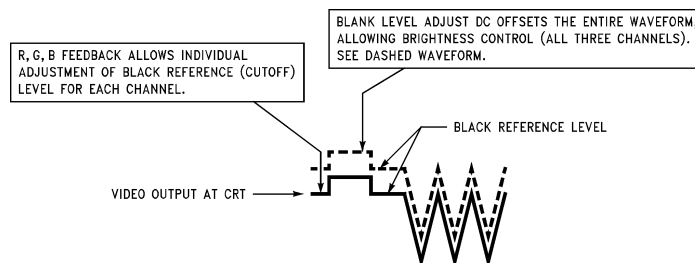
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TL/H/11238-13



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FIGURE 4. LM1204 Adjustments without Blanking

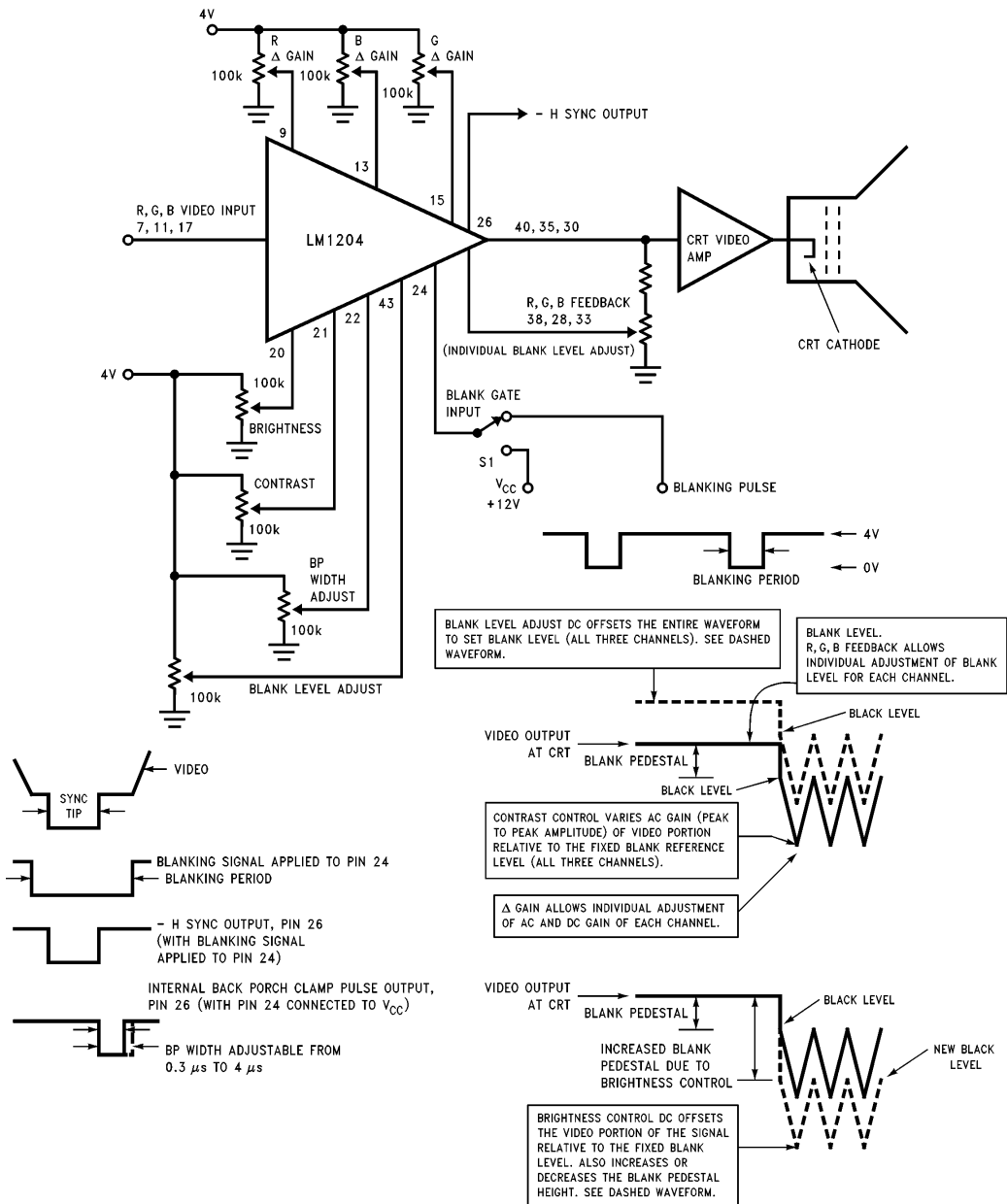


FIGURE 5. LM1204 Adjustments with Blanking

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Typical Applications Circuits

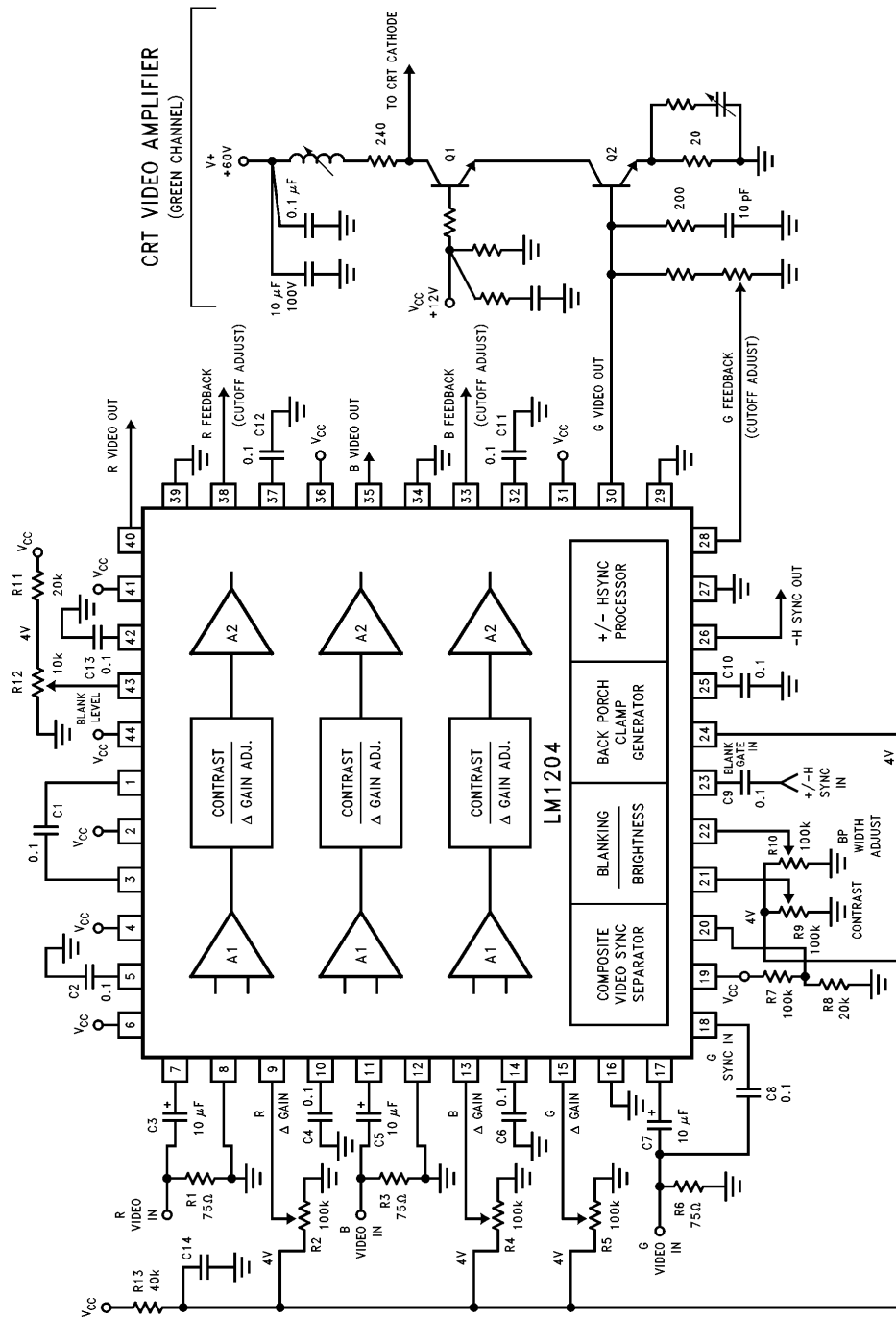
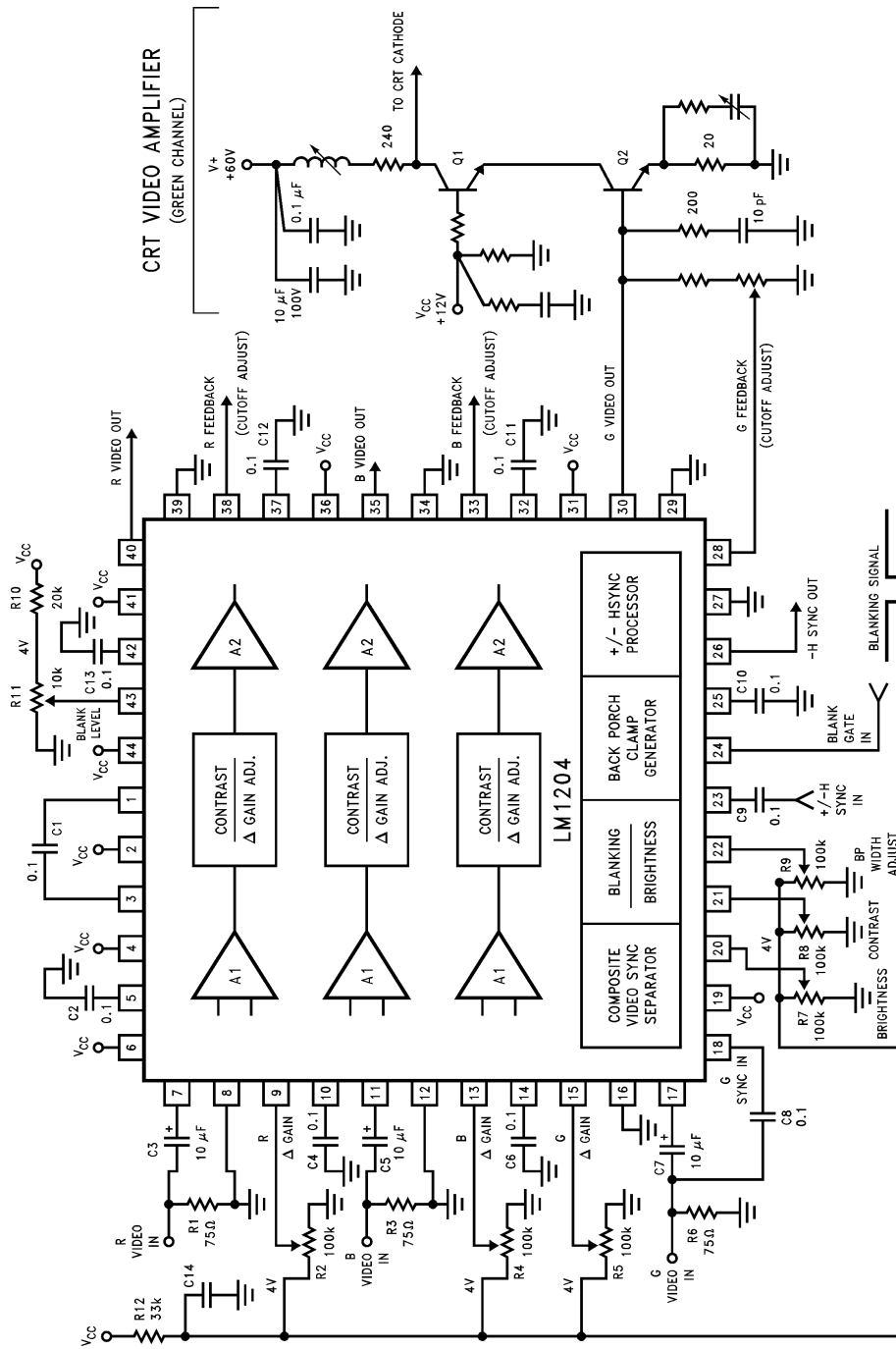


FIGURE 6. The LM1204 driving cascade CRT video amplifiers and operating without blanking. Brightness control is accomplished by potentiometer R12 (See Figure 4 for explanation of adjustments). Each V_{CC} pin should be bypassed with a $0.01 \mu F$ and a $0.1 \mu F$ capacitor connected as close to the pin as is possible.

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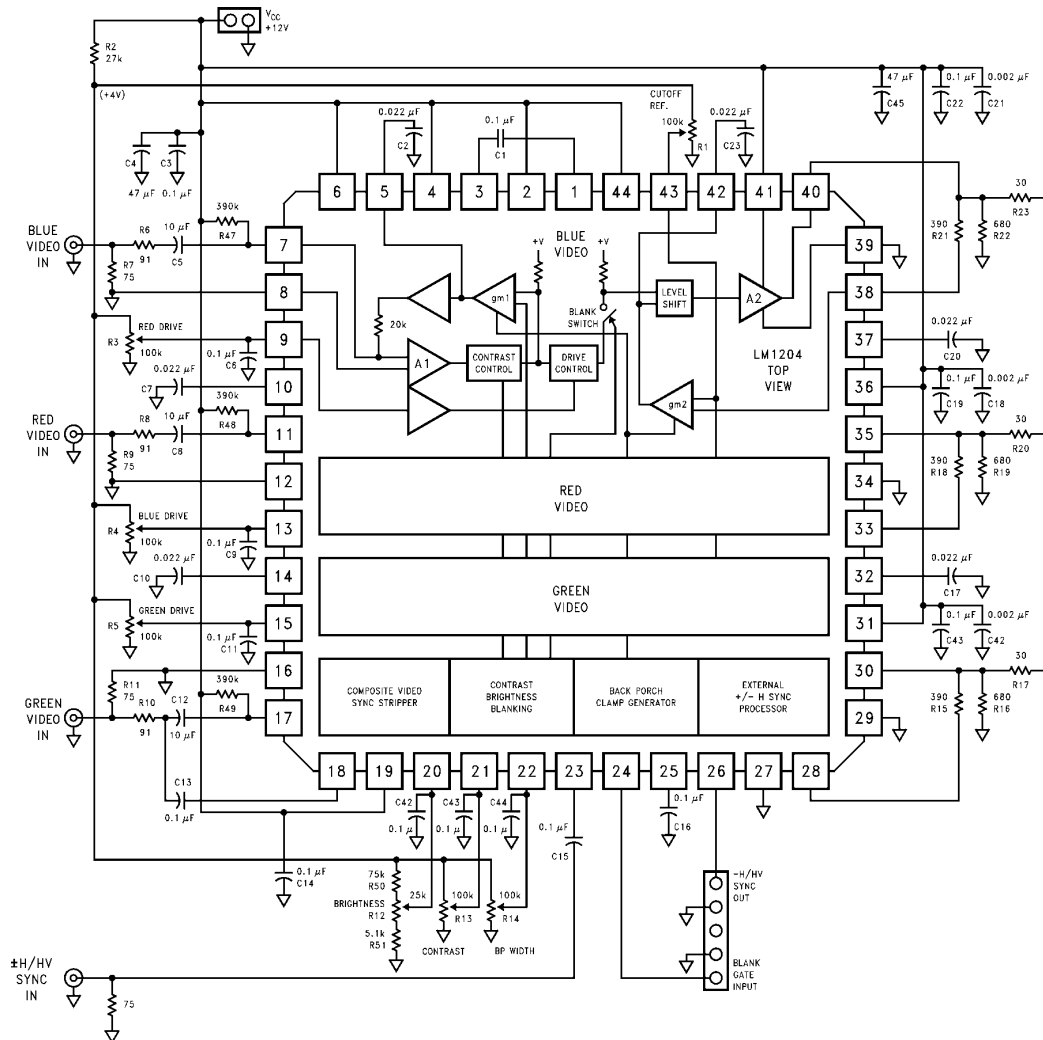
Typical Applications Circuits (Continued)



TL/H/11238-17

FIGURE 7. The LM1204 driving cascade CRT video amplifiers and operating with blanking. The video signal is level shifted to the user adjustable blank level during the blanking period. Brightness control DC offsets the video signal relative to the fixed blank level and is accomplished by potentiometer R7. See Figure 5 for explanation of adjustments. Each Vcc pin should be bypassed with a 0.01 μ F and a 0.1 μ F capacitor connected as close to the pin as is possible.

Typical Applications Circuits (Continued)



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FIGURE 8. Complete circuitry for an RGB CRT video board using the LM1204 and LH2426AS.
The video output signals from LH2426AS are AC coupled and diode clamped to greater than 80V.

The schematic diagram illustrates the internal wiring of the LH2426AS CRT socket driver circuit. The circuit is powered by +120V and +80V lines. It features 12 pins for the LH2426AS tube, each with a specific internal connection and external component network. The circuit includes various resistors (R24-R46), capacitors (C24-C39), diodes (D1-D6), and a heater (6.34V). Grounding points for FBT, CRT, and CRT SOCKET are indicated. The diagram is labeled with component values and pin numbers.

Component Values:

- Resistors: R24, R25, R26, R27, R28, R29, R30, R31, R32, R33, R34, R35, R36, R37, R38, R39, R40, R41, R42, R43, R44, R45, R46.
- Capacitors: C24, C25, C26, C27, C28, C29, C30, C31, C32, C33, C34, C35, C36, C37, C38, C39.
- Diodes: D1, D2, D3, D4, D5, D6.
- Heater: 6.34V.

Pin Connections:

- Pin 1: +120V, 10k R40, 1k R39, 10 μF C32, 0.1 μF C31, 56 pF C29, 300k R32, 0.1 μF C30, 56 pF C28, 300k R29, 0.1 μF C27, 56 pF C26, 300k R27, 0.1 μF C25, 56 pF C24, 300k R24, 0.1 μF C23, 56 pF C22, 300k R21, 0.1 μF C20, 56 pF C19, 300k R18, 0.1 μF C17, 56 pF C16, 300k R15, 0.1 μF C14, 56 pF C13, 300k R12, 0.1 μF C11, 56 pF C10, 300k R9, 0.1 μF C8, 56 pF C7, 300k R6, 0.1 μF C5, 56 pF C4, 300k R3, 0.1 μF C3, 56 pF C2, 300k R1.
- Pin 2: +80V, 10k R44, 1k R43, 10 μF C38, 1 μF C37, 1 μF C36, 1 μF C35, 1 μF C34, 1 μF C33, 1 μF C32, 1 μF C31, 1 μF C30, 1 μF C29, 1 μF C28, 1 μF C27, 1 μF C26, 1 μF C25, 1 μF C24, 1 μF C23, 1 μF C22, 1 μF C21, 1 μF C20, 1 μF C19, 1 μF C18, 1 μF C17, 1 μF C16, 1 μF C15, 1 μF C14, 1 μF C13, 1 μF C12, 1 μF C11, 1 μF C10, 1 μF C9, 1 μF C8, 1 μF C7, 1 μF C6, 1 μF C5, 1 μF C4, 1 μF C3, 1 μF C2, 1 μF C1.
- Pin 3: 10k R40, 1k R39, 10 μF C32, 0.1 μF C31, 56 pF C29, 300k R32, 0.1 μF C30, 56 pF C28, 300k R29, 0.1 μF C27, 56 pF C26, 300k R27, 0.1 μF C25, 56 pF C24, 300k R24, 0.1 μF C23, 56 pF C22, 300k R21, 0.1 μF C20, 56 pF C19, 300k R18, 0.1 μF C17, 56 pF C16, 300k R15, 0.1 μF C14, 56 pF C13, 300k R12, 0.1 μF C11, 56 pF C10, 300k R9, 0.1 μF C8, 56 pF C7, 300k R6, 0.1 μF C5, 56 pF C4, 300k R3, 0.1 μF C3, 56 pF C2, 300k R1.
- Pin 4: 10k R44, 1k R43, 10 μF C38, 1 μF C37, 1 μF C36, 1 μF C35, 1 μF C34, 1 μF C33, 1 μF C32, 1 μF C31, 1 μF C30, 1 μF C29, 1 μF C28, 1 μF C27, 1 μF C26, 1 μF C25, 1 μF C24, 1 μF C23, 1 μF C22, 1 μF C21, 1 μF C20, 1 μF C19, 1 μF C18, 1 μF C17, 1 μF C16, 1 μF C15, 1 μF C14, 1 μF C13, 1 μF C12, 1 μF C11, 1 μF C10, 1 μF C9, 1 μF C8, 1 μF C7, 1 μF C6, 1 μF C5, 1 μF C4, 1 μF C3, 1 μF C2, 1 μF C1.
- Pin 5: 10k R40, 1k R39, 10 μF C32, 0.1 μF C31, 56 pF C29, 300k R32, 0.1 μF C30, 56 pF C28, 300k R29, 0.1 μF C27, 56 pF C26, 300k R27, 0.1 μF C25, 56 pF C24, 300k R24, 0.1 μF C23, 56 pF C22, 300k R21, 0.1 μF C20, 56 pF C19, 300k R18, 0.1 μF C17, 56 pF C16, 300k R15, 0.1 μF C14, 56 pF C13, 300k R12, 0.1 μF C11, 56 pF C10, 300k R9, 0.1 μF C8, 56 pF C7, 300k R6, 0.1 μF C5, 56 pF C4, 300k R3, 0.1 μF C3, 56 pF C2, 300k R1.
- Pin 6: 10k R44, 1k R43, 10 μF C38, 1 μF C37, 1 μF C36, 1 μF C35, 1 μF C34, 1 μF C33, 1 μF C32, 1 μF C31, 1 μF C30, 1 μF C29, 1 μF C28, 1 μF C27, 1 μF C26, 1 μF C25, 1 μF C24, 1 μF C23, 1 μF C22, 1 μF C21, 1 μF C20, 1 μF C19, 1 μF C18, 1 μF C17, 1 μF C16, 1 μF C15, 1 μF C14, 1 μF C13, 1 μF C12, 1 μF C11, 1 μF C10, 1 μF C9, 1 μF C8, 1 μF C7, 1 μF C6, 1 μF C5, 1 μF C4, 1 μF C3, 1 μF C2, 1 μF C1.
- Pin 7: 10k R40, 1k R39, 10 μF C32, 0.1 μF C31, 56 pF C29, 300k R32, 0.1 μF C30, 56 pF C28, 300k R29, 0.1 μF C27, 56 pF C26, 300k R27, 0.1 μF C25, 56 pF C24, 300k R24, 0.1 μF C23, 56 pF C22, 300k R21, 0.1 μF C20, 56 pF C19, 300k R18, 0.1 μF C17, 56 pF C16, 300k R15, 0.1 μF C14, 56 pF C13, 300k R12, 0.1 μF C11, 56 pF C10, 300k R9, 0.1 μF C8, 56 pF C7, 300k R6, 0.1 μF C5, 56 pF C4, 300k R3, 0.1 μF C3, 56 pF C2, 300k R1.
- Pin 8: 10k R44, 1k R43, 10 μF C38, 1 μF C37, 1 μF C36, 1 μF C35, 1 μF C34, 1 μF C33, 1 μF C32, 1 μF C31, 1 μF C30, 1 μF C29, 1 μF C28, 1 μF C27, 1 μF C26, 1 μF C25, 1 μF C24, 1 μF C23, 1 μF C22, 1 μF C21, 1 μF C20, 1 μF C19, 1 μF C18, 1 μF C17, 1 μF C16, 1 μF C15, 1 μF C14, 1 μF C13, 1 μF C12, 1 μF C11, 1 μF C10, 1 μF C9, 1 μF C8, 1 μF C7, 1 μF C6, 1 μF C5, 1 μF C4, 1 μF C3, 1 μF C2, 1 μF C1.
- Pin 9: 10k R40, 1k R39, 10 μF C32, 0.1 μF C31, 56 pF C29, 300k R32, 0.1 μF C30, 56 pF C28, 300k R29, 0.1 μF C27, 56 pF C26, 300k R27, 0.1 μF C25, 56 pF C24, 300k R24, 0.1 μF C23, 56 pF C22, 300k R21, 0.1 μF C20, 56 pF C19, 300k R18, 0.1 μF C17, 56 pF C16, 300k R15, 0.1 μF C14, 56 pF C13, 300k R12, 0.1 μF C11, 56 pF C10, 300k R9, 0.1 μF C8, 56 pF C7, 300k R6, 0.1 μF C5, 56 pF C4, 300k R3, 0.1 μF C3, 56 pF C2, 300k R1.
- Pin 10: 10k R44, 1k R43, 10 μF C38, 1 μF C37, 1 μF C36, 1 μF C35, 1 μF C34, 1 μF C33, 1 μF C32, 1 μF C31, 1 μF C30, 1 μF C29, 1 μF C28, 1 μF C27, 1 μF C26, 1 μF C25, 1 μF C24, 1 μF C23, 1 μF C22, 1 μF C21, 1 μF C20, 1 μF C19, 1 μF C18, 1 μF C17, 1 μF C16, 1 μF C15, 1 μF C14, 1 μF C13, 1 μF C12, 1 μF C11, 1 μF C10, 1 μF C9, 1 μF C8, 1 μF C7, 1 μF C6, 1 μF C5, 1 μF C4, 1 μF C3, 1 μF C2, 1 μF C1.
- Pin 11: 10k R40, 1k R39, 10 μF C32, 0.1 μF C31, 56 pF C29, 300k R32, 0.1 μF C30, 56 pF C28, 300k R29, 0.1 μF C27, 56 pF C26, 300k R27, 0.1 μF C25, 56 pF C24, 300k R24, 0.1 μF C23, 56 pF C22, 300k R21,

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Typical Applications Circuits (Continued)

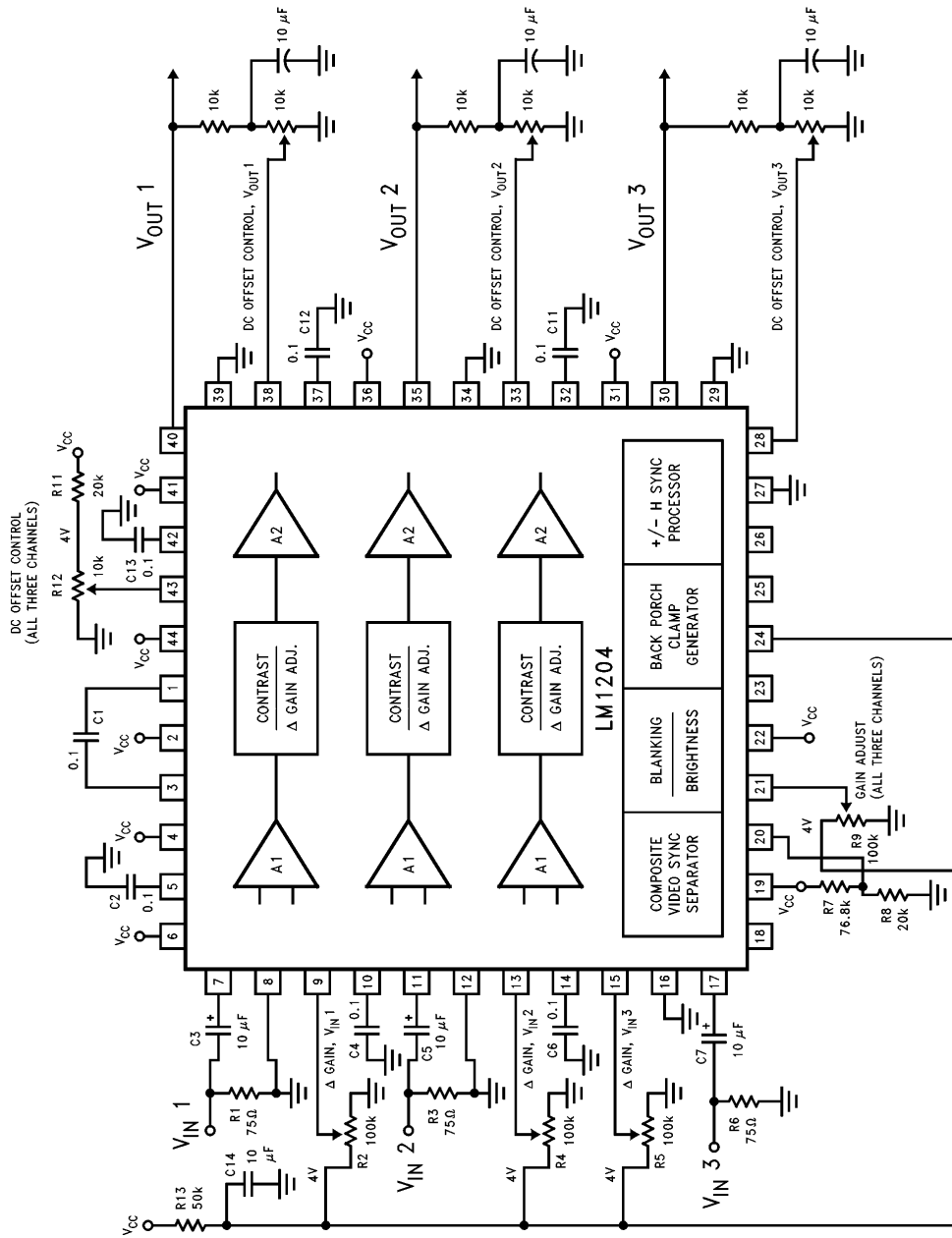
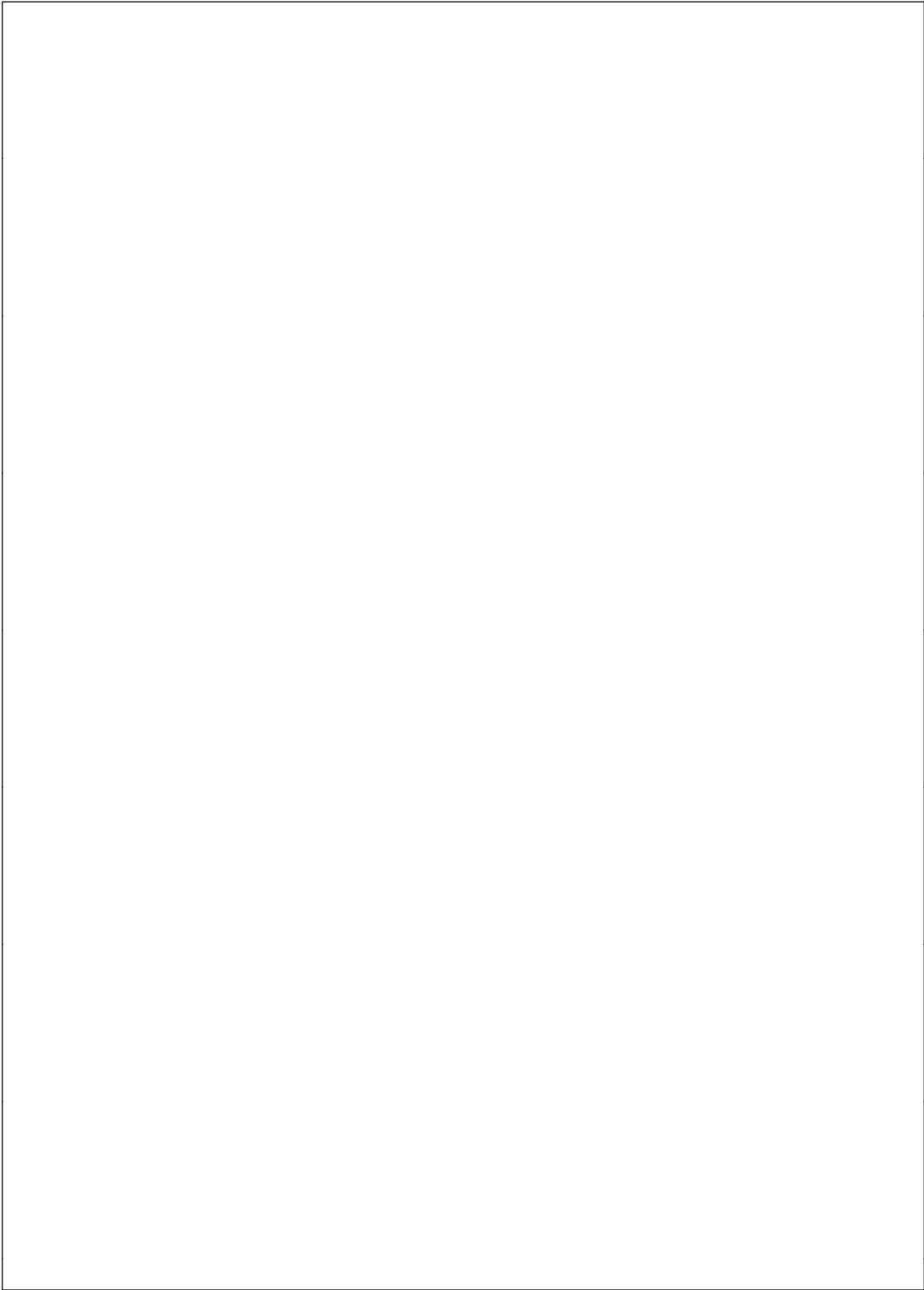
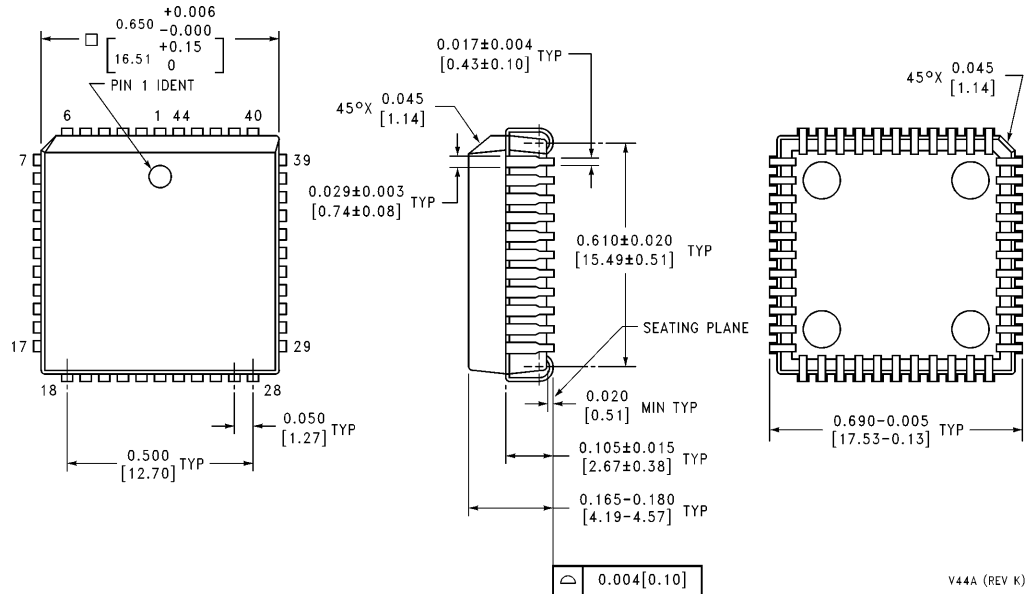


FIGURE 9. Three channel high frequency amplifier with gain and DC offset control (non-video application). Each VCC pin should be bypassed with a 0.01 μF and a 0.1 μF capacitor connected as close to the pin as is possible.



Physical Dimensions inches (millimeters)



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