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National Semiconductor

LM1246
150 MHz I²C Compatible RGB Preamplifier with Internal 512 Character OSD ROM, 512 Character RAM and 4 DACs

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General Description

The LM1246 pre-amp is an integrated CMOS CRT preamp. It has an I²C compatible interface which allows control of all the parameters necessary to directly setup and adjust the gain and contrast in the CRT display. Brightness and bias can be controlled through the DAC outputs, which are well matched to the LM2479 and LM2480 integrated bias clamp ICs. The LM1246 preamp is also designed to be compatible with the LM246x high gain driver family.

Black level clamping of the video signal is carried out directly on the AC coupled input signal into the high impedance preamplifier input, thus eliminating the need for additional clamp capacitors. Horizontal and vertical blanking of the outputs is provided. Vertical blanking is optional and its duration is register programmable.

The IC is packaged in an industry standard 24-lead DIP molded plastic package.

Features

- **Fully addressable 512 Character OSD, simiilar in features to the LM1237/LM1247, with selectable 2 byte character addressing or LM1247 bank select modes**
- Internal 512 character OSD ROM usable as either (a) 384 2-color plus 128 4-color characters, (b) 640 2-color characters, or (c) some combination in between
- Internal 512 character RAM, which can be displayed as one single or two independent windows
- **Enhanced I²C compatible microcontroller interface to allow versatile Page RAM access**
- **OSD Window Fade In/Fade Out**
- **OSD Half Tone Transparency**
- Video Data dectection for **Auto Centering & Sizing**
- OSD override allows OSD messages to override video and the use of burn-in screens with no video output.
- 4 DAC outputs (8-bit resolution) for bus controlled CRT bias and brightness
- Spot killer which blanks the video outputs when V_{CC} falls below the specified threshold
- Suitable for use with discrete or integrated clamp, with software configurable brightness mixer
- **4-Bit Programmable start position for internal Horizontal Blanking**
- Horizontal blanking and OSD synchronization directly from deflection signals. The blanking can be disabled, if desired.
- Vertical blanking and OSD synchronization directly from deflection signals. The blanking width is register programmable and can be disabled, if desired.
- Power Saving Mode with 65% power reduction
- Matched to LM246x driver and LM2479/80 bias IC's

Applications

- Low end 15" and 17" bus controlled monitors with OSD
- 1024x768 displays up to 85 Hz requiring OSD capability
- Very low cost systems with LM246x driver

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Internal Block Diagram

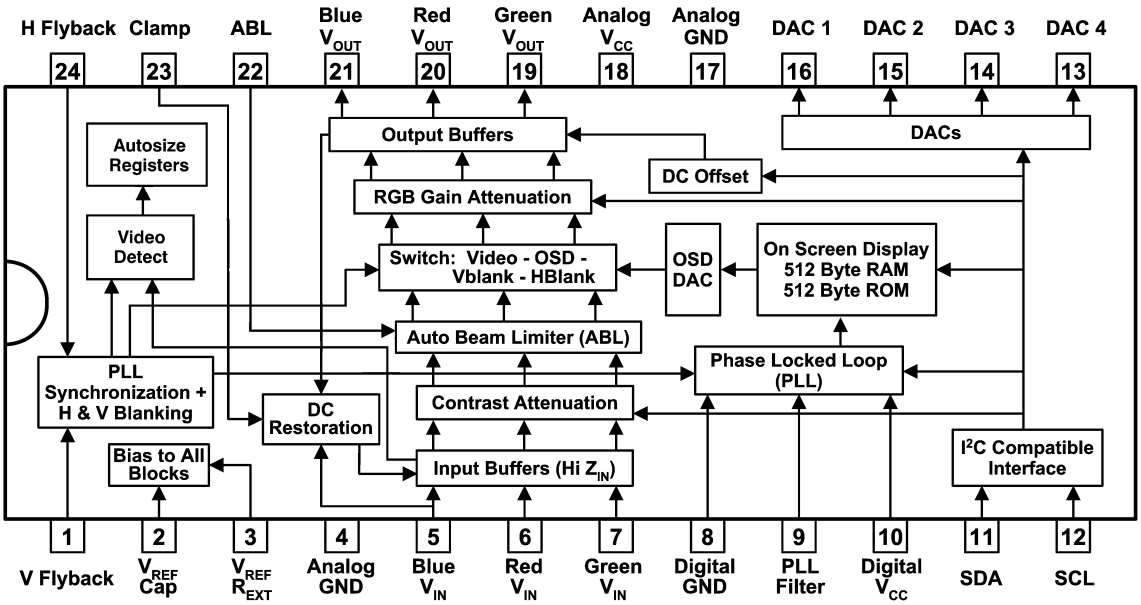

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FIGURE 1. Order Number LM1246AAA/NA
See NS Package Number N24D

Absolute Maximum Ratings (Notes 1, 3)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage V_{CC}, Pins 10 and 18	6.0V
Peak Video DC Output Source Current (Any One Amp) Pins 19, 20 or 21	1.5 mA
Voltage at Any Input Pin (V_{IN})	V_{CC} +0.5 ≥ V_{IN} ≥ −0.5V
Video Inputs (pk-pk)	0.0 ≤ V_{IN} ≤ 1.2V
Thermal Resistance to Ambient (θ_{JA})	51˚C/W
Power Dissipation (P_D) (Above 25˚C Derate Based on θ_{JA} and T_J)	2.4W
Thermal Resistance to Case (θ_{JC})	32˚C/W
Junction Temperature (T_J)	150˚C
ESD Susceptibility (Note 4)	3.0 kV
ESD Machine Model (Note 13)	350V
Storage Temperature	−65˚C to +150˚C
Lead Temperature (Soldering, 10 sec.)	265˚C

Operating Ratings (Note 2)

Temperature Range	0˚C to +70˚C
Supply Voltage V_{CC}	4.75V ≤ V_{CC} ≤ 5.25V
Video Inputs (pk-pk)	0.0V ≤ V_{IN} ≤ 1.0V

Video Signal Electrical Characteristics

Unless otherwise noted: T_A = 25˚C, V_{CC} = +5.0V, V_{IN} = 0.70 V_{P-P}, V_{ABL} = V_{CC}, C_L = 8 pF, Video Outputs = 2.0 V_{P-P}. Setting numbers refer to the definitions in *Table 1. Test Settings*. See (Note 7) for Min and Max parameters and (Note 6) for Typicals.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_S	Supply Current	Test Setting 1, both supplies, no output loading. See (Note 8).		200	250	mA
I_{S-PS}	Supply Current, Power Save Mode	Test Setting 1, both supplies, no output loading. See (Note 8).		70	95	mA
$V_{O\ BLK}$	Active Video Black Level Output Voltage	Test Setting 4, no AC input signal, DC offset (register 0x8438 set to 0xd5).		1.2		VDC
$V_{O\ BLK\ STEP}$	Active Video Black Level Step Size	Test Setting 4, no AC input signal.		100		mVDC
V_O Max	Maximum Video Output Voltage	Test Setting 3, Video in = 0.70 V_{P-P}	4.0	4.3		V
LE	Linearity Error	Test Setting 4, staircase input signal (see *Table 9. Page RAM Format (9-bit mode)*).		5		%
t_r	Video Rise Time	(Note 5), 10% to 90%, Test Setting 4, AC input signal.		3.1		ns
OS_R	Rising Edge Overshoot	(Note 5), Test Setting 4, AC input signal.		2		%
t_f	Video Fall Time	(Note 5), 90% to 10%, Test Setting 4, AC input signal.		2.9		ns
OS_F	Falling Edge Overshoot	(Note 5), Test Setting 4, AC input signal.		2		%
BW	Channel Bandwidth (−3 dB)	(Note 5), Test Setting 4, AC input signal.		150		MHz
V_{SEP} 10 kHz	Video Amplifier 10 kHz Isolation	(Note 14), Test Setting 8.		−60		dB
V_{SEP} 10 MHz	Video Amplifier 10 MHz Isolation	(Note 14), Test Setting 8.		−50		dB
A_V Max	Maximum Voltage Gain	Test Setting 8, AC input signal.	3.8	4.1		V/V
A_V C-50%	Contrast Attenuation @ 50%	Test Setting 5, AC input signal.		−5.2		dB
A_V Min/A_V Max	Maximum Contrast Attenuation (dB)	Test Setting 2, AC input signal.		−20		dB
A_V G-50%	Gain Attenuation @ 50%	Test Setting 6, AC input signal.		−4.0		dB
A_V G-Min	Maximum Gain Attenuation	Test Setting 7, AC input signal.		−11		dB
A_V Match	Maximum Gain Match between Channels	Test Setting 3, AC input signal.		±0.5		dB
A_V Track	Gain Change between Channels	Tracking when changing from Test Setting 8 to Test Setting 5. See (Note 11).		±0.5		dB

Video Signal Electrical Characteristics (Continued)

Unless otherwise noted: T_A = 25˚C, V_{CC} = +5.0V, V_{IN} = 0.70 V_{P-P}, V_{ABL} = V_{CC}, C_L = 8 pF, Video Outputs = 2.0 V_{P-P}. Setting numbers refer to the definitions in *Table 1. Test Settings*. See (Note 7) for Min and Max parameters and (Note 6) for Typicals.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$Vid_{Threshold}$	Video Threshold	Normal Operation		80		mV
V_{ABL} TH	ABL Control Range Upper Limit	(Note 12), Test Setting 4, AC input signal.		4.8		V
V_{ABL} Range	ABL Gain Reduction Range	(Note 12), Test Setting 4, AC input signal.		2.8		V
$A_{V\ 3.5}/A_{V\ Max}$	ABL Gain Reduction at 3.5V	(Note 12), Test Setting 4, AC input signal. V_{ABL} = 3.5V		–2		dB
$A_{V\ 2.0}/A_{V\ Max}$	ABL Gain Reduction at 2.0V	(Note 12), Test Setting 4, AC input signal. V_{ABL} = 2.0V		–12		dB
I_{ABL} Active	ABL Input Bias Current during ABL	(Note 12), Test Setting 4, AC input signal. V_{ABL} = V_{ABL} MIN GAIN			10	µA
I_{ABL} Max	ABL Input Current Sink Capability	(Note 12), Test Setting 4, AC input signal.			1.0	mA
V_{ABL} Max	Maximum ABL Input Voltage during Clamping	(Note 12), Test Setting 4, AC input signal. I_{ABL} = I_{ABL} MAX			V_{CC} + 0.1	V
A_V ABL Track	ABL Gain Tracking Error	*Table 9. Page RAM Format (9-bit mode)*, Test Setting 4, 0.7 V_{P-P} input signal, ABL voltage set to 4.5V and 2.5V.			4.5	%
R_{IP}	Minimum Input Resistance (pins 5, 6, 7)	Test Setting 4.		20		MΩ

OSD Electrical Characteristics

Unless otherwise noted: T_A = 25˚C, V_{CC} = +5.0V. See (Note 7) for Min and Max parameters and (Note 6) for Typicals.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$V_{OSDHIGH}$ max	Maximum OSD Level with OSD Contrast 11	Palette Set at 111, OSD Contrast = 11, RGB Gain = 96, DC Offset = 4		3.85		V
$V_{OSDHIGH}$ 10	Maximum OSD Level with OSD Contrast 10	Palette Set at 111, OSD Contrast = 10, RGB Gain = 96, DC Offset = 4		3.27		V
$V_{OSDHIGH}$ 01	Maximum OSD Level with OSD Contrast 01	Palette Set at 111, OSD Contrast = 01, RGB Gain = 96, DC Offset = 4		2.70		V
$V_{OSDHIGH}$ 00	Maximum OSD Level with OSD Contrast 00	Palette Set at 111, OSD Contrast = 00, RGB Gain = 96, DC Offset = 4		1.97		V
ΔV_{OSD} (Black)	Difference between OSD Black Level and Video Black Level (same channel)	Register 08=0x18, Input Video = Black, Same Channel, Test Setting 8		20		mV
$\Delta V_{BL,OSD\text{-}Video}$ (Ch to Ch)	Difference between OSD Black Level and Video Black Level between Channels	Register 08=0x18, Input Video = Black, Same Channel, Test Setting 8		20		mV
ΔV_{OSD} (White)	Output Match between Channels	Palette Set at 111, OSD Contrast = 11, Maximum difference between R, G and B		3		%
$\Delta V_{OSD}/V_{Video}$ (White)	Matching of OSD to Video peak to peak amplitude ratios between channels, normalized to the smallest ratio.	Palette Set at 111, OSD Contrast = 10, Test Setting 4		3		%
$V_{OSD\text{-}out}$ (Track)	Output Variation between Channels	OSD contrast varied from max to min		3		%

DAC Output Electrical Characteristics

Unless otherwise noted: T_A = 25˚C, V_{CC} = +5.0V, V_{IN} = 0.7V, V_{ABL} = V_{CC}, C_L = 8 pF, Video Outputs = 2.0 V_{P-P}. See (Note 7) for Min and Max parameters and (Note 6) for Typicals. DAC parameters apply to all 4 DACs.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$V_{Min\ DAC}$	Min Output Voltage of DAC	Register Value = 0x00		0.5	0.7	V
$V_{Max\ DAC}$ Mode 00	Max Output Voltage of DAC	Register Value = 0xFF, DCF[1:0] = 00b	3.7	4.2		V
$V_{Max\ DAC}$ Mode 01	Max Output Voltage of DAC in DCF Mode 01	Register Value = 0xFF, DCF[1:0] = 01b	1.85	2.35		V
$\Delta V_{Max\ DAC}$ (Temp)	DAC Output Voltage Variation with Temperature	0 < T < 70˚C ambient		±0.5		mV/˚C
$\Delta V_{Max\ DAC}$ (V_{CC})	DAC Output Voltage Variation with V_{CC}	V_{CC} varied from 4.75V to 5.25V, DAC register set to mid-range (0x7F)		50		mV
Linearity	Linearity of DAC over its Range			5		%
Monotonicity	Monotonicity of the DAC Excluding Dead Zones			±0.5		LSB
I_{MAX}	Max Load Current		–1.0		1.0	mA

System Interface Signal Characteristics

Unless otherwise noted: T_A = 25˚C, V_{CC} = +5.0V, V_{IN} = 0.7V, V_{ABL} = V_{CC}, C_L = 8 pF, Video Outputs = 2.0 V_{P-P}. See (Note 7) for Min and Max parameters and (Note 6) for Typicals. DAC parameters apply to all 4 DACs.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{VTH+}	VFLYBACK Positive Switching Guarantee	Vertical Blanking triggered	2.0			V
V_{SPOT}	Spot Killer Voltage	*Table 17. LM1246 Four-Color Attribute Registers*, V_{CC} Adjusted to Activate	3.4	3.9	4.3	V
V_{Ref}	V_{Ref} Output Voltage (pin 2)		1.25	1.45	1.65	V
V_{IL} (SCL, SDA)	Logic Low Input Voltage		–0.5		1.5	V
V_{IH} (SCL, SDA)	Logic High Input Voltage		3.0		V_{CC} + 0.5	V
I_L (SCL, SDA)	Logic Low Input Current	SDA or SCL, Input Voltage = 0.4V		±10		µA
I_H (SCL, SDA)	Logic High Input Voltage	SDA or SCL, Input Voltage = 4.5V		±10		µA
V_{OL} (SCL, SDA)	Logic Low Output Voltage	I_O = 3 mA		0.5		V
f_H Min	Minimum Horizontal Frequency	PLL & OSD Functioning; PPL = 0		25		kHz
f_H Max	Maximum Horizontal Frequency	PLL & OSD Functioning; PPL = 4		110		kHz
$I_{HFB\ IN}$ Max	Horizontal Flyback Input	Current Absolute Maximum during Flyback			5	mA
I_{IN}	Peak Current during Flyback	Design Value		4		mA
$I_{HFB\ OUT}$ Max	Horizontal Flyback Input Current	Absolute Maximum during Scan	–700			µA
I_{OUT}	Peak Current during Scan	Not exact - Duty Cycle Dependent		–550		µA
$I_{IN\ THRESHOLD}$	I_{IN} H-Blank Detection Threshold			0		µA
$t_{H\text{-}BLANK\ ON}$	H-Blank Time Delay - On	+ Zero crossing of I_{HFB} to 50% of output blanking start. I_{24} = +1.5mA		45		ns
$t_{H\text{-}BLANK\ OFF}$	H-Blank Time Delay - Off	– Zero crossing of I_{HFB} to 50% of output blanking end. I_{24} = –100µA		85		ns
V_{BLANK} Max	Maximum Video Blanking Level	Test Setting 4, AC input signal	0		0.25	V
$f_{FREERUN}$	Free Run H Frequency, Including H Blank			42		kHz
$t_{PW\ CLAMP}$	Minimum Clamp Pulse Width	See (Note 15)	200			ns
$V_{CLAMP\ MAX}$	Maximum Low Level Clamp Pulse Voltage	Video Clamp Functioning			2.0	V

System Interface Signal Characteristics (Continued)

Unless otherwise noted: T_A = 25˚C, V_{CC} = +5.0V, V_{IN} = 0.7V, V_{ABL} = V_{CC}, C_L = 8 pF, Video Outputs = 2.0 V_{P-P}. See (Note 7) for Min and Max parameters and (Note 6) for Typicals. DAC parameters apply to all 4 DACs.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$V_{CLAMP\ MIN}$	Minimum High Level Clamp Pulse Voltage	Video Clamp Functioning	3.0			V
I_{CLAMP} Low	Clamp Gate Low Input Current	V_{23} = 2V		–0.4		µA
I_{CLAMP} High	Clamp Gate High Input Current	V_{23} = 3V		0.4		µA
$t_{CLAMP-VIDEO}$	Time from End of Clamp Pulse to Start of Video	Referenced to Blue, Red and Green inputs	50			ns

Note 1: Limits of Absolute Maximum Ratings indicate below which damage to the device must not occur.

Note 2: Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits.

Note 3: All voltages are measured with respect to GND, unless otherwise specified.

Note 4: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 5: Input from signal generator: t_r, t_f < 1 ns.

Note 6: Typical specifications are specified at +25˚C and represent the most likely parametric norm.

Note 7: Datasheet min/max specification limits are guaranteed by design, test, or statistical analysis. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may change when the device is not operated under the listed test conditions.

Note 8: The supply current specified is the quiescent current for V_{CC} and 5V Dig with R_L = ∞. Load resistors are not required and are not used in the test circuit, therefore all the supply current is used by the pre-amp.

Note 9: Linearity Error is the maximum variation in step height of a 16 step staircase input signal waveform with a 0.7 V_{P-P} level at the input. All 16 steps equal, with each at least 100 ns in duration.

Note 10: $dt/dV_{CC} = 200*(t_{5.5V}–t_{4.5V})/ ((t_{5.5V} + t_{4.5V}))$ %/V, where: $t_{5.5V}$ is the rise or fall time at V_{CC} = 5.5V, and $t_{4.5V}$ is the rise or fall time at V_{CC} = 4.5V.

Note 11: ΔA_V track is a measure of the ability of any two amplifiers to track each other and quantifies the matching of the three gain stages. It is the difference in gain change between any two amplifiers with the contrast set to A_VC–50% and measured relative to the A_V max condition. For example, at A_V max the three amplifiers' gains might be 12.1 dB, 11.9 dB, and 11.8 dB and change to 2.2 dB, 1.9 dB and 1.7 dB respectively for contrast set to A_VC–50%. This yields a typical gain change of 10.0 dB with a tracking change of ±0.2 dB.

Note 12: The ABL input provides smooth decrease in gain over the operational range of 0 dB to –5 dB: $\Delta A_{ABL} = A(V_{ABL} = V_{ABL\ MAX\ GAIN}) – A\ (V_{ABL} = V_{ABL\ MIN\ GAIN})$. Beyond –5 dB the gain characteristics, linearity and pulse response may depart from normal values.

Note 13: Machine Model ESD test is covered by specification EIAJ IC-121-1981. A 200 pF cap is charged to the specific voltage, then discharged directly into the IC with no external series resistor (resistance of discharge path must be under 50Ω).

Note 14: Measure output levels of the other two undriven amplifiers relative to the driven amplifier to determine channel separation. Terminate the undriven amplifier inputs to simulate generator loading. Repeat test at f_{IN} = 10 MHz for V_{SEP} 10 MHz.

Note 15: A minimum pulse width of 200 ns is the guaranteed minimum for a horizontal line of 15 kHz. This limit is guaranteed by design. If a lower line rate is used then a longer clamp pulse may be required.

Note 16: Adjust input frequency from 10 MHz (A_V max reference level) to the –3 dB corner frequency ($f_{-3\ dB}$).

Note 17: Once the spot killer has been activated, the LM1246 remains in the off state until V_{CC} is cycled (reduced below 0.5V and then restored to 5V).

Hexadecimal and Binary Notation

Hexadecimal numbers appear frequently throughout this document, representing slave and register addresses, and register values. These appear in the format "0x...". For example, the slave address for writing the registers of the LM1246 is hexadecimal BA, written as 0xBA. On the other hand, binary values, where the individual bit values are shown, are indicated by a trailing "b". For example, 0xBA is equal to 10111010b. A subset of bits within a register is referred to by the bit numbers in brackets following the register value. For example, the OSD contrast bits are the fourth and fifth bits of register 0x8438. Since the first bit is bit 0, the OSD contrast register is 0x8438[4:3].

Register Test Settings

Table 1. Test Settings shows the definitions of the Test Settings 1–8 referred to in the specifications sections. Each test setting is a combination of five hexadecimal register values, Contrast, Gain (Blue, Red, Green) and DC offset.

TABLE 1. Test Settings

Control	No. of Bits	Test Settings							
		1	2	3	4	5	6	7	8
Contrast	7	0x7F (Max)	0x00 Min	0x7F (Max)	0x7F (Max)	0x40 (50.4%)	0x7F (Max)	0x7F (Max)	0x7F (Max)
B, R, G Gain	7	0x7F (Max)	0x7F (Max)	0x7F (Max)	Set V_O to 2 V_{P-P}	0x7F (Max)	0x40 (50.4%)	0x00 (Min)	0x7F (Max)
DC Offset	3	0x00 (Min)	0x05	0x07 (Max)	0x05	0x05	0x05	0x05	0x05

Compatibility with LM1237 and LM1247

Compatibility with LM1237 and LM1247 (Continued)

The Compatibility of the LM1246 to the LM1237 and LM1253A is the same as that of the LM1247. Please refer to the LM1247 datasheet for details.

In order to maintain register compatibility with the LM1253A and LM1237 preamplifier datasheet assignments for bias and brightness, the color assignments are recommended as shown in *Table 2. LM1253A/LM1237 Compatibility*. If datasheet compatibility is not required, then the DAC assignments can be arbitrary.

TABLE 2. LM1253A/LM1237 Compatibility

	DAC Bias Outputs			
LM1246 Pin:	DAC 1	DAC 2	DAC 3	DAC 4
Assignment:	Blue	Green	Red	Brightness

OSD vs Video Intensity

The OSD amplitude has been increased over the LM1237 level. During monitor alignment, the three gain registers are used to achieve the desired front of screen color balance. This also causes the OSD channels to be adjusted accordingly, since these are inserted into the video channels prior to the gain attenuators. This provides the means to fine tune the intensity of the OSD relative to the video as follows. If a typical starting point for the alignment is to have the gains at maximum (0x7F) and the contrast at 0x55, the resultant OSD intensity will be higher than if the starting point is with the gains at 0x55 and the contrast at maximum (0x7F). This tradeoff allows fine tuning the final OSD intensity relative to the video. In addition, the OSD contrast register, 0x8438 [4:3], provides 4 major increments of intensity. Together, these allow setting the OSD intensity to the most pleasing level.

ESD Protection

The LM1246 features a 3.0 kV ESD protection level (see (Notes 4, 13)). This is provided by special internal circuitry which activates when the voltage at any pin goes beyond the supply rails by a preset amount. At that time, the protection is applied to all the pins, including SDA and SCL.

Typical Performance Characteristics V_{CC} = 5V, T_A = 25˚C unless otherwise specified

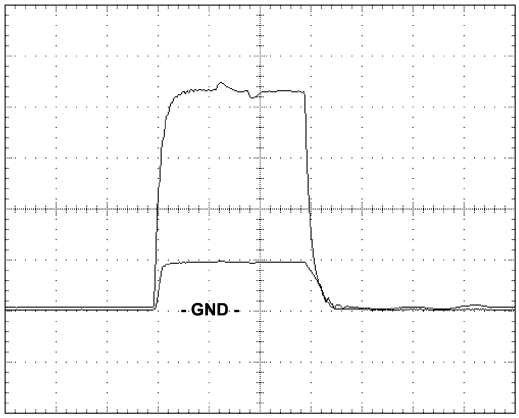


FIGURE 2. Logic Horizontal Blanking

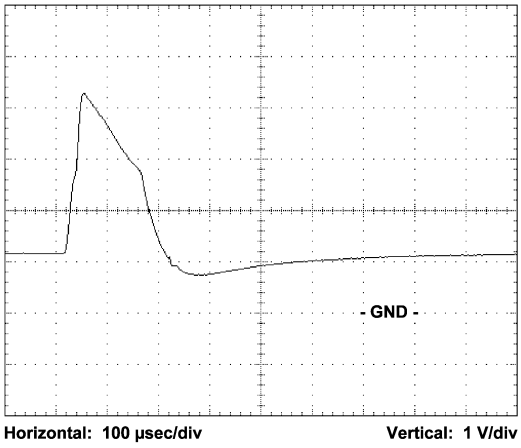


FIGURE 5. Deflection Vertical Blanking

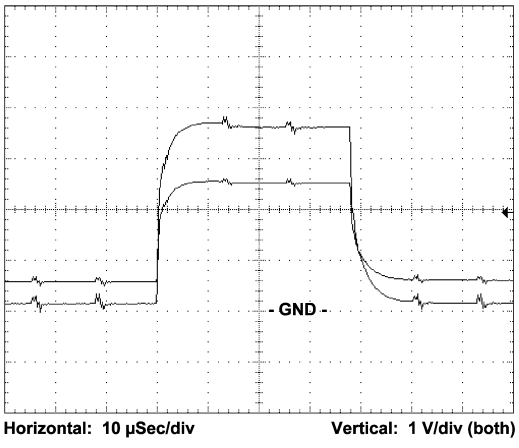


FIGURE 3. Logic Vertical Blanking

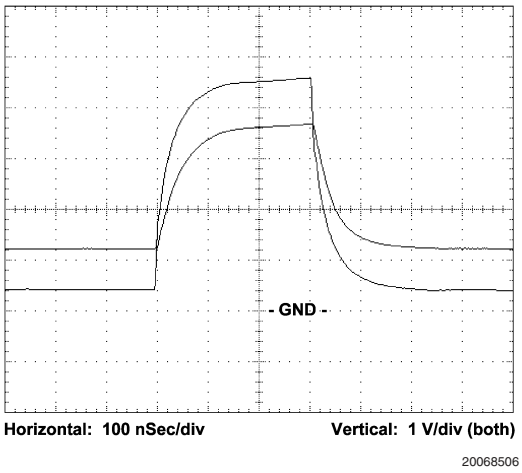


FIGURE 6. Logic Clamp Pulse

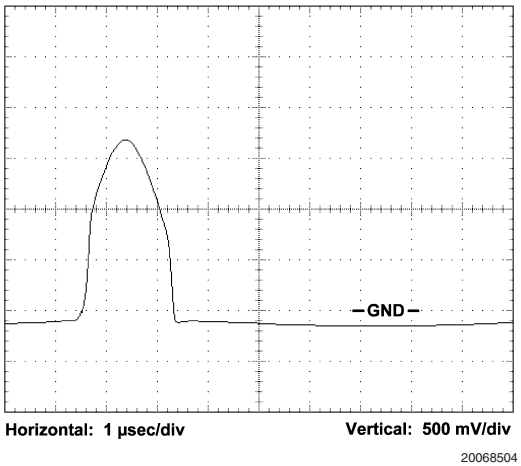


FIGURE 4. Deflection Horizonal Blanking

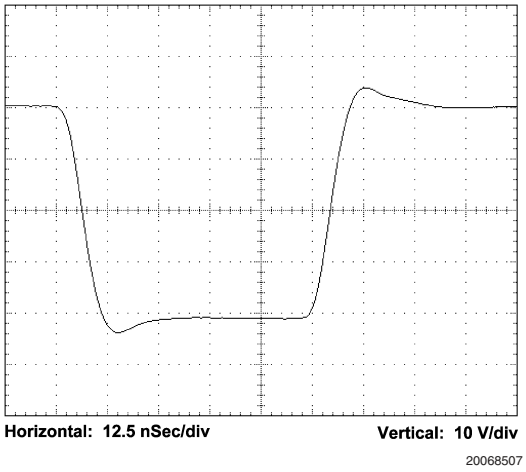


FIGURE 7. Red Cathode Response

Typical Performance Characteristics V_{CC} = 5V, T_A = 25˚C unless otherwise specified (Continued)

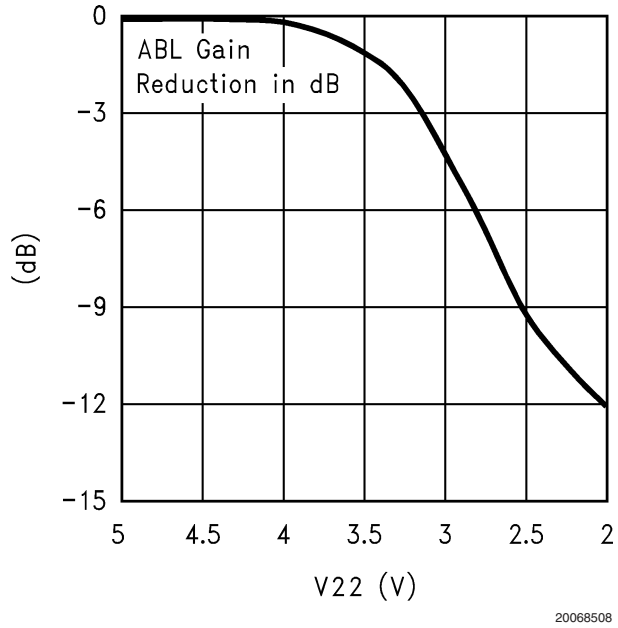


FIGURE 8. ABL Gain Reduction Curve

SYSTEM INTERFACE SIGNALS

The Horizontal and Vertical Blanking and the Clamping input signals are important for proper functionality of the LM1246. Both blanking inputs must be present for OSD synchronization. In addition, the Horizontal blanking input also assists in setting the proper cathode black level, along with the Clamping pulse. The Vertical blanking input initiates a blanking level at the LM1246 outputs which is programmable from 3 to 127 lines (we recommend at least 10). The start position of the internal Horizontal blanking pulse is programmable from 0 to 64 pixels ahead of the start position of the Horizontal flyback input. Both horizontal and vertical blanking can be individually disabled, if desired.

Figure 2 and *Figure 3* show the case where the Horizontal and Vertical inputs are logic levels. *Figure 2* shows the smaller pin 24 voltage superimposed on the horizontal blanking pulse input to the neck board with R_H = 4.7k and C_{17} = 0.1 µF. Note where the voltage at pin 24 is clamped to about 1V when the pin is sinking current. *Figure 3* shows the smaller pin 1 voltage superimposed on the vertical blanking input to the neck board with C_4 jumpered and R_V = 4.7k. These component values correspond to the application circuit of *Figure 9*.

Figures 4, 5 show the case where the horizontal and vertical inputs are from deflection. *Figure 4* shows the pin 24 voltage which is derived from a horizontal flyback pulse of 35V peak to peak with R_H = 8.2K and C_{17} jumpered. *Figure 5* shows the pin 1 voltage which is derived from a vertical flyback pulse of 55V peak to peak with C_4 = 1500 pF and R_V = 120k.

Figure 6 shows the pin 23 clamp input voltage superimposed on the neck board clamp logic input pulse. R_{31} = 1k and should be chosen to limit the pin 23 voltage to about 2.5V peak to peak. This corresponds to the application circuit given in *Figure 9*.

CATHODE RESPONSE

Figure 7 shows the response at the red cathode for the application circuit in *Figures 9, 10*. The input video risetime is 1.5 ns. The resulting leading edge has a 7.1 ns risetime and a 7.6% overshoot, while the trailing edge has a 7.1 ns risetime and a 6.9% overshoot with an LM2467 driver.

ABL GAIN REDUCTION

The ABL function reduces the contrast level of the LM1246 as the voltage on pin 22 is lowered from V_{CC} to around 2V. *Figure 8* shows the amount of gain reduction as the voltage is lowered from V_{CC} (5.0V) to 2V. The gain reduction is small until V_{22} reaches the knee around 3.7V, where the slope increases. Many system designs will require about 3 dB to 5 dB of gain reduction in full beam limiting. Additional attenuation is possible, and can be used in special circumstances. However, in this case, video performance such as video linearity and tracking between channels will tend to depart from normal specifications.

OSD PHASE LOCKED LOOP

The PLL in the LM1246 has a maximum pixels per line setting significantly higher than that of the LM1247. The range for the LM1246 is from 704 to 1152 pixels per line, in increments of 64. The maximum OSD pixel frequency available is 111 MHz. For example, if the horizontal scan rate is 106kHz, 1024 pixels per line would be acceptable to use, since the OSD pixel frequency is:

Horizontal Scan Rate X PPL =
106kHz X 1024 = 108.5 MHz

Typical Performance Characteristics V_{CC} = 5V, T_A = 25˚C unless otherwise specified (Continued)

TABLE 3. OSD Register Recommendations

	PPL=0	PPL=1	PPL=2	PPL=3	PPL=4	PPL=5	PPL=6	PPL=7
PLL Auto	25 - 110	25 - 110	25 - 110	25 - 110	25 - 110	25 - 108	25 - 102	25 - 96

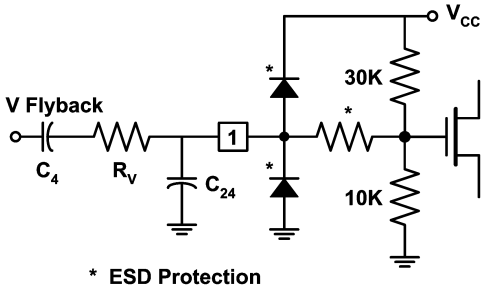
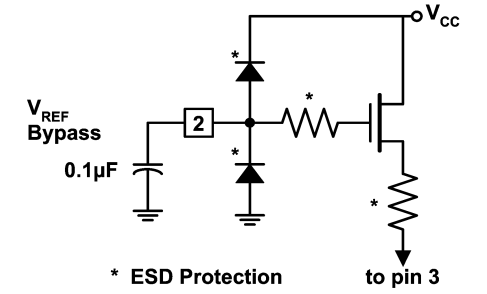
If 1152 pixels per line is being used, the horizontal scan rate would have to be lower than 106 kHz in order to not exceed the maximum OSD pixel frequency of 111 MHz. The maximum number of vertical video lines that may be used is 1536 lines as in a 2048x1536 display. The LM1246 has a **PLL Auto** feature, which will automatically select an internal PLL frequency range setting that will guarantee optimal OSD locking for any horizontal scan rate. This offers improved PLL performance and eliminates the need for PLL register settings determined by the user. To initialize the PLL Auto feature, set bits, 0x843E[1:0] to 0 for pre-calibration, which takes one vertical scan period to complete, and must be done while the video is blanked. Subsequently, set 0x843E[6] to 1, which must also be done while the video is blanked. *Table 3. OSD Register Recommendations* shows the recommended horizontal scan rate ranges (in kHz) for each pixels per line register setting, 0x8401[7:5]. These ranges are recommended for chip ambient temperatures of 0°C to 70°C, and the recommended PLL filter values are 6.2kohms, 0.01uF, and 1000pF as shown in the schematic. While the OSD PLL will lock for other register combinations and at scan rates outside these ranges, the performance of the loop will be improved if these recommendations are followed.

PLL Auto Mode Initialization Sequence

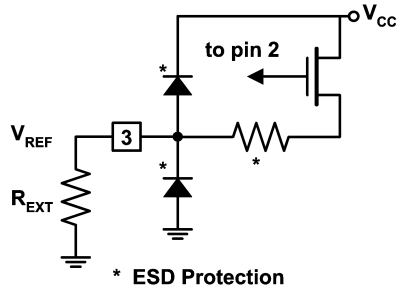
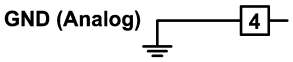
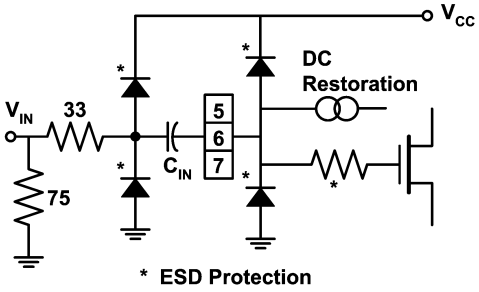
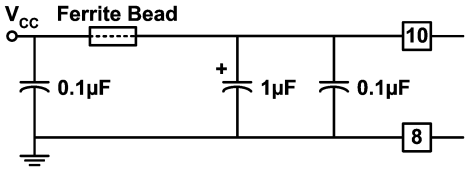
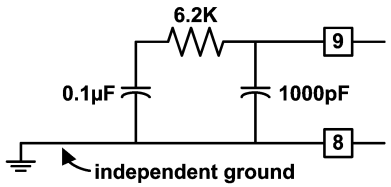
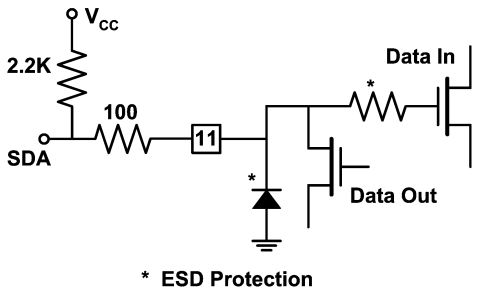
- Blank video
- In PLL manual mode, set PLL range (0x843E[1:0]) to 0
- Wait for at least one vertical period or vertical sync pulse to pass
- Set 0x843E[6] to 1 to activate the Auto mode
- Wait for at least one vertical period or vertical sync pulse to pass
- Unblank video

This Sequence must be done by the microcontroller at system power up, as well as each time there is a horizontal line rate change from the video source, for the PLL Auto mode to function properly.

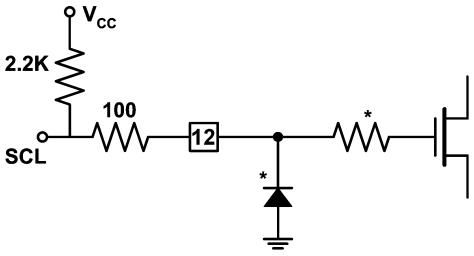
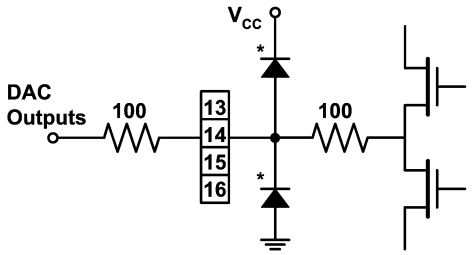
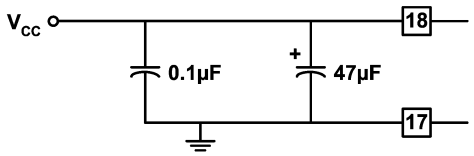
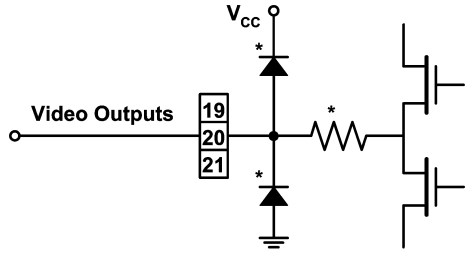
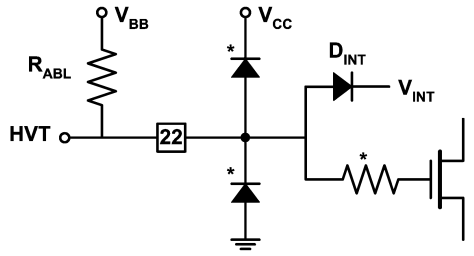
Pin Descriptions and Application Information

Pin No.	Pin Name	Schematic	Description
1	V Flyback		Required for OSD synchronization and is also used for vertical blanking of the video outputs. The actual switching threshold is about 35% of V_{CC}. For logic level inputs C_4 can be a jumper, but for flyback inputs, an AC coupled differentiator is recommended, where R_V is large enough to prevent the voltage at pin 1 from exceeding V_{CC} or going below GND. C_4 should be small enough to flatten the vertical rate ramp at pin 1. C_{24} may be needed to reduce noise.
2	V_{REF} Bypass		Provides filtering for the internal voltage which sets the internal bias current in conjunction with R_{EXT}. A minimum of 0.1 µF is recommended for proper filtering. This capacitor should be placed as close to pin 2 and the pin 4 ground return as possible.

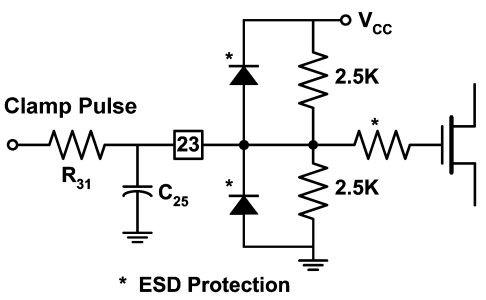
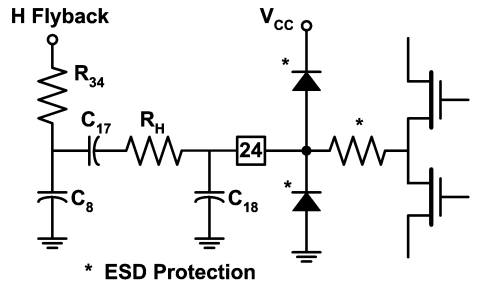
Pin Descriptions and Application Information (Continued)

Pin No.	Pin Name	Schematic	Description
3	V_{REF}		External resistor, 10k 1%, sets the internal bias current level for optimum performance of the LM1247. This resistor should be placed as close to pin 3 and the pin 4 ground return as possible.
4	Analog Input Ground		This is the ground for the input analog portions of the LM1247 internal circuitry.
5 6 7	Blue Video In Red Video In Green Video In		These video inputs must be AC coupled with a .0047 µF cap. Internal DC restoration is done at these inputs. A series resistor of about 33Ω and external ESD protection diodes should also be used for protection from ESD damage.
8 10	Digital Ground PLL V_{CC}		The ground pin should be connected to the rest of the circuit ground by a short but independent PCB trace to prevent contamination by extraneous signals. The V_{CC} pin should be isolated from the rest of the V_{CC} line by a ferrite bead and bypassed to pin 8 with an electrolytic capacitor and a high frequency ceramic.
9	PLL Filter		Recommended topology and values are shown to the left. It is recommended that both filter branches be bypassed to the independent ground as close to pin 8 as possible. Great care should be taken to prevent external signals from coupling into this filter from video, I^2C, etc.
11	SDA		The I^2C compatible data line. A pull-up resistor of about 2 kΩ should be connected between this pin and V_{CC}. A resistor of at least 100Ω should be connected in series with the data line for additional ESD protection.

Pin Descriptions and Application Information (Continued)

Pin No.	Pin Name	Schematic	Description
12	SCL		The I^2C compatible clock line. A pull-up resistor of about 2 kΩ should be connected between this pin and V_{CC}. A resistor of at least 100Ω should be connected in series with the clock line for additional ESD protection.
13 14 15 16	DAC 4 Output DAC 2 Output DAC 3 Output DAC 1 Output		DAC outputs for cathode cut-off adjustments and brightness control. DAC 4 can be set to change the outputs of the other three DACs, acting as a brightness control. The DAC values and the special DAC 4 function are set through the I^2C compatible bus. A resistor of at least 100Ω should be connected in series with these outputs for additional ESD protection.
17 18	Ground V_{CC}		Ground pin for the output analog portion of the LM1247 circuitry, and power supply pin for all the analog of the LM1247. Note the recommended charge storage and high frequency capacitors which should be as close to pins 17 and 18 as possible.
19 20 21	Green Output Red Output Blue Output		These are the three video output pins. They are intended to drive the LM246x family of cathode drivers. Nominally, about 2V peak to peak will produce 40V peak to peak of cathode drive.
22	ABL		The Automatic Beam Limiter input is biased to the desired beam current limit by R_{ABL} and V_{BB} and normally keeps D_{INT} forward biased. When the current resupplying the CRT capacitance (averaged by C_{ABL}) exceeds this limit, then D_{INT} begins to turn off and the voltage at pin 22 begins to drop. The LM1247 then lowers the gain of the three video channels until the beam current reaches an equilibrium value.

Pin Descriptions and Application Information (Continued)

Pin No.	Pin Name	Schematic	Description
23	CLAMP		This pin accepts either TTL or CMOS logic levels. The internal switching threshold is approximately one-half of V_{CC}. An external series resistor, R_{31}, of about 1K is recommended to avoid overdriving the input devices. In any event, R_{EXT} must be large enough to prevent the voltage at pin 23 from going higher than V_{CC} or below GND.
24	H Flyback		Proper operation requires current reversal. R_H should be large enough to limit the peak current at pin 24 to about +4 ma during blanking, and −500 µA during scan. C_{17} is usually needed for logic level inputs and should be large enough to make the time constant, R_HC_{17} significantly larger than the horizontal period. R_{34} and C_8 are typically 300Ω and 330 pF when the flyback waveform has ringing and needs filtering. C_{18} may be needed to filter extraneous noise and can be up to 100 pF.

Schematic Diagram

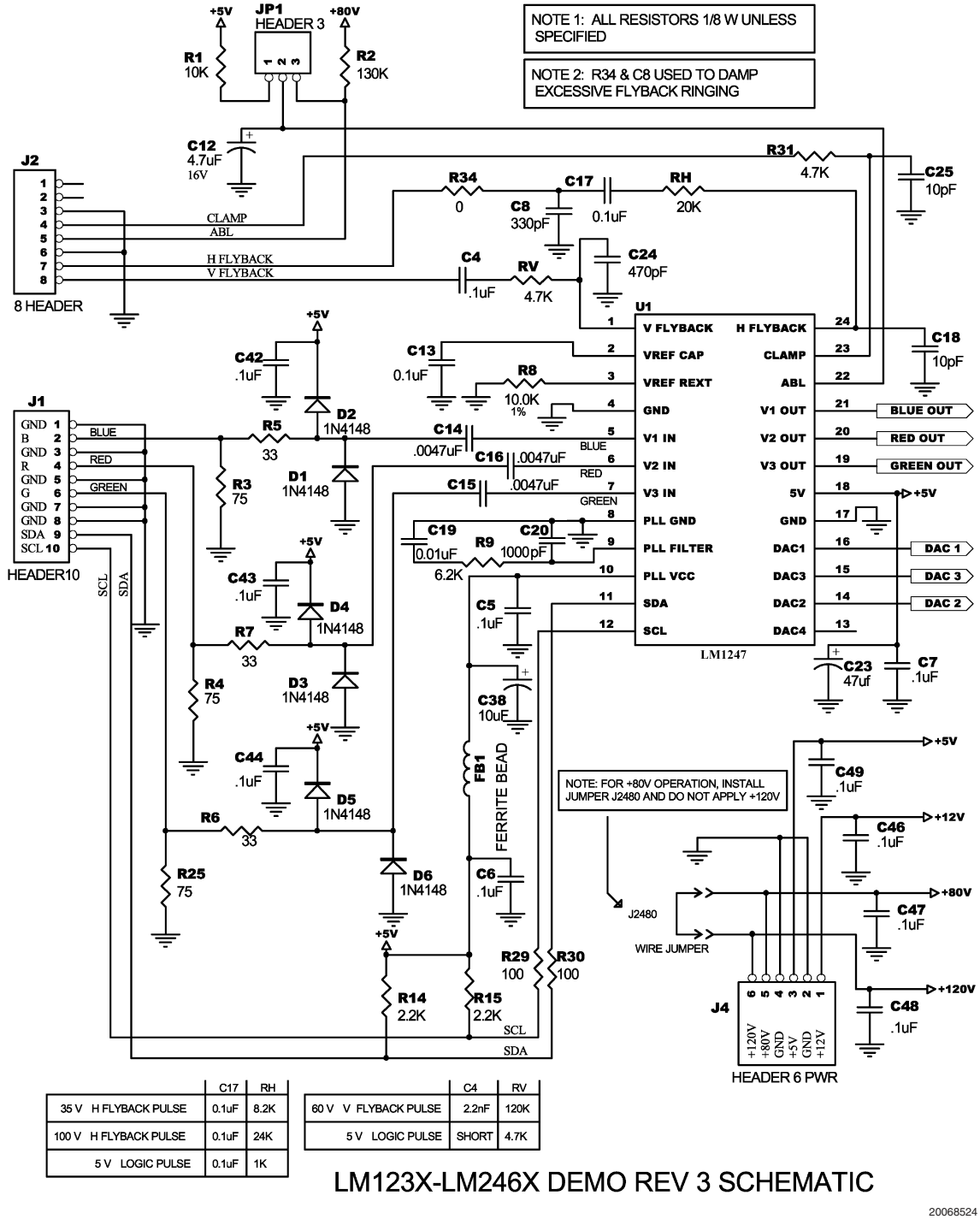
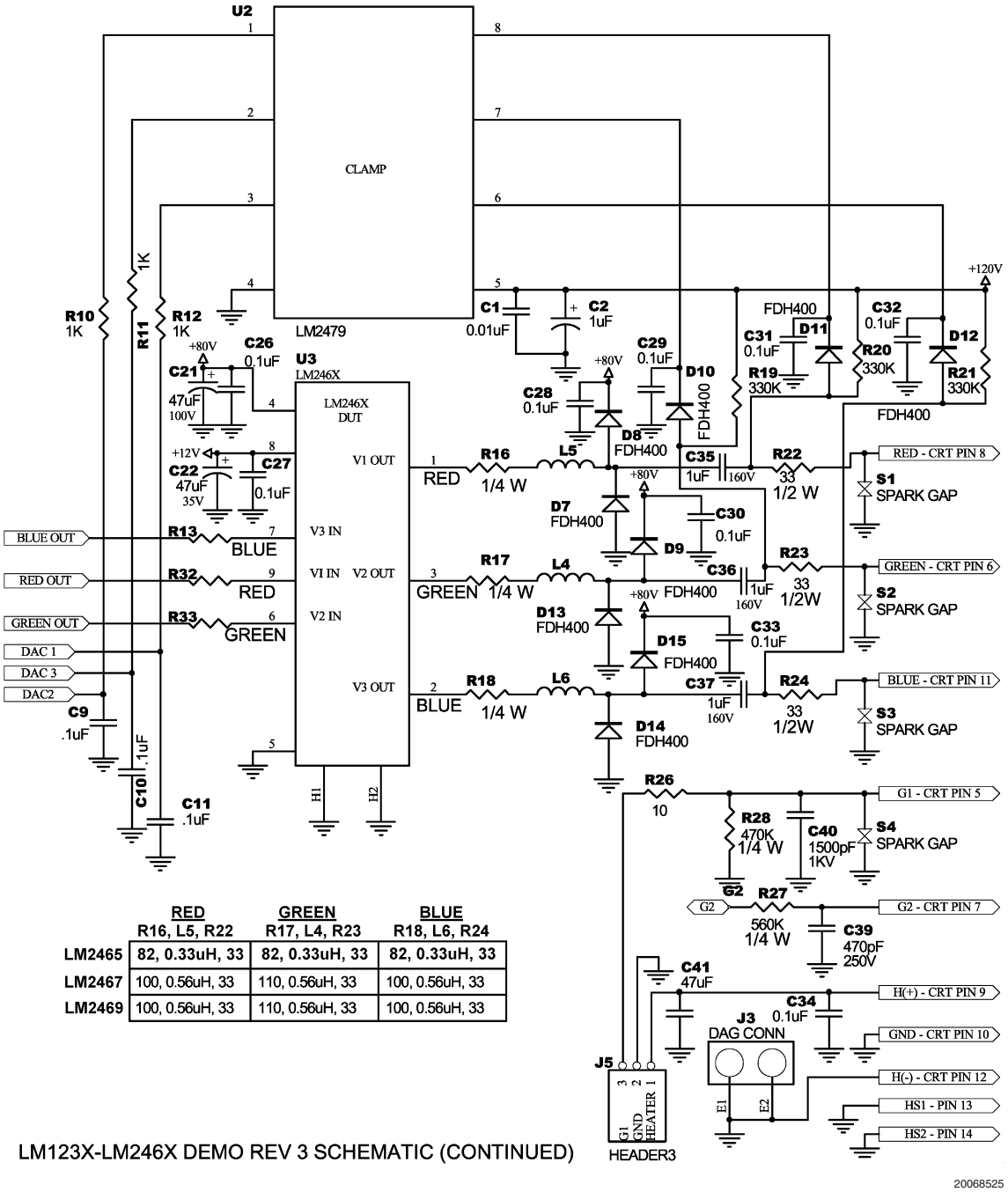


FIGURE 9. LM123x/LM124x-LM246x Demo Board Schematic

Schematic Diagram



	RED R16, L5, R22	GREEN R17, L4, R23	BLUE R18, L6, R24
LM2465	82, 0.33uH, 33	82, 0.33uH, 33	82, 0.33uH, 33
LM2467	100, 0.56uH, 33	110, 0.56uH, 33	100, 0.56uH, 33
LM2469	100, 0.56uH, 33	110, 0.56uH, 33	100, 0.56uH, 33

FIGURE 10. LM123x/LM124x-LM246x Demo Board Schematic (continued)

PCB Layout

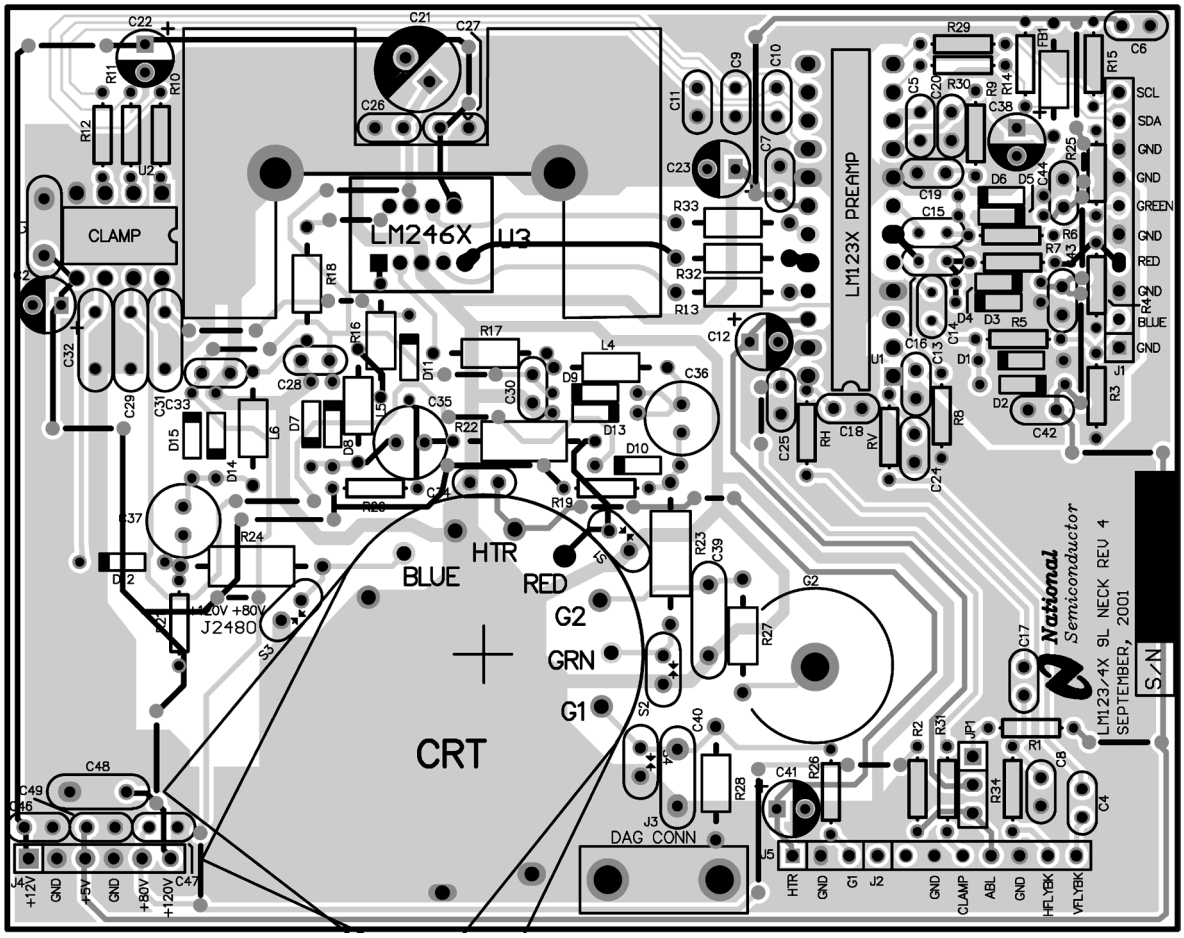


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FIGURE 11. LM123x/LM124x-LM246x Demo Board Layout

Programmable Horizontal Blank

The leading edge position of the internal horizontal blank can be programmed with respect to the horizontal flyback zero crossing leading edge in steps of 4 OSD pixels up to a maximum of 16 steps as shown below in *Figure 12*. This start position of the horizontal blanking pulse is only programmable to occur before the horizontal flyback zero crossing edge, and cannot be programmed in the opposite direction. The trailing edge of the horizontal blanking pulse is independent of the programmable leading edge, and its relativity to the Horizontal flyback trailing edge remains unchanged. To use this feature, Horizontal Blanking (0x843E[3]) and Programmable Horizontal Blanking (0x843A[2]) must be enabled. The number of steps is programmed with the bits in 0x843A[6:3]. When this feature is disabled, please refer to the H-Blank Time Delay - On specification (+ Zero Crossing of I_{HFB} to 50% of output blanking end) listed under the System Interface Signal Characteristic section.

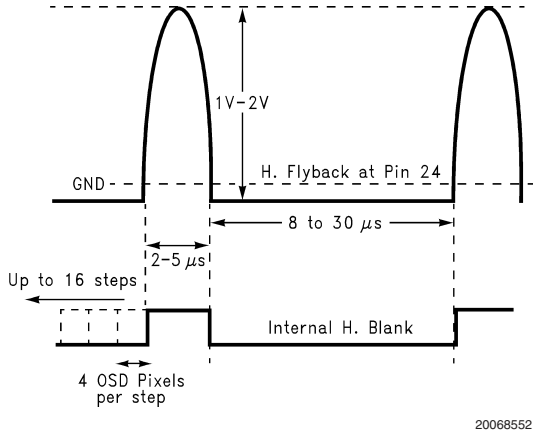


FIGURE 12. Programmable Internal H. Blank

Video Detection for Auto-Sizing & Auto-Centering

The LM1246 is capable of taking measurements necessary for the monitor's microcontroller to perform the auto-sizing and auto-centering operations. The horizontal and vertical flybacks/syncs are used as the reference for timing. Either the flyback or sync signals may be used. In this section, the flyback signals will be considered, although horizontal and vertical sync can be applied similarly. The resultant outputs are the flyback time, the position of the start of video relative to the flyback end, and the time from the end of the active video to the start of the flyback time. Since the total line time is known, the microcontroller can calculate the active video time. The microcontroller can center the video between the start and end of flyback for best image centering, and to calculate the duty cycle of the video with respect to the forward scan time, thus giving a measure of the relative size of the image.

VIDEO INPUT DETECTION

The LM1246 will detect even low-level video information to determine the video image size and position. The video detect logic must also find the extreme points of the displayed image during each frame with respect to the horizontal and vertical flyback pulses as measured using the internal PLL. For best performance in the auto-sizing mode, it is recommended that the application use the maximum OSD pixels per line mode when measurements are made. The durations to be measured are shown generically in *Figure 13* below, and apply to both horizontal and vertical timings. **Since measurements are made in terms of OSD pixels, the ratio of OSD pixels per line to the video pixels per line must be applied to the data below to attain measurements in terms of video pixels.**

1. Flyback or sync period: The duration of either the sync input or the horizontal flyback, in either horizontal lines (vertical) or OSD pixels (horizontal).
2. Back porch period: The duration between the trailing edge of the sync or flyback pulse and the leading edge of the first detected video, in either lines (vertical) or OSD pixels (horizontal).
3. Front porch: The duration between the trailing edge of the last detected video and the leading edge of the sync or flyback pulse, in either lines (vertical) or OSD pixels (horizontal).

The video period is the duration between the leading edge of the first detected video and the trailing edge of the last detected video, in either lines (vertical) or OSD pixels (horizontal). This period is calculated by the microcontroller with the measured periods above.

As the video may start and finish at different positions on the screen, depending upon the image, the measured horizontal porches and video time may vary from line to line. To overcome this, the periods should be measured over at least one entire field. The hardware records the shortest back porch and front porch periods used over the measured period. The possible error for the above measurements are within 1 to 2 OSD pixels.

Video Detection for Auto-Sizing & Auto-Centering (Continued)

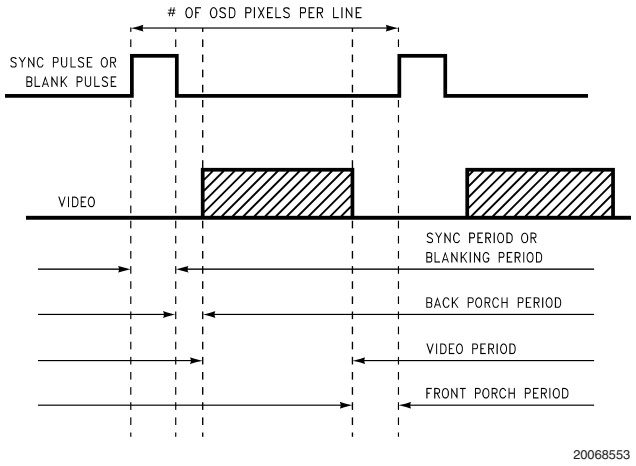


FIGURE 13. Timing Intervals

OSD Generator Operation

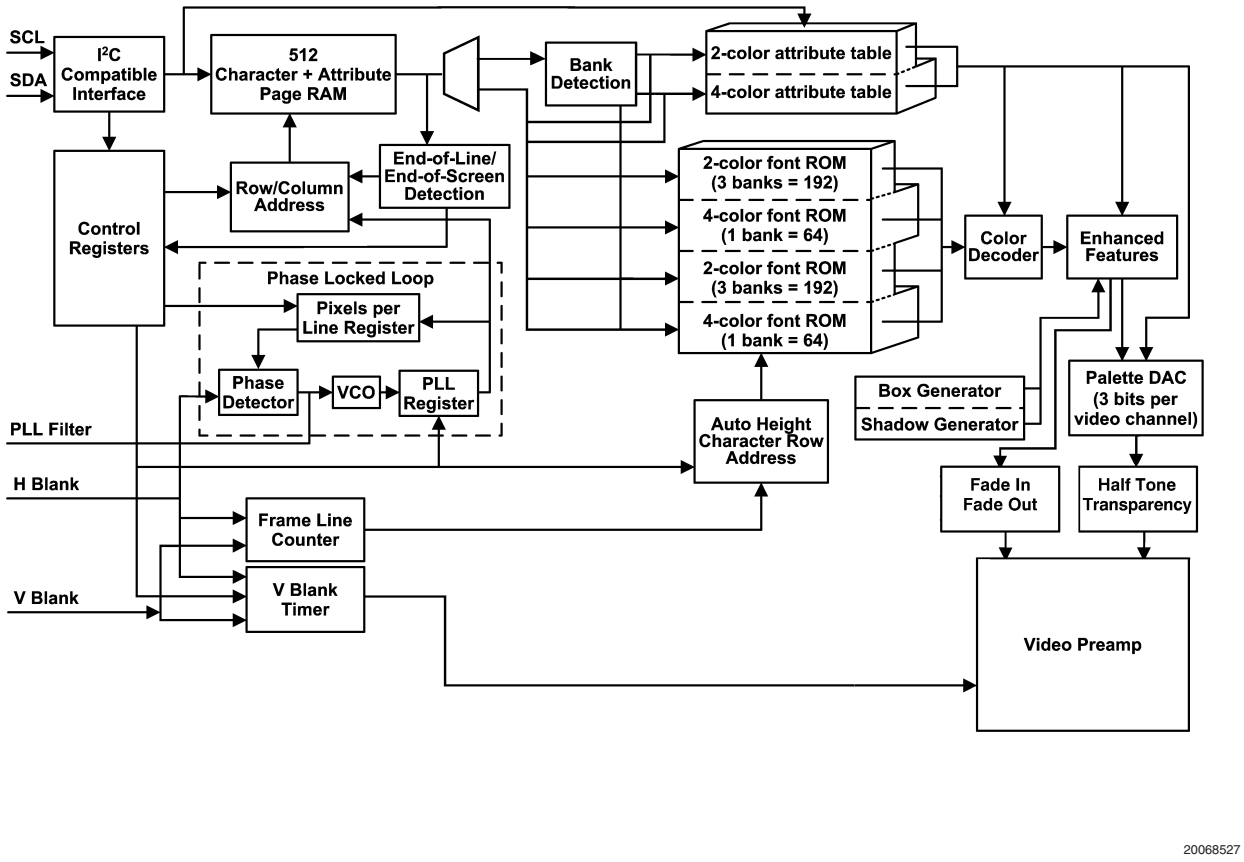


FIGURE 14. OSD Generator Block Diagram

OSD Generator Operation (Continued)

PAGE OPERATION

Figure 14 shows the block diagram of the OSD generator. OSD screens are created using any of the 512 predefined characters stored in the mask programmed ROM. The LM1246 offers two modes of operation. The full 9-bit character code definition mode **allows the entire 512 ROM character set to be displayed at once**. There is also an 8-bit character code definition mode, which ensures compatibility with the LM1247. In this mode, the LM1246 works exactly as a LM1247, where only half of the 512 ROM characters can be displayed at any one time. The two different modes can be selected with bit 2 of register 0x8439, while the default mode is the standard LM1247 mode. Please see the PAGE OPERATION section of the LM1247 datasheet for a detailed explanation on the standard LM1247 mode's 8-bit character code definition and bank select operation. The more flexible 9-bit character code operation enables all 512 character addresses to be independently accessed on one page, however this mode requires more information to be transmitted to specify a full 9-bit character code. The standard LM1247 mode with an 8-bit character code requires minimal I2C transmission as well as minimal ROM in the monitor's microcontroller, however the application is limited to the display of only 254 out of the 512 characters on any single OSD menu page.

OSD ROM CONFIGURATION

The OSD ROM is equivalent to two 256 character ROMs of the type used in the LM1253A and LM1237. When the standard LM1247 is the selected mode of operation, where the bank select method is in effect, each can be considered as a group of 3 banks, (192) two-color characters followed by 1 bank (64) four-color characters. Physically, the combined ROM is then 192x2 + 64x4 + 192x2 + 64x4. This is shown in *Figure 14*.

BANK ADDRESSING

A pictorial view of this addressing method is shown in *Figure 15*. On the left side is a section of the Page RAM with four different addresses in successive locations, which have been chosen to demonstrate accessing 4 of the 8 ROM banks using the Bank Select Registers. The first has 10b for the two most significant bits, so the OSD generator looks in B2AD[2:0], located in Bank Select Register B, for its ROM bank address. SInce B2AD[2:0] contains 101b, the character font is read from Bank 5. The complete font address is composed of this bank address, plus the lower six bits of the original byte in Page RAM, giving a ROM address of 101101110b. The remaining addresses demonstrate that the four selected banks can be displayed in any order.

END-OF-LINE AND END-OF-SCREEN CODES

There are two special character addresses used in the page RAM, 0x00 (End-Of-Screen) and 0x01 (End-Of-Line). The first must be used to terminate a window and the second to terminate a line. The LM1246 is different from the LM1253A and LM1237 in that these are now not actually encoded into ROM, but are instead detected by the logic as the OSD image is read from page RAM. This means that the two lowest locations in the bank which is currently selected by Bank Select Register 0, 0x8427[2:0], cannot be displayed in an OSD image. However, these two characters can be masked in the ROM, and if this bank is selected by Bank Select Registers 1, 2 or 3, then these two characters are usable on screen.

BLANK CHARACTER REQUIREMENT

Five of the 512 Character ROM should be reserved as blank. ROM Addresses 0 and 1 are for the use of the End-Of-Screen and End-Of-Line characters as mentioned above. ROM addresses 32, 64 ,and 511 must be reserved for test engineering purposes. All other ROM addresses are usable, and any that are unused must be filled with at least a duplicate character. Any other addresses except for those listed above should not be left blank.

DISPLAYING AN OSD IMAGE

Consecutive lines of characters make up the displayed window. These characters are stored in the page RAM through the I^2C compatible bus. Each line can contain any number of characters up to the limit of the displayable line length (dependent on the pixels per line register), although some restrictions concerning the enhanced features apply on character lines longer than 32 characters. The number of characters across the width and height of the page can be varied under I^2C compatible control, but the total number of characters that can be stored and displayed on the screen is limited to 512 including any End-of-Line and End-of-Screen characters. The horizontal and vertical start position can also be programmed through the I^2C compatible bus.

OSD Generator Operation (Continued)

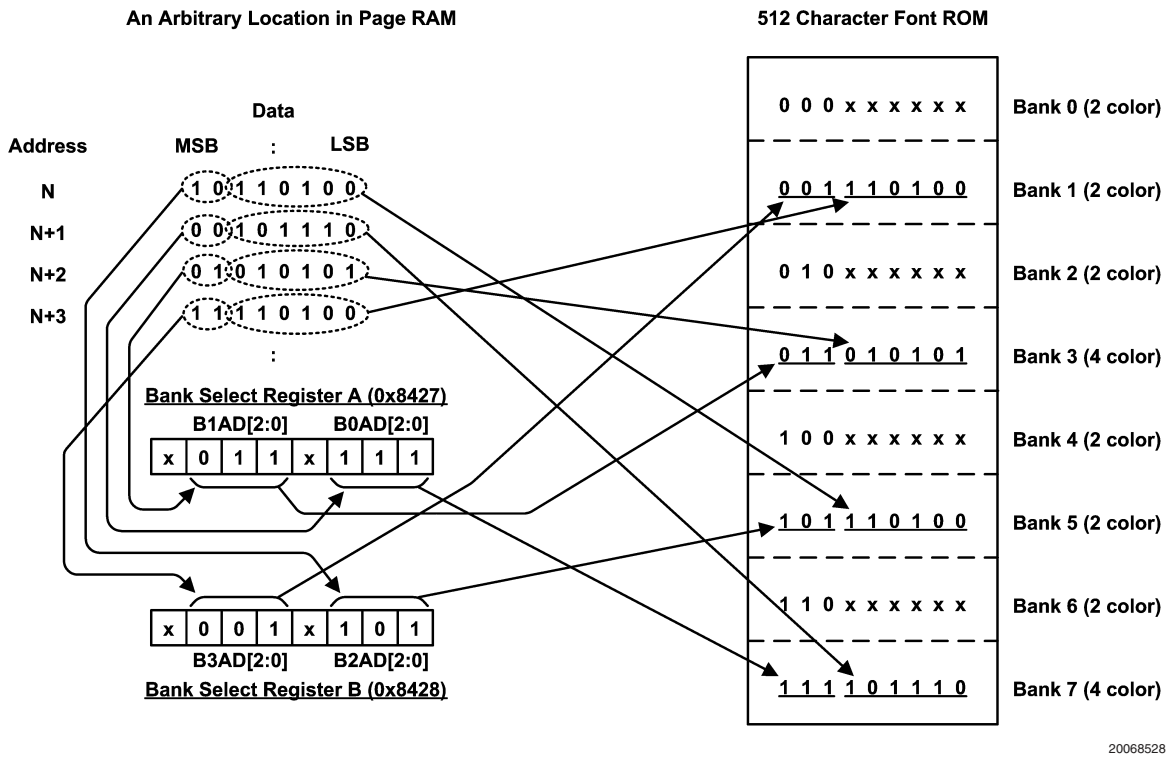


FIGURE 15. Bank Addressing

WINDOWS

Two separate windows can be opened, utilizing the data stored in the page RAM. Each window has its own horizontal and vertical start position, although the second window should be horizontally spaced at least two character spaces away from the first window, and should never overlap the first window when both windows are on. The OSD window must be placed within the active video.

OSD VIDEO DAC

The OSD DAC is controlled by the 9-bit (3x3 bits) OSD video information coming from the pixel serializer look-up table. The look-up table in the OSD palette is programmed to select 4 color levels out of 8 linearly spaced levels per channel. The OSD DAC is shown in *Figure 16*, where the gain is programmable by the 2-bit OSD contrast register, in 4 stages to give the required OSD signal. The OSD DACs use the reference voltage, V_{REF}, to bias the OSD outputs.

OSD VIDEO TIMING

The OSD analog signal then goes to the switch, shown in *Figure 16* and *Figure 1* where the timing control switches from input video to OSD and back again as determined by the control registers. This is also where horizontal and vertical blanking are also inserted at their appropriate intervals.

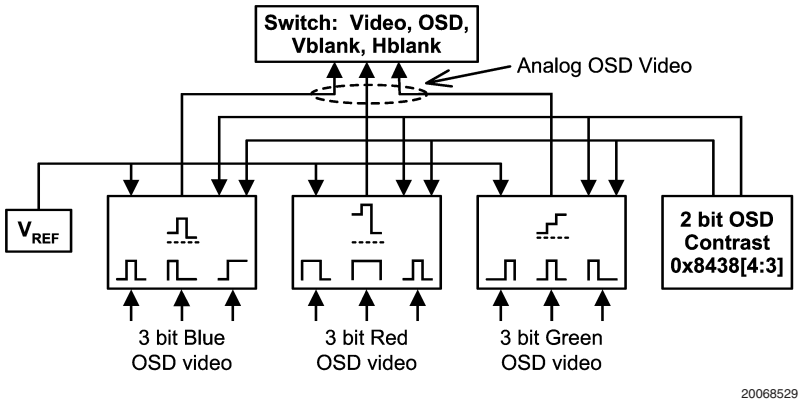


FIGURE 16. Block Diagram of OSD DACs

OSD Generator Operation (Continued)

CHARACTER CELL

Each character is defined as a 12 column by 18 row matrix of picture elements, or "pixels". The character font is shown in *Figure 17 through Figure 24*. There are two types of characters defined in the character ROM:

1. Two-color: There are a total of 384 two-color characters in 6 banks (banks 0, 1, 2, 4, 5 and 6). Each pixel of these characters is defined by a single bit value. If the bit value is 0, then the color is defined as "Color 0" or the "background" color. If the bit value is 1, then the color is defined as "Color 1", or the "foreground" color. An example of a character is shown in *Figure 17*. The grid lines are shown for clarity to delineate individual pixels and are not part of the actual displayed character.
2. Four-color: There are a total of 128 four-color characters, in two banks of 64 (banks 3 and 7). Each pixel of the four-color character is defined by two bits of information, and thus can define four different colors, Color 0, Color 1, Color 2 and Color 3. Color 0 is defined as the "background" color. All other colors are considered "foreground" colors, although for most purposes, any of the four colors may be used in any way. Because each four-color character has two bits, the LM1247 internally has a matrix of two planes of ROM as shown in *Figure 18*. In that figure, dark pixels indicate a logic "1" and light pixels which indicate a logic "0". The left side shows plane 0 which is the least significant bit and the middle figure shows plane 1 which is the most significant bit. The right side composite character formed when each pixel is represented by its two bits formed from the two planes. The color palette used in this example is "00" for white, "01" for black, "10" for blue and "11" for red.
3. By appropriately selecting the color attributes, it is possible to have two 2-color characters in one four color ROM location. If the required number of four color characters is less than 128, the remaining characters can be used to increase the number of two color characters from 384 to 384 + 2*N, where N is the number of unused four color characters. This is explained in the next section.

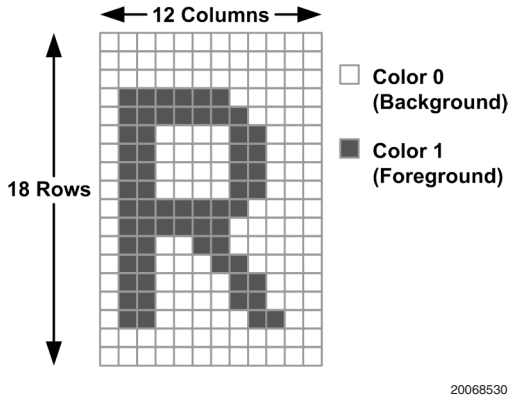


FIGURE 17. Two-Color Character

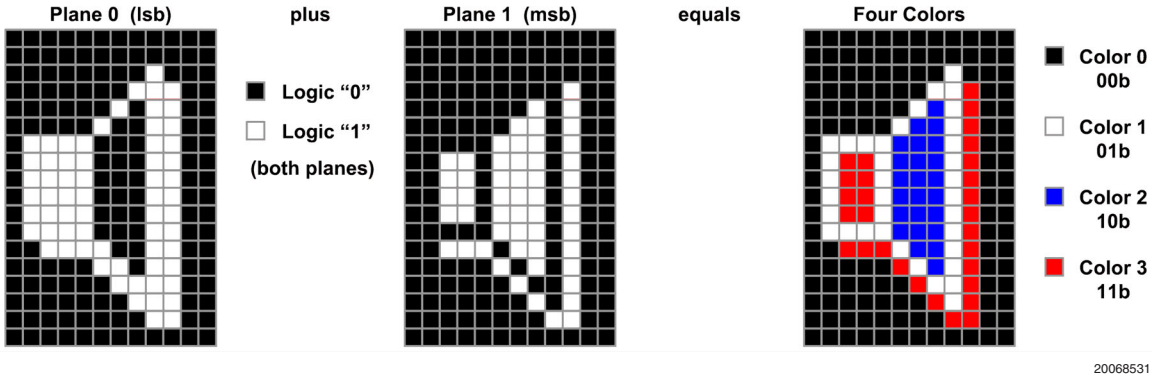


FIGURE 18. Four-Color Character

FOUR COLOR FONT AS TWO 2-COLOR

Using a 4 color character as two 2 color characters is achieved by careful assignment of the four colors. When two 2 color characters are combined, there will be four pixel colors:

Color 0: Those that are background pixels for both characters,

Color 1: Those that are foreground pixels in character one

OSD Generator Operation (Continued)

and background pixels in character two,

Color 2: Those that are foreground pixels in character two and background pixels in character one,

Color 3: Those that are foreground pixels for both characters.

In order to identify which pixels are which, both characters should be drawn in one character cell using the same background color, and different background colors. In *Figure 19*, both "A" and a "B" are drawn separately, then superimposed, with the final 4 color character on the right. Comparing it to the list of colors, it is seen that white is color 0, black is color 1, blue is color 2 and red is color 3. (These particular four colors were chosen for clarity).

Figure 20 shows the composite four color character in the center and the palette choices on the left and the right which result in the display of the two original characters.

To display character 1, which has a foreground color 1, character 2 must be hidden by setting its foreground color (color 2) to equal the background. Color 3 (common pixels) must be set to the desired foreground (color 1). In this case, color 0 and color 2 are black and color 1 and color 3 are white.

To display character 2, set color 1 = color 0 (to hide character 1) and color 3 = color 2. Other than this, there is no restriction on the choice of the actual colors used.

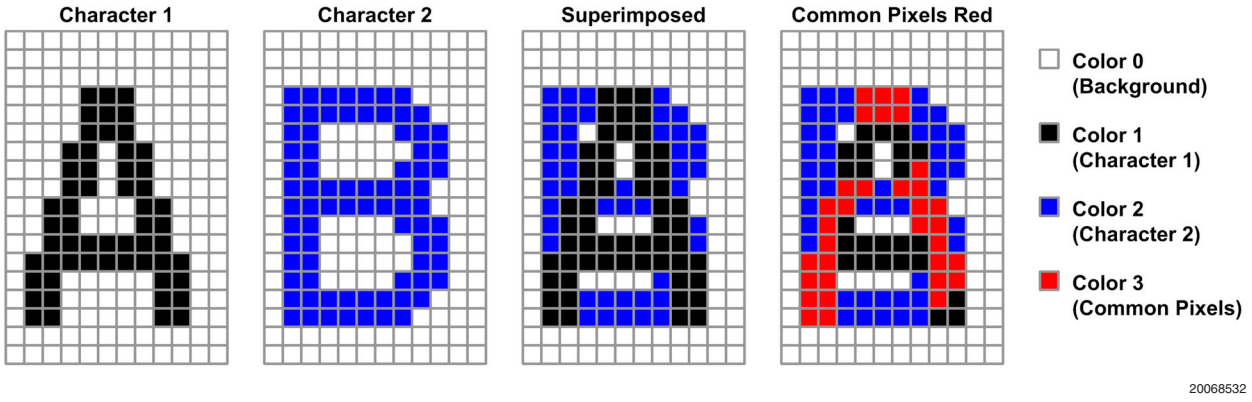


FIGURE 19. Four Color Character as a 2 x 2 Color

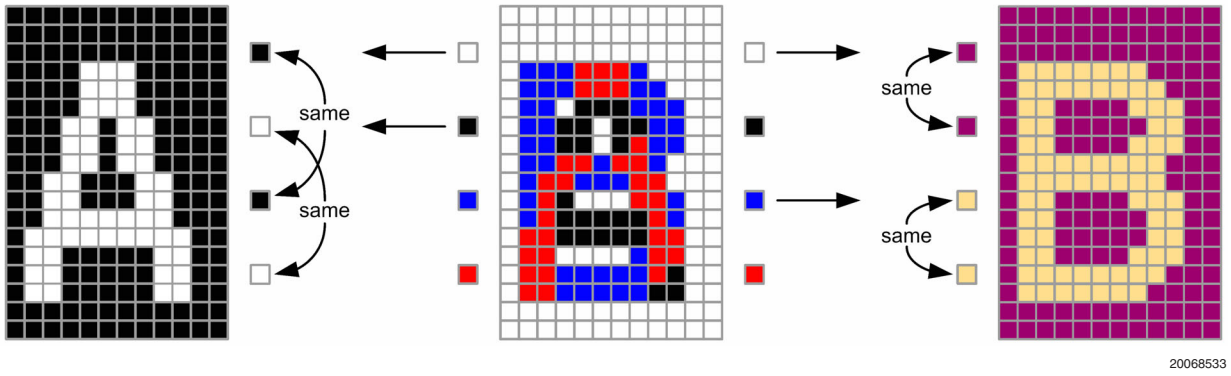


FIGURE 20. Displaying Each Character Individually

ATTRIBUTE TABLES

Each character has an attribute value assigned to it in the page RAM. The attribute value is 4 bits wide, making each character entry in the page RAM 13 bits wide in total. The attribute value acts as an address, which points to one of 16 entries in either the two-color attribute table RAM or the four-color attribute table RAM. The attribute word in the table contains the coding information which defines which color is represented by color 0 and color 1 in the two color attribute table and color 0, color 1, color 2, color 3 in the four-color attribute table. Each color is defined by a 9-bit value, with 3 bits assigned to each channel of RGB. A dynamic look-up table defines each of the 16 different color 'palettes'. As the look-up table can be dynamically coded by the microcontroller over the I^2C compatible interface, each color can be assigned to any one of 2^9 (i.e. 512) choices. This allows a maximum of 64 different colors to be used within one page using the 4-color characters, with up to 4 different colors within any one character and 32 different colors using the 2-color characters, with 2 different colors within any one character.

TRANSPARENT DISABLE

In addition to the 9 lines of video data, a tenth data line is generated by the transparent disable bit. When this line is activated, the black color code will be translated as 'trans-

OSD Generator Operation (Continued)

parent' or invisible. This allows the video information from the PC system to be visible on the screen when this is present. Note that this feature is enabled on any black color in any of the first 8 attribute table entries.

HALF TONE TRANSPARENCY

In addition to the transparent disable bit, there is a half tone disable bit. When the transparency is already in effect and the half tone feature is activated, the contrast of the PC video that is visible in the "transparent area" is reduced to 50%, providing a semi-transparent effect. Just as in the conventional transparency mode, half tone transparency is effective on backgrounds or foregrounds with black color codes from only the first 8 attribute table entries. This feature is controlled by bit 7 of the frame control register, 0x8400, and is only available when the transparency mode is already enabled.

OSD WINDOW FADE IN/ FADE OUT

The OSD window can be opened and closed with a fade in/fade out effect. The interval for fading in and fading out the OSD window in the horizontal and vertical direction is variable and can be set by the microcontroller. This allows the OSD window to be opened or closed in the vertical directions, horizontal direction, or from the upper left to lower right corner. Assuming the desired time to typically complete a full fade in or fade out is 0.5 seconds, and if the vertical scan frequency is for example, 60 Hz, the number of steps is:

$$\frac{\text{fade in/fade out time}}{\text{V. scan time}} = \frac{500\ \text{ms}}{16.67\ \text{ms}} = 30\ \text{steps}$$

With a typical OSD window that is 300 pixels wide and 180 video lines long, the horizontal and vertical intervals would be:

$$\text{Horizontal Interval} = \frac{300\ \text{pixels}}{30\ \text{steps}} = 10$$

$$\text{Vertical Interval} = \frac{180\ \text{lines}}{30\ \text{steps}} = 6$$

For a smooth fade in or fade out animation from the upper left corner to the lower right corner, the horizontal to vertical interval ratio must be matched to the aspect ratio of the OSD window. In the example above, the 300 pixel wide by 180 lines long OSD window has an aspect ratio of 5:3. Thus, the horizontal to vertical interval ratio should be set to 5/3 or 10/6. With an OSD window aspect ratio of 3:2, the H/V intervals can be set to 3/2, 6/4, 9/6, 12/8, or 15/10 for optimal operation. If the calculated aspect ratio of an OSD window is a non-integer ratio, the H/V interval ratio should meet or exceed the aspect ratio. For example, if the OSD aspect ratio is 3.7:2 (or 1.85:1), the H/V intervals should be set to 2/1, 4/2, 6/3, 8/4, 10/5, or 12/6. The fade in/out speed increases as H/V interval settings are increased. The OSD window can also be faded in or out in only one direction if desired, by setting the horizontal interval to 0 for fading in/out strictly in the vertical direction or setting the vertical interval to 0 for fading in/out in the horizontal direction. In interlaced video formats, it is not recommended to fade in and fade out the OSD in the vertical direction, and should be only faded in the horizontal direction. The fade in/out function can be enabled/disabled with bit 5 of the frame control register, 0x8400, and the horizontal & vertical intervals are controlled by setting register 0x8429. The OSD window fade in/out feature can only be used with OSD window 1.

ENHANCED FEATURES

In addition to the wide selection of colors for each character, additional character features can be selected on a character by character basis. There are 3 Enhanced Feature Registers, EF0, EF1 and EF2.

1. Button Boxes — The OSD generator examines the character string being displayed and if the "button box" attributes have been set in the Enhanced feature byte, then a box creator selectively substitutes the character pixels in either or both the top and left most pixel line or column with a button box pixel. The shade of the button box pixel depends upon whether a "depressed" or "raised" box is required, and can be programmed through the I^2C compatible interface. The raised pixel color ("highlight") is defined by the value in the color palette register, EF1 (0x8405–0x8406), which is normally set to white. The depressed pixel ("lowlight") color by the value in the color palette register, EF2 (0x8407–0x8408), which is normally set to gray. See *Figure 21* for detail and *Figure 22* for the on-screen effect.
2. Heavy Button Boxes — When heavy button boxes are selected, the color palette value stored in register EF3 (0x8409 - 0x840A) is used for the depressed ("lowlight") pixel color instead of the value in register EF2.
3. Shadowing — Shadowing can be added to two-color characters by choosing the appropriate attribute value for the character. When a character is shadowed, a shadow pixel is added to the lower right edges of the color 1 image, as shown in *Figure 23*. The color of the shadow is determined by the value in the color palette register EF3, which is normally set to black.
4. Bordering — A border can be added to the two-color characters. When a character is bordered, a border pixel is added at every horizontal, vertical or diagonal transition between color 0 and color 1. See *Figure 24*. The color of the border is determined by the value in the color palette register EF3 (normally black).
5. Blinking — If blinking is enabled as an attribute, all colors within the character except the button box pixels which have been overwritten will alternately switch to color 0 and then back to the correct color at a rate determined by the microcontroller through the I^2C compatible interface.

OSD Generator Operation (Continued)

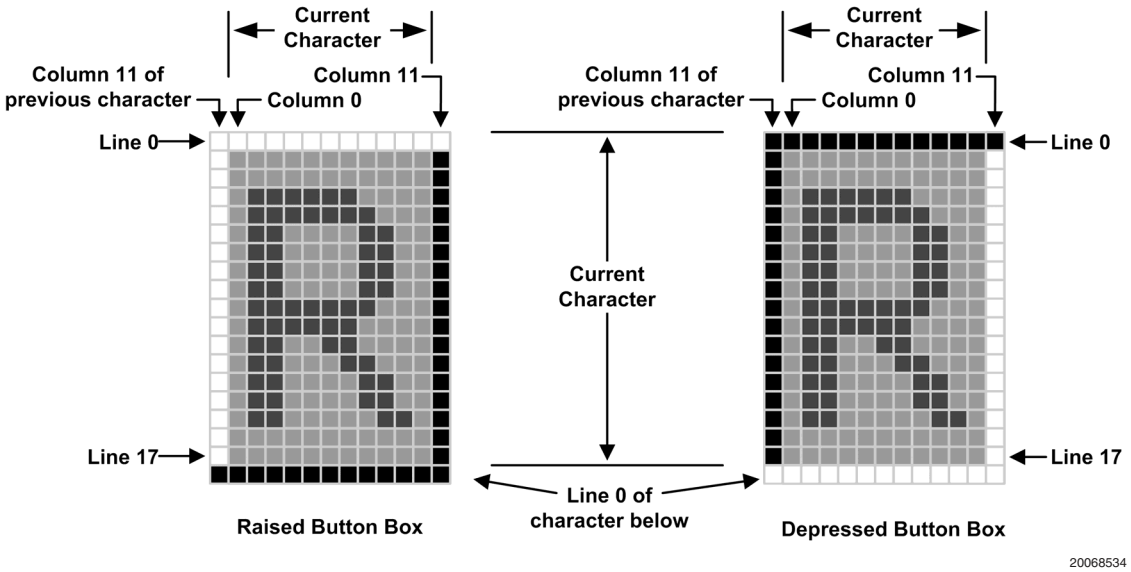


FIGURE 21. Button Box Detail

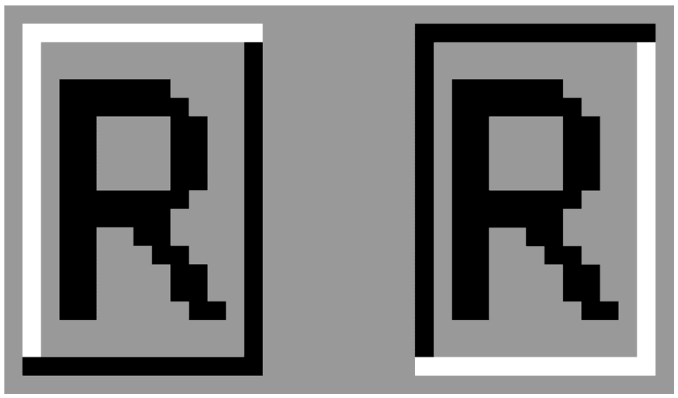


FIGURE 22. On-Screen Effect of Button Boxes

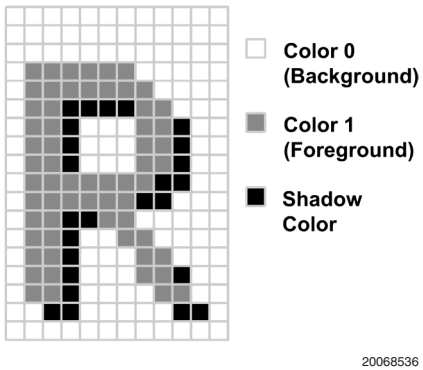


FIGURE 23. Shadowing

OSD Generator Operation (Continued)

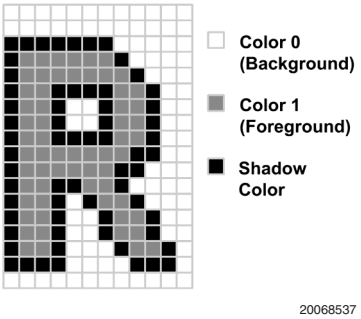


FIGURE 24. Bordering

Microcontroller Interface

The microcontroller interfaces to the LM1246 preamp using the I^2C compatible interface. The protocol of the interface begins with a Start Pulse followed by a byte comprised of a 7-bit Slave Device Address and a Read/Write bit. Since the first byte is composed of both the address and the read/write bit, the address of the LM1246 for writing is 0xBA (10111010b) and the address for reading is 0xBB (10111011b). The development software provided by National Semiconductor will automatically take care of the difference between the read and write addresses if the target address under the communications tab is set to 0xBA. *Figures 25, 26* show a write and read sequence on the I^2C compatible interface.

WRITE SEQUENCE

The write sequence begins with a start condition, which consists of the master pulling SDA low while SCL is held high. The Slave Device Write Address, 0xBA, is sent next. Each byte that is sent is followed by an acknowledge bit. When SCL is high, the master will release the SDA line. The slave must pull SDA low to acknowledge. The register to be written to is next sent in two bytes, the least significant byte being sent first. The master can then send the data, which consists of one or more bytes. Each data byte is followed by an acknowledge bit. If more than one data byte is sent, the data will increment to the next address location. See *Figure 25*.

READ SEQUENCE

Read sequences are comprised of two I2C compatible transfer sequences: The first is a write sequence that only transfers the two byte address to be accessed. The second is a read sequence that starts at the address transferred in the previous address only write access and increments to the next address upon every data byte read. This is shown in *Figure 26*. The write sequence consists of the Start Pulse, the Slave Device Write Address (0xBA), and the Acknowledge bit; the next byte is the least significant byte of the address to be accessed, followed by its Acknowledge bit. This is then followed by a byte containing the most significant address byte, followed by its Acknowledge bit. Then a Stop bit indicates the end of the address only write access. Next the read data access will be performed beginning with the Start Pulse, the Slave Device Read Address (0xBB), and the Acknowledge bit. The next 8 bits will be the read data driven out by the LM1246 preamp associated with the address indicated by the two address bytes. Subsequent read data bytes will correspond to the next increment address locations. Data should only be read from the LM1246 when both OSD windows and the Fade In/ Fade Out are disabled.

Microcontroller Interface (Continued)

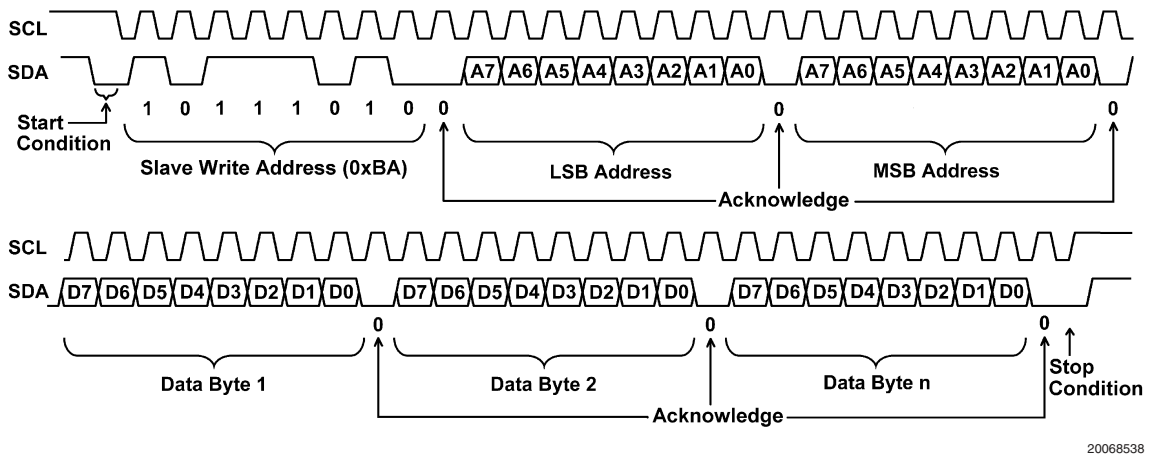


FIGURE 25. I²C Compatible Write Sequence

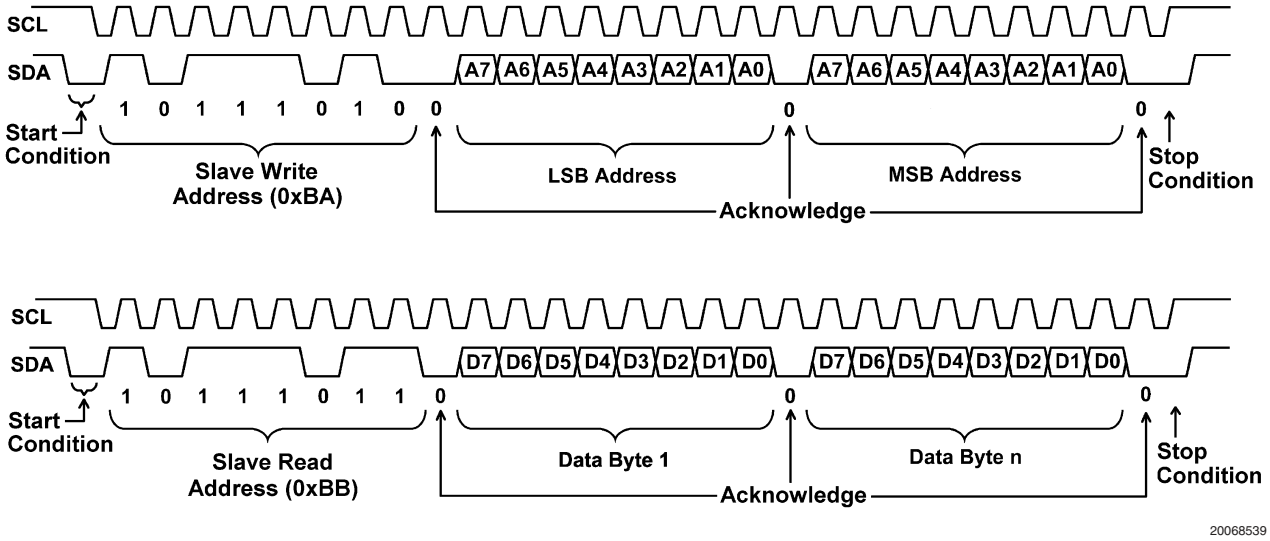


FIGURE 26. I²C Compatible Read Sequence

LM1246 Address Map

CHARACTER ROM

The 512 font characters from 0x0000 to 0x7FFF can be read from ROM by addressing the individual pixel rows of the desired character. Since the characters have 12 columns, it takes two bytes to read a given row of pixels within one character. Since the characters have 18 rows, a total of 36 bytes are needed to read the entire character. The 16-bit address for reading a row of pixels is formed as follows:

$$\text{Address} = (N * 0x1000) + (I * 0x40) + (R * 0x02) + H$$

where: N = bank number ($0x0 \le N \le 0x7$)

I = Character Index within its respective bank ($0x00 \le I \le 0x3F$)

R = row of pixels within the character ($0x00 \le R \le 0x11$)

H = 0 for low byte, 1 for high byte

Note that bit 0 of the Character Font Access Register, 0x8402, needs to be set to 0 to read the 2-color fonts. In order to read the four-color fonts, two complete reads are needed. Set bit 0 of the Character Font Access Register, 0x8402, to a 0 to read the least significant plane and to a 1 to read the most significant plane. See *Table 4. Character ROM Addressing*.

LM1246 Address Map (Continued)

TABLE 4. Character ROM Addressing

Address Range	R/W	Description	0x8402[0]	N
0x0000–0x2FFF	R	These are the first 3 banks of two-color, read-only ROM character fonts. There are 192 total characters in this range.	0	0x0 0x1 0x2
0x3000–0x3FFF	R	This is bank 3 of four-color, read-only ROM character fonts. There are 64 total characters in this range.	0/1	0x3
0x4000–0x6FFF	R	These are banks 4, 5 and 6 of two-color, read-only ROM character fonts. There are 192 characters in this range.	0	0x4 0x5 0x6
0x7000–0x7FFF	R	This is bank 7 of four-color, read-only ROM character fonts. There are 64 total characters in this range.	0/1	0x7

When read back, the low byte will contain the first eight pixels of the row with data bit 0 corresponding to the left most bit in the pixel row. The high byte will contain the remaining four pixels in the least significant nibble. The remaining 4 bits, shown as "X", are "don't care" bits, and should be discarded. Bit 3 of the high byte corresponds to the right most pixel in the pixel row. This is shown in *Table 5. Character ROM Read Data*.

TABLE 5. Character ROM Read Data

Register	Address	D7	D6	D5	D4	D3	D2	D1	D0
Fonts - 2 Color	0x0000–0x2FFE	PIXEL[7:0]							
	+1	X	X	X	X	PIXEL[11:8]			
Fonts - 4 Color	0x3000–0x3FFE	PIXEL[7:0]							
	+1	X	X	X	X	PIXEL[11:8]			
Fonts - 2 Color	0x4000–0x6FFE	PIXEL[7:0]							
	+1	X	X	X	X	PIXEL[11:8]			
Fonts - 4 Color	0x7000–0x7FFE	PIXEL[7:0]							
	+1	X	X	X	X	PIXEL[11:8]			
Display Page	0x8000–0x83FF	X	CHAR_CODE[7:4] or reserved			CHAR_CODE[3:0] or ATTR_CODE			

DISPLAY PAGE RAM

Standard 1247 Mode

This address range (0x8000–0x81FF) contains the 512 characters, which comprise the displayable OSD screens. There must be at least one End-Of-Screen code (0x00) in this range to prevent unpredictable behavior. **NOTE:** To avoid any unpredictable behavior, this range should be cleared by writing a 0 to bit 3 of the FRMCTRL1 Register, 0x8400, immediately after power up. There may also be one or more pairs of End-Of-Line and Skip Line codes. The codes and characters are written as 8-bit bytes, but are stored with their attributes in groups of 13 bits. When writing, one byte describes a displayed character (CC), Attribute Code (AC), End-Of-Screen (EOS), End-Of-Line (EOL) or Skip Line (SL) code.

Full 512 Displayable Character Mode

This mode differs from the above in that the character code is 9 bits long; the attribute code is still 4 bits long, and so the 13-bit wide Page RAM of the LM1246 is fully utilized. The codes and characters are still written as 8-bit bytes, but are stored with their attributes in groups of 13 bits.

When reading characters from RAM, bit 1 of the Character Font Access Register (0x8402) determines whether the lower 8 bits or upper 5 bits of the Page RAM are returned. *Table 6. Page RAM Lower Byte Read Data* gives the lower byte read, which is the first 8 character code bits when bit 1 of the Character Font Access Register is a 0. *Table 7. Page RAM Upper Byte Read Data* gives the upper byte read, which is the 9th character code bit and 4 attribute code bits when this bit is set to a 1.

TABLE 6. Page RAM Lower Byte Read Data

Address Range	D7	D6	D5	D4	D3	D2	D1	D0
0x8000–0x81FF	CHAR_CODE[7:0]							

TABLE 7. Page RAM Upper Byte Read Data

Address	D7	D6	D5	D4	D3	D2	D1	D0
0x8000–0x81FF	X	X	X	CC[8]	ATTR_CODE[3:0]			

LM1246 Address Map (Continued)

RAM Data Format (Standard LM1247 Mode)

Each of the 512 locations in the page RAM is comprised of a 13-bit code consisting of an 8-bit character or control code, and a 4-bit attribute code. Each of the characters is stored in sequence in the page RAM in bits 7:0. Special codes are used between lines to show where one line ends and the next begins, and also to allow blank (or 'skipped') single scan lines to be added between character lines. *Table 8. Page RAM Format (Standard Mode)* shows the format of a character stored in RAM. Note that even though this is a 13- bit format, reading and writing characters and codes is done in 8-bit bytes.

TABLE 8. Page RAM Format (Standard Mode)

ATTRIBUTE CODE	CHARACTER CODE		
	CC[8]	BANK SEL.	BANK CHARACTER
ATT[3:0]	0	CC[7:6]	CC[5:0]

Bits 7–6 determine which Bank Select Register is used to look up the 3-bit address of the bank where the character will be called from. Bits 5–0 determine which of the 64 characters is called from that bank. Bit 8 is unused since this would be the 9th character code bit for the mode below, however in this mode, the character code is defined with only 8 bits. Bits 12–9 address one of the 16 attributes in the table containing the colors and enhanced features to be used for this particular character. Two separate attribute tables are used, one for 2-color characters, and the other for 4-color characters. Note there are 16 available attributes for 2-color characters and a different set of 16 available attributes for 4-color characters. It is the bank number in the register called by the Bank Select bits, which determines whether the character has a 2-color or 4-color attribute.

RAM Data Format (9-Bit Character Code Definition Mode)

Each of the 512 locations in the page RAM is comprised of a 13-bit code consisting of a 9-bit character or control code, and a 4-bit attribute code. Each of the characters is stored in sequence in the page RAM in bits 8:0. Special codes are used between lines to show where one line ends and the next begins, and also to allow blank (or 'skipped') single scan lines to be added between character lines. *Table 9. Page RAM Format (9-bit mode)* shows the format of a character stored in RAM. Note that even though this is a 13- bit format, reading and writing characters and codes is done in 8-bit bytes.

TABLE 9. Page RAM Format (9-bit mode)

ATTRIBUTE CODE	CHARACTER CODE
ATT[3:0]	CC[8:0]

Bits 8–0 determined which of the 512 characters is to be called from the character ROM. Bits 12–9 address one of the 16 attributes in the table containing the colors and enhanced features to be used for this particular character. Two separate attribute tables are used, one for 2-color characters, and the other for 4-color characters. Note there are 16 available attributes for 2-color characters and a different set of 16 available attributes for 4-color characters.

End-Of-Line Code

To signify the end of a line of characters, a special End-of-Line (EOL) code is used in place of a character code. This code, shown in *Table 10. End-Of-Line Code* tells the OSD generator that the character and attribute codes which follow must be placed on a new line in the displayed window. Bits 8–1 are zeros, bit 0 is a one. The attribute that is stored in Page RAM along with this code is not used.

TABLE 10. End-Of-Line Code

ATTRIBUTE CODE	END-OF-LINE CODE								
ATT[3:0]	0	0	0	0	0	0	0	0	1

Skip-Line Code

In order to allow finer control of the vertical spacing of character lines, each displayed line of characters may have up to 15 skipped (i.e., blank) lines between it and the line beneath it. Each skipped line is treated as a single character pixel line, so multiple scan lines may actually be displayed in order to maintain accurate size relative to the character cell. An internal algorithm maintains vertical height proportionality (see the section on Constant Character Height Mechanism). To specify the number of skipped lines, the first character in each new line of characters is interpreted differently than the others in the line. Its data are interpreted as shown in *Table 11. Skipped-Line Code*, with the attribute bits setting the color of the skipped lines.

TABLE 11. Skipped-Line Code

ATTRIBUTE CODE	NUMBER OF SKIPPED LINES					
ATT[3:0]	X	X	X	X	X	SL[3:0]

Bits 8–4 are reserved and should be set to zero. Bits 3–0 determine how many blank pixel lines will be inserted between the present line of display characters and the next. A range of 0–15 may be selected. Bits 12–9 determine which attribute the pixels in the skipped lines will have, which is always called from the two-color attribute table. The pixels will have the background color (Color 0) of the selected attribute table entry.

LM1246 Address Map (Continued)

Note that the pixels in the first line immediately below the character may be overwritten by the pixel override system that creates the button box. (Refer to the Button Box Formation Section for more information).

After the first line, each new line always starts with an SL code, even if the number of skipped lines to follow is zero. This means an SL code must always follow an EOL code. An EOL code may follow an SL code if several 'transparent' lines are required between sections of the window. See example 3 below for a case where skipped lines of zero characters are displayed, resulting in one window being displayed in two segments.

End-Of-Screen Code

To signify the end of the window, a special End-Of-Screen (EOS) code is used in place of a End-Of-Line (EOL) code. There must be at least one EOS code in the Page RAM to avoid unpredictable behavior. This can be accomplished by clearing the RAM by writing a 0 to bit 3 of the FRMCTRL1 Register, 0x8400, immediately after power up.

TABLE 12. End-Of-Screen Code

ATTRIBUTE CODE	END-OF-SCREEN CODE								
ATT[3:0]	0	0	0	0	0	0	0	0	0

Bits 8–0 are all zeros. Bits 12–9 will have the previously entered AC but this is not used and so these bits are "don't cares".

OSD CONTROL REGISTERS

These registers, shown in *Table 13. OSD Control Register Detail*, control the size, position, enhanced features and ROM bank selection of up to two independent OSD windows. Any bits marked as "X" are reserved and should be written to with zeros and should be ignored when the register is read. Additional register detail is provided in the *Control Register Definitions Section,* later in this document.

TABLE 13. OSD Control Register Detail

Register	Address	Default	D7	D6	D5	D4	D3	D2	D1	D0
FRMCTRL1	0x8400	0x98	HTD	ASZEN	FEN	TD	CDPR	D2E	D1E	OSE
FRMCTRL2	0x8401	0x80	PIXELS_PER_LINE[2:0]			BLINK_PERIOD[4:0]				
CHARFONTACC	0x8402	0x00	X	X	X	X	X	X	ATTR	FONT4
VBLANKDUR	0x8403	0x10	X	VBLANK_DURATION[6:0]						
CHARHTCTRL	0x8404	0x51	CHAR_HEIGHT[7:0]							
BBHLCTRLB0	0x8405	0xFF	B[1:0]		G[2:0]			R[2:0]		
BBHLCTRLB1	0x8406	0x01	X	X	X	X	X	X	X	B[2]
BBLLCTRLB0	0x8407	0x00	B[1:0]		G[2:0]			R[2:0]		
BBLLCTRLB1	0x8408	0x00	X	X	X	X	X	X	X	B[2]
CHSDWCTRLB0	0x8409	0x00	B[1:0]		G[2:0]			R[2:0]		
CHSDWCTRLB1	0x840A	0x00	X	X	X	X	X	X	X	B[2]
ROMSIGCTRL	0x840D	0x00	X	X	X	X	X	X	X	CRS
ROMSIGDATAB0	0x840E	0x00	CRC[7:0]							
ROMSIGDATAB1	0x840F	0x00	CRC[15:8]							
HSTRT1	0x8410	0x62	HPOS[7:0]							
VSTRT1	0x8411	0x32	VPOS[7:0]							
W1STRTADRL	0x8412	0x00	ADDR[7:0]							
W1STRTADRH	0x8413	0x00	X	X	X	X	X	X	X	ADDR[8]
COLWIDTH1B0	0x8414	0x00	COL[7:0]							
COLWIDTH1B1	0x8415	0x00	COL[15:8]							
COLWIDTH1B2	0x8416	0x00	COL[23:16]							
COLWIDTH1B3	0x8417	0x00	COL[31:24]							
HSTRT2	0x8418	0x56	HPOS[7:0]							
VSTRT2	0x8419	0x5B	VPOS[7:0]							
W2STRTADRL	0x841A	0x00	ADDR[7:0]							
W2STRTADRH	0x841B	0x01	X	X	X	X	X	X	X	ADDR[8]
COLWIDTH2B0	0x841C	0x00	COL[7:0]							
COLWIDTH2B1	0x841D	0x00	COL[15:8]							
COLWIDTH2B2	0x841E	0x00	COL[23:16]							

LM1246 Address Map (Continued)

TABLE 13. OSD Control Register Detail (Continued)

Register	Address	Default	D7	D6	D5	D4	D3	D2	D1	D0
COLWIDTH2B3	0x841F	0x00	COL[31:24]							
Any registers in the range of 0x8420 - 0x8426 are for National Semiconductor internal use only and should not be written to under application conditions.										
BANKSEL_0–1	0x8427	0x10	X	B1AD[2:0]			X	B0AD[2:0]		
BANKSEL_2–3	0x8428	0x32	X	B3AD[2:0]			X	B2AD[2:0]		
FADE_INTVL	0x8429	0x35	V_INTVL[3:0]				H_INVTVL[3:0]			

PREAMPLIFIER CONTROL

These registers, shown in *Table 14. LM1246 Preamplifier Interface Registers*, control the gains, DAC outputs, PLL, horizontal and vertical blanking, OSD contrast and DC offset of the video outputs. The registers, shown in *Table 15. LM1246 Preamplifier Interface Auto Size Registers*, provide measured and calculated data for the microcontroller to perform auto size and auto center functions. Any bits marked as "X" are reserved and should be written to with zeros and should be ignored when the register is read. Additional register detail is provided in the *Control Register Definitions Section*, later in this document.

TABLE 14. LM1246 Preamplifier Interface Registers

Register	Address	Default	D7	D6	D5	D4	D3	D2	D1	D0
BGAINCTRL	0x8430	0x60	X	BGAIN[6:0]						
GGAINCTRL	0x8431	0x60	X	GGAIN[6:0]						
RGAINCTRL	0x8432	0x60	X	RGAIN[6:0]						
CONTRCTRL	0x8433	0x60	X	CONTRAST[6:0]						
DAC1CTRL	0x8434	0x80	DAC1[7:0]							
DAC2CTRL	0x8435	0x80	DAC2[7:0]							
DAC3CTRL	0x8436	0x80	DAC3[7:0]							
DAC4CTRL	0x8437	0x80	DAC4[7:0]							
DACOSDDCOFF	0x8438	0x14	X	DCF[1:0]		OSD CONT[1:0]		DC OFFSET[2:0]		
GLOBALCTRL	0x8439	0x02	X	X	X	X	X	BSD	PS	BV
AUXCTRL	0x843A	0x03	X	HB_POS[3:0]				HBPOS _EN	RSV	HBD
PLLFREQRNG	0x843E	0x06	X	PLL_ AUTO	CLMP	X	OOR	VBL	PFR[1:0]	
SRTSTCTRL	0x843F	0x00	X	AID	X	X		X	X	SRST

TABLE 15. LM1246 Preamplifier Interface Auto Size Registers

Register	Address	Default	D7	D6	D5	D4	D3	D2	D1	D0
H_FP0	0x8580	0xFF	HFP[7:0]							
H_FP1	0x8581	0x07	X					HFP[10:8]		
HF_S0	0x8582	0xFF	HFL_HS[7:0]							
HF_S1	0x8583	0x03	X						HFL HS[9:8]	
H_BP0	0x8584	0xFF	HBP[7:0]							
H_BP1	0x8585	0x07	X					HBP[10:8]		
V_FP0	0x8586	0xFF	VFP[7:0]							
V_FP1	0x8587	0x07	X					VFP[10:8]		
V_SYN_D	0x8588	0xFF	VSYNC[7:0]							
V_BP0	0x8589	0xFF	VBP[7:0]							
V_BP1	0x858A	0x07	X					VBP[10:8]		

TWO-COLOR ATTRIBUTE RAM

This address range (0x8440–0x8497) contains the attribute lookup tables used for displaying two-color characters. There are 16 groups of 4 bytes each according to the format shown in *Table 16. LM1246 Two-Color Attribute Registers*. The attributes are stored starting with Color 0 (background) and each color is stored red first, green second and then blue. They may be written or read using the following address format:

LM1246 Address Map (Continued)

Address = 0x8440 + (N * 0x4) + B

where: N = Attribute number (0x0 ≤ N ≤ 0xF)

B = Attribute byte number (0x0 ≤ B ≤ 0x3)

When reading, it is OK to read only one, two, or all three bytes. When writing more than one 2-color attribute using the auto increment feature, all four bytes must be written. When writing, bytes 0 through 2 must be written in order. Bytes 0 through 2 will take effect after byte 2 is written. Since byte 3 contains all reserved bits, this byte may be written, but will have no effect. Any bits marked as "X" are reserved and should be written to with zeros and should be ignored when the register is read.

TABLE 16. LM1246 Two-Color Attribute Registers

Register	Address	D7	D6	D5	D4	D3	D2	D1	D0
ATT2C0n	0x8440 + 4n	C0B[1:0]		C0G[2:0]			C0R[2:0]		
ATT2C1n	+1	C1B[0]	C1G[2:0]			C1R[2:0]			C0B[2]
ATT2C2n	+2	X	X	EF[3:0]				C1B[2:1]	
ATT2C3n	+3	X	X	X	X	X	X	X	X

FOUR-COLOR ATTRIBUTE RAM

This address range (0x8500–0x857F), contains the attribute lookup tables used for displaying four-color characters. There are 16 groups of 8 bytes each according to the format shown in *Table 17. LM1246 Four-Color Attribute Registers*. The attributes are stored starting with Color 0 (background) and each color is stored red first, green second and then blue. They may be written or read using the following address format:

Address = 0x8500 + (N * 0x8) + B

where: N = Attribute number (0x0 ≤ N ≤ 0xF)

B = Attribute byte number (0x0 ≤ B ≤ 0x7)

When writing, bytes 0 through 2 must be written in order and bytes 4 through 6 must be written in order. Bytes 0 through 2 will take effect after byte 2 is written. Bytes 4 through 6 will take effect after byte 6 is written. Since bytes 5 and 7 contain all reserved bits, these bytes may be written, but no effect will result. When reading, it is OK to read only one, two, or all three bytes. If writing more than one 4-color attributes using the auto increment feature, all eight bytes must be written. Any bits marked as "X" are reserved and should be written to with zeros and should be ignored when the register is read.

TABLE 17. LM1246 Four-Color Attribute Registers

Register	Address	D7	D6	D5	D4	D3	D2	D1	D0
ATT4C0n	8500 + (n*8)	C0B[1:0]		C0G[2:0]			C0R[2:0]		
ATT4C1n	+1	C1B[0]	C1G[2:0]			C1R[2:0]			C0B[2]
ATT4C2n	+2	X	X	EF[3:0]				C1B[2:1]	
ATT4C3n	+3	X	X	X	X	X	X	X	X
ATT4C4n	+4	C2B[1:0]		C2G[2:0]			C2R[2:0]		
ATT4C5n	+5	C3B[0]	C3G[2:0]			C3R[2:0]			C2B[2]
ATT4C6n	+6	X	X	X	X	X	X	C3B[2:1]	
ATT4C7n	+7	X	X	X	X	X	X	X	X

Building Display Pages

THE OSD WINDOW

The Display Page RAM contains all of the 9-bit display character codes and their associated 4-bit attribute codes, and the special 13-bit page control codes — the End-Of-Line, Skip-Line parameters and End-Of-Screen characters. The LM1246 has a distinct advantage over many OSD Generators in that it allows variable size and format windows. The window size is not dictated by a fixed geometric area of RAM. Instead, 512 locations of 13-bit words are allocated in RAM for the definition of the windows, with special control codes to define the window size and shape.

Window width can be any length supported by the number of pixels per line that is selected divided by the number of pixels in a character line. It must be remembered that OSD characters displayed during the monitor blanking time will not be displayed on the screen, so the practical limit to the number of horizontal characters on a line is reduced by the number of characters within the horizontal blanking period.

The EOS code tells the OSD generator that the character codes following belong to another displayed window at the next window location. An EOS code may follow normal characters or an SL code, but never an EOL control code, because EOL is always followed by an AC plus an SL code.

WRITING TO THE PAGE RAM

The Display Page RAM can contain up to 512 of the above listed characters and control codes. Each character, or control code will consume one of the possible 512 locations. For convenience, a single write instruction to bit 3 of the Frame Control Register (0x8400) can reset the page RAM value to all zero. This should be done at power up to avoid unpredictable behaviour.

Display Window 1 will also start at the first location (corresponding to the I^2C address 0x8000). This location must

Building Display Pages (Continued)

always contain the Skip-Line (SL) code associated with the first line of Display Window 1. The attribute for this SL code must be written before the SL code itself, and will be stored in the lower four bits of this memory location. Subsequent locations should contain the characters to be displayed on line 1 of Display Window 1, until the EOL code or EOS code is written into the Display Page-RAM.

The Skip-Line parameters associated with the next line must always be written to the location immediately after the preceding line's End-Of-Line character. The only exception to this rule is when an End-Of-Screen character (value 0x0000) is encountered. It is important to note that an End-Of-Line character should not precede an End-Of-Screen character (otherwise the End-Of-Screen character will be interpreted as the next line's Skip-Line code). Instead, the End-Of-Screen code will end the line and also end the window, making it unnecessary to precede it with a EOL. The I^2C Format for writing a sequence of display characters is minimized by allowing sequential characters with the same attribute code to send in a string as follows:

Byte #1: I^2C Slave Address

Byte #2: LSB Register Address

Byte #3: MSB Register Address

Byte #4: Attribute Table Entry to use for the following Skip-Line code or characters

Byte #5: First display character, SL parameter, EOL or EOS control code

Byte #6: Second display character, SL parameter, EOL or EOS control code

Byte #7: Third display character, SL parameter, EOL or EOS control code

Byte #n: Last display character in this color sequence, SL parameter, EOL or EOS control code to use the associated Attribute Table Entry.

TABLE 18. Sequence of Transmitted Bytes

This communication protocol is known as the Auto Attribute Mode, which is also used by the LM1237 and LM1247. Please see examples of usage for this mode in the LM1247 datasheet.

ENHANCED PAGE RAM ADDRESS MODES

Since the LM1246 is able to support 9-bit character codes, usually two bytes of Page RAM information has to be sent to every location. To avoid this, the LM1246 addressing control system has 3 additional addressing modes offering increased flexibility that may be helpful in sending data to the Page RAM. Some of the left over bits in the Attribute byte are employed as data control bits to select the desired addressing mode as shown in *Table 19. Attribute Byte*. This is identified as the first byte sent in a write operation or the Page RAM's upper byte read in *Table 7. Page RAM Upper Byte Read Data*.

TABLE 19. Attribute Byte

ATTRIBUTE Byte				
X	DC[1]	DC[0]	CC[8]	ATT[3:0]

AUTO ATTRIBUTE MODE

The Auto Attribute mode is the standard LM1247 mode that is described above in the WRITING TO THE PAGE RAM section. The attribute byte is shown in *Table 20. Auto Attribute Mode*.

TABLE 20. Auto Attribute Mode

ATTRIBUTE Byte				
X	0	0	0	ATT[3:0]

When bits 6–5 are 0, the 9th character code and the 4-bit attribute code will be automatically applied to all the character codes transmitted after this attribute byte, as in the LM1237 and LM1247. This mode is useful for sending character codes that use the same attribute, and which are in the same 4 out of 8 banks of the Page ROM. A new transmission must be started to access another character that is not in the same 4 banks of the Page ROM, and no further attribute codes can follow without stopping and restarting a new transmission. The Page RAM address is automatically incremented starting with the initial LSB and MSB address in the beginning of the sequence.

TWO BYTE COMMUNICATION MODE

The Two Byte Communication mode allows different attribute and character codes to be sent within one transmission without stopping. The entire 512-character Page ROM is also fully accessible in this mode, without the need to stop and restart transmission. The attribute byte is shown in *Table 21. Two Byte Communication Mode*, and the sequence of transmitted bytes is shown in *Table 22. Sequence of Transmitted Bytes*. Either another attribute & character code pair or a STOP must follow after each character code. The Page RAM address is automatically incremented just as in the Auto Attribute mode above.

Building Display Pages (Continued)

TABLE 21. Two Byte Communication Mode

ATTRIBUTE Byte				
X	0	1	CC[8]	ATT[3:0]

TABLE 22. Sequence of Transmitted Bytes

$BA	LSB Addr.	MSB Addr.	ATTR	CC	ATTR	...	STOP

REPEAT

HALF RANDOM ADDRESS MODE

The Half Random Address mode allows different attribute and character codes to be sent within one transmission in the same way as the Two Byte Communication mode. The entire 512-character Page ROM is fully accessible in this mode, without the need to stop and restart transmission. The advantage of Half Random Addressing over the Two Byte mode is that the Page RAM addresses do not have to be written to in a sequential order. However, the Page RAM addresses cannot be entirely random, as they must be within one half of the Page RAM. A new transmission must be restarted to switch to another half of the Page RAM. The Page RAM address is not automatically incremented in this mode. This mode is very useful for modifying character codes and attributes in the first 256 locations of the Page RAM. The attribute byte is shown in *Table 23. Half Random Address Mode*, and the sequence of transmitted bytes is shown in *Table 24. Sequence of Transmitted Bytes*. Either another LSB address & attribute & character code or a STOP must follow after each character code.

TABLE 23. Half Random Address Mode

ATTRIBUTE Byte				
X	1	0	CC[8]	ATT[3:0]

TABLE 24. Sequence of Transmitted Bytes

$BA	LSB Addr.	MSB Addr.	ATTR	CC	LSB Addr.	ATTR	CC	...	STOP

REPEAT

FULL RANDOM ADDRESS MODE

The Full Random Address mode is very similar to the Half Random Address mode. However, the advantage is that the Page RAM addresses can now be entirely random. There is no longer a restriction to only one half of the Page RAM. The Page RAM address is not automatically incremented in this mode. This is very useful for modifying character codes and attributes anywhere in the Page RAM without starting a new transmission sequence. The Full Random Address mode is the most flexible mode of transmission. The attribute byte is shown in *Table 25. Full Random Address Mode*, and the sequence of transmitted bytes is shown in *Table 26. Sequence of Transmitted Bytes*. Either another LSB address & MSB address & attribute & character code or a STOP must follow after each character code.

TABLE 25. Full Random Address Mode

ATTRIBUTE Byte				
X	1	1	CC[8]	ATT[3:0]

TABLE 26. Sequence of Transmitted Bytes

$BA	LSB Addr.	MSB Addr.	ATTR	CC	LSB Addr.	MSB Addr.	ATTR	CC	...	STOP

REPEAT

Control Register Definitions

OSD INTERFACE REGISTERS

Frame Control Register 1:

FRMCTRL1 (0x8400)							
	autosize	**Fade i/o**	**trans**	**clear**	**win2**	**win1**	**OSD**
HTD	ASZEN	FEN	TD	CDPR	D2E	D1E	OsE

Control Register Definitions (Continued)

Bit 0	On-Screen Display Enable. The On-Screen Display will be disabled when this bit is a zero. When this bit is a one the On-Screen Display will be enabled. This controls both Window 1 and Window 2.
Bit 1	Display Window 1 Enable. When this bit and Bit 0 of this register are both ones, Display Window 1 is enabled. If either bit is a zero, then Display Window 1 will be disabled.
Bit 2	Display Window 2 Enable. When this bit and Bit 0 of this register are both ones, Display Window 2 is enabled. If either bit is a zero, then Display Window 2 will be disabled.
Bit 3	Clear Display Page RAM. Writing a one to this bit will result in setting all of the Display Page RAM values to zero. This bit is automatically cleared after the operation is complete. This bit is initially asserted by default at power up, and will clear itself back to zero shortly after. Thus, the default value is one only momentarily, and then will remain zero until manually asserted again or until the power is cycled.
Bit 4	Transparent Disable. When this bit is a zero, a palette color of black (i.e., color palette look-up table value of 0x00) in the first 8 palette look-up table address locations (i.e., ATT0–ATT7) will be interpreted as transparent. When this bit is a one, the color will be interpreted as black.
Bit 5	Fade In/Out Enable. When this bit is a 1, the OSD Fade In/Fade Out function is enabled. When this bit is a 0, the function is disabled.
Bit 6	Auto Size Enable. When this bit is a 1, the Auto Size function is enabled. Once video detection and measurement is completed, the bit will automatically clear itself back to 0.
Bit 7	Half Tone Disable. When this bit is a 1, the OSD Half Tone Transparency function is disabled. When this bit is a 0, the half tone transparency is enabled.

Frame Control Register 2:

FRMCTRL2 (0x8401)	
Pixels per Line	**Blink Period**
PL[2:0]	BP[4:0]

Bits 4–0	Blinking Period. These five bits set the blinking period of the blinking feature, which is determined by mulitiplying the value of these bits by 8, and then multiplying the result by the vertical field rate.
Bits 7–5	Pixels per Line. These three bits determine the number of pixels per line of OSD characters. See *Table 27. OSD Pixels per Line* which gives the maximum horizontal scan rate. Also see *Table 3. OSD Register Recommendations* since the maximum recommended scan rate is also a function of the PLLFREQRNG register, 0x843E[1:0].

TABLE 27. OSD Pixels per Line

Bits 7–5	Description	Max Horizontal Frequency (kHz)
0x0	704 pixels per line	110
0x1	768 pixels per line	110
0x2	832 pixels per line	110
0x3	896 pixels per line	110
0x4	960 pixels per line	110
0x5	1024 pixels per line	108
0x6	1088 pixels per line	102
0x7	1152 pixels per line	96

Character Font Access Register:

CHARFONTACC (0x8402)							
Reserved						**Select**	**Plane**
X	X	X	X	X	X	ATTR	FONT4

Bit 0	This is the Color Bit Plane Selector. This bit must be set to 0 to read or write a two-color attribute from the range 0x0000 to 0x2FFF. When reading or writing four-color attributes from the range 0x3000 to 0x3FFF, this bit is set to 0 for the least significant plane and to 1 for the most significant plane. It is also required to set this bit to read the individual bit planes of the four color character fonts in 0x3000 to 0x3FFF and 0x7000 to 0x7FFF.
Bit 1	This is the Character/Attribute Selector. This applies to reads from the Display Page RAM (address range 0x8000–0x81FF). When a 0, the character code is returned and when a 1, the attribute code is returned.

Control Register Definitions (Continued)

Bits 7–2	Reserved. These should be set to zero.

Vertical Blank Duration Register:

VBLANKDUR (0x8403)	
Res'd	**Vertical Blanking Duration**
X	VB[6:0]

Bits 6–0	This register determines the duration of the vertical blanking signal in scan lines. When vertical blanking is enabled, it is recommended that this register be set to a number greater than 0x0A.
Bit 7	Reserved. This bit should be set to zero.

OSD Character Height Register:

CHARHTCTRL (0x8404)
CH[7:0]

Bits 7–0	This register determines the OSD character height as described in the section Constant Character Height Mechanism. The values of this register is equal to the approximate number of OSD height compensated lines required on the screen, divided by 4. This value is not exact due to the approximation used in scaling the character. Example: If approximately 384 OSD lines are required on the screen (regardless of the number of scan lines) then the Character Height Control Register is programmed with 81 (0x51).

Enhanced Feature Register 1: **Button Box Highlight Color**

BBHLCTRLB1 (0x8406)							BBHLCTRLB0 (0x8405)		
Reserved							**Highlight - Green**	**Highlight - Red**	**Highlight - Blue**
X	X	X	X	X	X	X	G[2:0]	R[2:0]	B[2:0]

Bits 8–0	These determine the button box highlight color.
Bits 15–9	Reserved. These bits should be set to zero.

Enhanced Feature Register 2: **Button Box Lowlight Color**

BBLLCTRLB1 (0x8408)							BBLLCTRLB0 (0x8407)		
Reserved							**Lowlight - Green**	**Lowlight - Red**	**Lowlight - Blue**
X	X	X	X	X	X	X	G[2:0]	R[2:0]	B[2:0]

Bits 8–0	These determine the button box lowlight color.
Bits 15–9	Reserved. These bits should be set to zero.

Enhanced Feature Register 3: **Heavy Button Box Lowlight/Shading/Shadow**

CHSDWCTRLB1 (0x840A)							CHSDWCTRLB0 (0x8409)		
Reserved							**Shadow - Green**	**Shadow - Red**	**Shadow - Blue**
X	X	X	X	X	X	X	G[2:0]	R[2:0]	B[2:0]

Bits 8–0	These registers determine the heavy button box lowlight, shading or shadow color.
Bits 15–9	Reserved. These bits should be set to zero.

ROM Signature Control Register:

ROMSIGCTRL (0x840D)							
Reserved							**check**
X	X	X	X	X	X	X	CRS

Control Register Definitions (Continued)

Bit 0	This controls the calculation of the ROM signature. Setting this bit causes the ROM to be read sequentially and a 16-bit checksum calculated over the 256 characters. The sum, modulo 65535, is stored in the ROM Signature Data Register, and this bit is then automatically cleared.
Bits 7–1	Reserved. These should be set to zero.

ROM Signature Data:

ROMSIGDATAB1 (0x840F)	ROMSIGDATAB0 (0x840E)
16-Bit Checksum	
CRC[15:0]	

Bits 15–0	This is the checksum of the 256 ROM characters truncated to 16 bits (modulo 65535). All devices with the same masked ROM will have the same checksum.

Display Window 1 Horizontal Start Address:

HSTRT1 (0x8410)
Window 1 Horizontal Start Location
1H[7:0]

Bits 7–0	There are two possible OSD windows which can be displayed simultaneously or individually. This register determines the horizontal start position of Window 1 in OSD pixels (not video signal pixels). The actual position, to the right of the horizontal flyback pulse, is determined by multiplying this register value by 4 and adding 30. Due to pipeline delays, the first usable start location is approximately 42 OSD pixels following the horizontal flyback time. For this reason, we recommend this register be programmed with a number larger than 2, otherwise improper operation may result.

Display Window 1 Vertical Start Address:

VSTRT1 (0x8411)
Window 1 Vertical Start Address
1V[7:0]

Bits 7–0	This register determines the Vertical start position of the Window 1 in constant-height character lines (not video scan lines). The actual position is determined by multiplying this register value by 2. (Note: each character line is treated as a single auto-height character pixel line, so multiple scan lines may actually be displayed in order to maintain accurate position relative to the OSD character cell size. See the Constant Character Height Mechanism section.) This register should be set so the entire OSD window is within the active video.

Display Window 1 Start Address:

W1STRTADRH (0x8413)							W1STRTADRL (0x8412)
Reserved							Window 1 Start Address
X	X	X	X	X	X	X	1AD[8:0]

Bits 8–0	This register determines the starting address of Display Window 1 in the Display Page RAM. The power-on default of 0x00 starts Window 1 at the beginning of the Page RAM (0x8000). This first address location always contains the SL code for the first line of Display Window 1. This register is new for the LM1246 and allows Window 1 to start anywhere in the Page RAM rather than just at 0x8000. Note that the address this points to in Page RAM must always contain the SL code for the first line of the window.
Bits 15–9	These bits are reserved and should be set to zero.

Display Window 1 Column Width:

COLWIDTH1B3 (0x8417)	COLWIDTH1B2 (0x8416)
Window 1 Column Width - High Bytes	
COL[31:16]	

Control Register Definitions (Continued)

COLWIDTH1B1 (0x8415)	COLWIDTH1B0 (0x8414)
Window 1 Column Width - Low Bytes	
COL[15:0]	

Bits 31–0	These are the Display Window 1 Column Width 2x Enable Bits. These thirty-two bits correspond to columns 31–0 of Display Window 1, respectively. A value of zero indicates the column will have normal width (12 pixels). A "1" indicates the column will be twice as wide as normal (24 pixels). For the double wide case, each Character Font pixel location will be displayed twice, in two consecutive horizontal pixel locations. The user should note that if more than 32 display characters are programmed to reside on a line, then all display characters after the first thirty-two will have normal width (12 pixels).

Display Window 2 Horizontal Start Address:

HSTRT2 (0x8418)
Window 2 Horizontal Start Address
2H[7:0]

Bits 7–0	This register determines the horizontal start position of Window 2 in OSD pixels (not video signal pixels). The actual position, to the right of the horizontal flyback pulse, is determined by multiplying this register value by 4 and adding 30. Due to pipeline delays, the first usable start location is approximately 42 OSD pixels following the horizontal flyback time. For this reason, we recommend this register be programmed with a number larger than 2, otherwise improper operation may result.

Display Window 2 Vertical Start Address:

VSTRT2 (0x8419)
Window 2 Vertical Start Address
2V[7:0]

Bits 7–0	This register determines the Vertical start position of Window 2 in constant-height character lines (not video scan lines). The actual position is determined by multiplying this register value by 2. (Note: each character line is treated as a single auto-height character pixel line, so multiple scan lines may actually be displayed in order to maintain accurate position relative to the OSD character cell size. (See the *Constant Character Height Mechanism* section.) This register should be set so the entire OSD window is within the active video.

Display Window 2 Start Address:

W2STRTADRH (0x841B)							W2STRTADRL (0x841A)
Reserved							**Window 2 Start Address**
X	X	X	X	X	X	X	2AD[8:0]

Bits 8–0	This register determines the starting address of Display Window 2 in the Display Page RAM. The power-on default of 0x10 starts Window 2 at the midpoint of the Page RAM (0x8100). This location always contains the SL code for the first line of Window 2.
Bits 15–9	These bits are reserved and should be set to zero.

Display Window 2 Column Width:

COLWIDTH2B3 (0x841F)	COLWIDTH2B2 (0x841E)
Window 2 Column Width - High Bytes	
COL[31:16]	

COLWIDTH2B1 (0x841D)	COLWIDTH2B0 (0x841C)
Window 2 Column Width - Low Bytes	
COL[15:0]	

Control Register Definitions (Continued)

Bits 31–0	These are the Display Window 2 Column Width 2x Enable Bits. These thirty-two bits correspond to columns 31–0 of Display Window 2, respectively. A value of zero indicates the column will have normal width (12 OSD pixels). A value of one indicates the column will be twice as wide as normal (24 OSD pixels). For the double wide case, each Character Font pixel location will be displayed twice, in two consecutive horizontal pixel locations. The user should note that if more than 32 display characters are programmed to reside on a line, then all display characters after the first thirty-two will have normal width (12 pixels).

ROM Bank Select Register A:

BANKSEL_0-1 (0x8427)			
Res'd	**Bank Select 1**	**Res'd**	**Bank Select 0**
X	B1AD[2:0]	X	B1AD[2:0]

Bits 2–0	This three-bit field determines the ROM bank (0–7) selected when bits 7–6 of the character address in Page RAM are 00 (Character Address = 00xxxxxb)
Bit 3	This bit is reserved and should be set to 0.
Bits 6–4	This three-bit field determines the ROM bank (0–7) selected when bits 7–6 of the character address in Page RAM are 01 (Character Address = 01xxxxxb)
Bit 7	This bit is reserved and should be set to 0.

ROM Bank Select Register B:

BANKSEL_2-3 (0x8428)			
Res'd	**Bank Select 3**	**Res'd**	**Bank Select 2**
X	B3AD[2:0]	X	B2AD[2:0]

Bits 2–0	This three-bit field determines the ROM bank (0–7) selected when bits 7–6 of the Page RAM address are 10 (Character Address = 10xxxxxb)
Bit 3	This bit is reserved and should be set to 0.
Bits 6–4	This three-bit field determines the ROM bank (0–7) selected when bits 7–6 of the Page RAM address are 11 (Character Address = 11xxxxxb)
Bit 7	This bit is reserved and should be set to 0.

The actual address for any character in ROM is formed, in logic, from the address in the Page RAM, by this sequence (also see *Figure 13*):

1. The upper 2 bits of the character address in Page RAM are used to address one of the four 3-bit fields in Bank Select Register A or Bank Select Register B. As shown in *Table 28. Address Lookup*, depending on which of the four values is present, the corresponding 3-bit bank address is obtained from the BANKSEL_0, BANKSEL_1, BANKSEL_2, or BANKSEL_3 field shown in the last column.

TABLE 28. Address Lookup

Character Address in Page RAM	Upper Two Bits	Three-Bit Bank Address Source
00xxxxxb	00b	B0AD[2:0]
01xxxxxb	01b	B1AD[2:0]
10xxxxxb	10b	B2AD[2:0]
11xxxxxb	11b	B3AD[2:0]

Control Register Definitions (Continued)

2. Then, the 3-bit address obtained from B0AD[2:0], B1AD[2:0], B2AD[2:0] and B3AD[2:0] are used to select four of the eight 2 or 4 color ROM banks as shown in *Table 29. Resulting ROM Bank Address*. The BxAD[2:0] column gives the range of three-bit addresses and the next two columns give the corresponding ROM address range and the character type.

TABLE 29. Resulting ROM Bank Address

BxAD[2:0]	Character ROM Address Range	ROM Character Type
000b	0x000–0x03F	2 Color
001b	0x040–0x07F	2 Color
010b	0x080–0x0BF	2 Color
011b	0x0C0–0x0FF	4 Color
100b	0x100–0x13F	2 Color
101b	0x140–0x17F	2 Color
110b	0x180–0x1BF	2 Color
111b	0x1C0–0x1FF	4 Color

3. In summary, the final ROM character address is formed by concatenating (combining end to end) the three bits of the corresponding Bank Address Register with the lower six bits of the original character address in RAM. Since just the two highest bits of the Page RAM address are used, only 4 banks can be addressed at one time.

Fade In/Fade Out Interval Register:

FADE_INTVL (0x8429)	
Vertical Interval	**Horizontal Interval**
V_INTVL[3:0]	H_INTVL[3:0]

Bits 7–4	These three bits determine the interval for fading in or fading out the OSD window in the vertical direction.
Bits 3–0	These three bits determine the interval for fading in or fading out the OSD window in the horizontal direction.

Pre-Amplifier Interface Registers

Blue Channel Gain:

BGAINCTRL (0x8430)	
Res'd	**Blue Gain**
X	BG[6:0]

Bits 6–0	This register determines the gain of the blue video channel. This affects only the blue channel whereas the contrast register (0x8433) affects all channels.
Bit 7	Reserved and should be set to zero.

Green Channel Gain:

GGAINCTRL (0x8431)	
Res'd	**Green Gain**
X	GG[6:0]

Bits 6–0	This register determines the gain of the green video channel. This affects only the green channel whereas the contrast register (0x8433) affects all channels.
Bit 7	Reserved and should be set to zero.

Red Channel Gain:

RGAINCTRL (0x8432)	
Res'd	**Red Gain**
X	RG[6:0]

Pre-Amplifier Interface Registers (Continued)

Bits 6–0	This register determines the gain of the red video channel. This affects only the red channel whereas the contrast register (0x8433) affects all channels.
Bit 7	Reserved and should be set to zero.

Contrast Control:

CONTRCTRL (0x8433)	
Res'd	**Contrast**
X	CG[6:0]

Bits 6–0	This register determines the contrast gain and affects all three channels, blue, red and green.
Bit 7	Reserved and should be set to zero.

DAC 1 Output Level:

DAC1CTRL (0x8434)
DAC 1 Output Level
BC[7:0]

Bits 7–0	This register determines the output of DAC 1. The full-scale output is determined by bit 5 of the DAC Config, OSD Contrast & DC Offset Register.

DAC 2 Output Level:

DAC2CTRL (0x8435)
DAC 2 Output Level
GC[7:0]

Bits 7–0	This register determines the output of DAC 2. The full-scale output is determined by bit 5 of the DAC Config, OSD Contrast & DC Offset Register.

DAC 3 Output Level:

DAC3CTRL (0x8436)
DAC 3 Output Level
RC[7:0]

Bits 7–0	This register determines the output of DAC 3. The full-scale output is determined by bit 5 of the DAC Config, OSD Contrast & DC Offset Register (0x8438).

DAC 4 Output Level:

DAC4CTRL (0x8437)
DAC 4 Output Level
BA[7:0]

Bits 7–0	This register determines the output of DAC 4. The output of this DAC can be scaled and mixed with the outputs of DACs 1–3 as determined by bit 6 of the DAC Config, OSD Contrast & DC Offset Register.

DAC Config, OSD Contrast & DC Offset:

DACOSDDCOFF (0x8438)			
Res'd	**DAC Options**	**OSD Contrast**	**DC Offset**
X	DCF[1:0]	OSD[1:0]	DC[2:0]

Bits 2–0	These determine the DC offset of the three video outputs, blue, red and green.
Bits 4–3	These determine the contrast of the internally generated OSD.

Pre-Amplifier Interface Registers (Continued)

Bit 5	When this bit is a 0, the full-scale outputs of DACs 1–3 are 0.5V to 4.5V. When it is a 1, the full-scale level is 0.5V to 2.5V.
Bit 6	When this bit is a 0, the DAC 4 output is independent. When it is a 1, the DAC 4 output is scaled by 50% and added to the outputs of DACs 1–3.
Bit 7	Reserved and should be set to zero.

Global Video Control:

GLOBALCTRL (0x8439)							
					Bank	**Power**	**Blank**
X	X	X	X	X	BSD	PS	BV

Bit 0	When this bit is a 1, the video outputs are blanked (set to black level). When it is a 0, video is not blanked.
Bit 1	When this bit is a 1, the analog sections of the preamplifier are shut down for low power consumption. When it is a 0, the analog sections are enabled.
Bit 2	This bit is a 0 by default, where Bank Select is enabled. In this mode, Page RAM addressing is in the standard mode identical to the LM1247. When this bits a 1, the Bank Select is disabled, and full 512 character address operation is used.
Bits 7–3	Reserved.

Auxiliary Control:

AUXCTRL (0x843A)				
Reserved	**Horizontal Blank Position**	**H. Blank**	**Reserved**	**H Blnk**
X	HBPOS[30]	HBPOS_EN	X	HBD

Bit 0	When this bit is a 0, the horizontal blanking input at pin 24 is gated to the video outputs to provide horizontal blanking. When it is a 1, the horizontal blanking at the outputs is disabled.
Bit 1	Reserved
Bit 2	When this bit is a 1, the position of the Horizontal Blanking pulse can be programmably varied relative to the horizontal flyback in number of pixels. When this bit is a 0, which is by default, the horizontal blanking pulse position will not be programmable.
Bits 6–3	These 4 bits determine the position of the Horizontal Blanking Pulse with respect to the horizontal flyback in number of pixels.
Bit 7	Reserved

PLL Range:

PLLFREQRNG (0x843E)						
Res'd	**PLL Auto Mode**	**Clamp**	**Res'd**	**OSD**	**V Blank**	**PLL Pre-calibration**
X	PLL_AUTO	CLMP	X	OOR	VBL	PFR[1:0]

Bit 1–0	These bits must be set to 0 to pre-calibrate the PLL Auto feature.
Bit 2	This is the Vertical Blanking register. When this bit is a 1, vertical blanking is gated to the video outputs. When set to a 0, the video outputs do not have vertical blanking.
Bit 3	This is the OSD override bit. This should be set to 0 for normal operation. When set to a 1, the video outputs are disconnected and OSD only is displayed. This is useful for the OSD display of special conditions such as "No Signal" and "Input Signal Out of Range", to avoid seeing unsynchronized video.
Bit 4	Reserved and should be set to zero.
Bit 5	This is the Clamp Polarity bit. When set to a 0, the LM1246 expects a positive going clamp pulse. When set to a 1, the expected pulse is negative going.
Bit 6	When this bit is set, the PLL Auto Mode will automatically determine the optimum frequency range of the Phase Locked Loop.

Pre-Amplifier Interface Registers (Continued)

Bit 7	Reserved and should be set to zero.

Software Reset and Test Control:

SRTSTCTRL (0x843F)							
Res'd		**Reserved**					**Reset**
X	AID	X	X	X	X	X	SRST

Bit 0	When this bit is a 1, all registers except this one are loaded with their default values. All operations are aborted, except data transfers in progress on the I^2C compatible bus. This bit clears itself when the reset is complete.
Bit 5–1	Reserved and should be set to zero.
Bit 6	This bit disables the register Auto-Increment feature of the I^2C compatible protocol. When set to a 1, Auto-Increment is disabled and when a 0, AI is enabled.
Bit 7	Reserved and should be set to zero.

Pre-Amplifier Interface Registers (Continued)

Horizontal Front Porch Duration:

H_FP1 (0x8581)					H_FP0 (0x8580)
Reserved					Horizontal Front Porch Duration
X	X	X	X	X	HFP[10:0]

Bit 10–0	This is an 11-bit wide register that records the lowest measured value of the horizontal front porch during video detect. When no video is detected, this register should return a value of zero. Once measurement is completed and the auto size enable bit has cleared itself back to 0, the measured data is ready to be read by the microcontroller. Reading this register before that may give erroneous results. This register resets to default values, ready to record new measured values when the auto size enable bit is set again.

Horizontal Flyback or Sync Duration:

HF_S1 (0x8583)						HF_S0 (0x8582)
Reserved						Horizontal Flyback or Sync Duration
X	X	X	X	X	X	HFL_HS[9:0]

Bits 9–0	This is a 10-bit wide register that records the measured value of the horizontal flyback or sync during video detect. When no video is detected, this register should return a value of zero. Once measurement is completed and the auto size enable bit has cleared itself back to 0, the measured data is ready to be read by the microcontroller. Reading this register before that may give erroneous results. This register resets to default values, ready to record new measured values when the auto size enable bit is set again.

Horizontal Back Porch Duration:

HF_BP1 (0x8585)					HF_BP0 (0x8584)
Reserved					Horizontal Back Porch Duration
X	X	X	X	X	HBP[10:0]

Bits 10–0	This is an 11-bit wide register that records the lowest measured value of the horizontal back porch during video detect. When no video is detected, the sum of this register and the horizontal flyback or sync should be within 1 pixel of the total number of pixels per line. Once measurement is completed and the auto size enable bit has cleared itself back to 0, the measured data is ready to be read by the microcontroller. Reading this register before that may give erroneous results. This register resets to default values, ready to record new measured values when the auto size enable bit is set again.

Vertical Front Porch Duration:

V_FP1 (0x8587)					V_FP0 (0x8586)
Reserved					Vertical Front Porch Duration
X	X	X	X	X	VBP[10:0]

Bits 10–0	This is an 11-bit wide register that records the lowest measured value of the vertical front porch in terms of horizontal line periods during video detect. When no video is detected, this register should return a value of zero. Once measurement is completed and the auto size enable bit has cleared itself back to 0, the measured data is ready to be read by the microcontroller. Reading this register before that may give erroneous results. This register resets to default values, ready to record new measured values when the auto size enable bit is set again.

Vertical Flyback or Sync Duration:

V_SYN_D (0x8588)
Vertical Flyback or Sync Duration
VSYNC[7:0]

Pre-Amplifier Interface Registers (Continued)

Bits 7–0	This is an 8-bit wide register that records the measured value of the vertical flyback or sync in terms of horizontal line periods during video detect. Once measurement is completed and the auto size enable bit has cleared itself back to 0, the measured data is ready to be read by the microcontroller. Reading this register before that may give erroneous results. This register resets to default values, ready to record new measured values when the auto size enable bit is set again.

Vertical Back Porch Duration:

V_BP1 (0x858A)					V_BP0 (0x8589)
Reserved					Vertical Back Porch Duration
X	X	X	X	X	VBP[10:0]

Bits 10–0	This is an 11-bit wide register that records the lowest measured value of the vertical back porch in terms of horizontal line periods during video detect. When no video is detected, the sum of this register and the vertical flyback or sync should be within 1 line of the total number of lines per field. Once measurement is completed and the auto size enable bit has cleared itself back to 0, the measured data is ready to be read by the microcontroller. Reading this register before that may give erroneous results. This register resets to default values, ready to record new measured values when the auto size enable bit is set again.

Attribute Table and Enhanced Features

Each display character and SL in the Display Page RAM will have a 4–bit Attribute Table entry associated with it. The user should note that two-color display characters and four-color display characters use two different Attribute Tables, effectively providing 16 attributes for two-color display characters and 16 attributes for four-color display characters.

For two-color characters, the attribute contains the code for the 9-bit foreground color (Color 1), the code for the 9-bit background color (Color 0), and the character's enhanced features (Button Box, Blinking, Heavy Box, Shadowing, Bordering, etc.).

For four-color characters, the attribute contains the code for the 9-bit Color 0, the code for the 9-bit Color 1, the code for the 9-bit Color 2, the code for the 9-bit Color 3, and the character's enhanced features (Button Box, Blinking, Heavy Box, Shadowing, Bordering, etc.).

TWO COLOR ATTRIBUTE FORMAT

The address range for an attribute number, 0 ≤ n ≤ 15, is provided in *Table 31. Attribute Tables and Corresponding Addresses*.

ATT2C3n (0x8443+n*4)								ATT2C2n (0x8442+n*4)			
Reserved										Enhanced Feature	Color 1 -
X	X	X	X	X	X	X	X	X	X	EFB[3:0]	C1B[2:1]

ATT2C1n (0x8441+n*4)			ATT2C0n (0x8440+n*4)		
Blue	Color 1 - Green	Color 1 - Red	Color 0 - Blue	Color 0 - Green	Color 0 - Red
C2B0	C1G[2:0]	C1R[2:0]	C0B[2:0]	C0G[2:0]	C0R[2:0]

Bits 8–0	These nine bits determine the background color (color1), which is displayed when the corresponding OSD pixel is a 0.
Bits 17–9	These nine bits determine the foreground color (color2), which is displayed when the corresponding OSD pixel is a 1.
Bits 21–18	These are the enhanced feature (EF) bits, which determine which feature is applied to the displayed character. The features and their corresponding codes are shown in *Table 30. Enhanced Feature Descriptions*.
Bits 31–22	Reserved and should be set to zero.

TABLE 30. Enhanced Feature Descriptions

Bits 21–18	Feature Description
0000b	Normal Display
0001b	Blinking
0010b	Shadowing
0011b	Bordering

Attribute Table and Enhanced Features (Continued)

TABLE 30. Enhanced Feature Descriptions (Continued)

Bits 21–18	Feature Description
0100b	RESERVED
0101b	RESERVED
0110b	RESERVED
0111b	RESERVED
1000b	Raised Box
1001b	Blinking and Raised Box
1010b	Depressed Box
1011b	Blinking and Depressed Box
1100b	Heavy Raised Box
1101b	Blinking and Heavy Raised Box
1110b	Heavy Depressed Box
1111b	Blinking and Heavy Depressed Box

FOUR COLOR ATTRIBUTE FORMAT

The address range for an attribute number, 0 ≤ n ≤ 15, is provided in *Table 31. Attribute Tables and Corresponding Addresses*.

ATT4C7n (0x8507+n*4)								ATT4C6n (0x8506+n*4)						
Reserved														Color 3 -
X	X	X	X	X	X	X	X	X	X	X	X	X	X	C3B[2:1]

ATT4C5n (0x8505+n*4)			ATT4C4n (0x8504+n*4)		
Blue	Color 3 - Green	Color 3 - Red	Color 2 - Blue	Color 2 - Green	Color 2 - Red
C3B0	C3G[2:0]	C3R[2:0]	C2B[2:0]	C2G[2:0]	C2R[2:0]

ATT4C3n (0x8503+n*4)								ATT4C2n (0x8502+n*4)			
Reserved										Enhanced Features	Color 1 -
X	X	X	X	X	X	X	X	X	X	EFB[3:0]	C1B[2:1]

ATT4C1n (0x8501+n*4)			ATT4C0n (0x8500+n*4)		
Blue	Color 1 - Green	Color 1 - Red	Color 0 - Blue	Color 0 - Green	Color 0 - Red
C1B0	C1G[2:0]	C1R[2:0]	C0B[2:0]	C0G[2:0]	C0R[2:0]

Bits 8–0	These nine bits determine color 0 which is displayed when the corresponding OSD pixel code is 00b.
Bits 17–9	These nine bits determine color 1 which is displayed when the corresponding OSD pixel code is 01b.
Bits 21–18	These are the enhanced feature (EF) bits, which determine which feature is applied to the displayed character. The features and their corresponding codes are shown in *Table 30. Enhanced Feature Descriptions*.
Bits 31–22	Reserved and should be set to zero.
Bits 40–32	These nine bits determine color2, which is displayed when the corresponding OSD pixel code is 10b.
Bits 49–41	These nine bits determine color3, which is displayed when the corresponding OSD pixel code is 11b.
Bits 63–50	Reserved and should be set to zero.

TABLE 31. Attribute Tables and Corresponding Addresses

Attribute Number, n	Two-Color Attribute Table Address	Four-Color Attribute Table Address
0000b	0x8440–0x8443	0x8500–0x8507
0001b	0x8444–0x8447	0x8508–0x850F
0010b	0x8448–0x844B	0x8510–0x8517

Attribute Table and Enhanced Features (Continued)

TABLE 31. Attribute Tables and Corresponding Addresses (Continued)

Attribute Number, n	Two-Color Attribute Table Address	Four-Color Attribute Table Address
0011b	0x844C–0x844F	0x8518–0x851F
0100b	0x8450–0x8453	0x8520–0x8527
0101b	0x8454–0x8457	0x8528–0x852F
0110b	0x8458–0x845B	0x8530–0x8537
0111b	0x845C–0x845F	0x8538–0x853F
1000b	0x8460–0x8463	0x8540–0x8547
1001b	0x8464–0x8467	0x8548–0x854F
1010b	0x8468–0x846B	0x8550–0x8557
1011b	0x846C–0x846F	0x8558–0x855F
1100b	0x8470–0x8473	0x8560–0x8567
1101b	0x8474–0x8477	0x8568–0x856F
1110b	0x8478–0x847B	0x8570–0x8577
1111B	0x847C–0x847F	0x8578–0x857F

BUTTON BOX FORMATION

The value of the most significant Enhanced Feature Bit (EFB3) determines when to draw the left, right, bottom and top sides of a Box. EFB1 denotes whether a box is raised or depressed, and EFB2 denotes whether the box is normal or "heavy". For normal boxes, the lowlight color is determined by the color code stored in the register EF2. For the heavy box feature, the lowlight is determined by the color code stored in register EF3. Boxes are created by a "pixel override" system that overwrites character cell pixel information with either the highlight color (EF1) or low light shadow (EF2 or EF3) of the box. Only the top pixel line of the character and the right edge of the character can be overwritten by the pixel override system.

To form a complete box, the left hand edge of a box is created by overwriting the pixels in the right most column of the preceding character to one being enclosed by the box. The bottom edge of a box is created by either—

- overwriting the pixels in the top line of the character below the character being enclosed by the box, or
- overwriting the pixels in the top line of the skipped lines below, in the case where skip lines are present below a boxed character.

Characters should be designed so that button boxes will not interfere with the character.

These are the limitations resulting from the button box formation methodology:

- No box may use the left most display character in the Display Window, or it will have no left side of the Box. To create a box around the left most displayed character, a transparent "blank" character must be used in the first character position. This character will not be visible on the screen, but allows the formation of the box.
- At least one skip line must be used beneath characters on the bottom row, if a box is required around any characters on this row in order to accommodate the bottom edge of the box.
- Skipped lines cannot be used within a box covering several rows.
- Irregular shaped boxes, (i.e., other than rectangular), may have some missing edges.

Operation of the Shadow Feature

The shadow feature is created as follows: As each 12-bit line in the character is called from ROM, the line immediately preceding it is also called and used to create a "pixel override" mask. Bits 11 through 1 of the preceding line are compared to bits 10 through 0 of the current character line. Each bit X in the current line is compared to bit X+1 in the preceding line (i.e., the pixel above and to the left of the current pixel). Note that bit 11 of the current line cannot be shadowed. A pixel override output mask is then created. When a pixel override output is 1 for a given pixel position, the color of that pixel must be substituted with the color code stored in the register EF3. Please see *Figure 27* for an example.

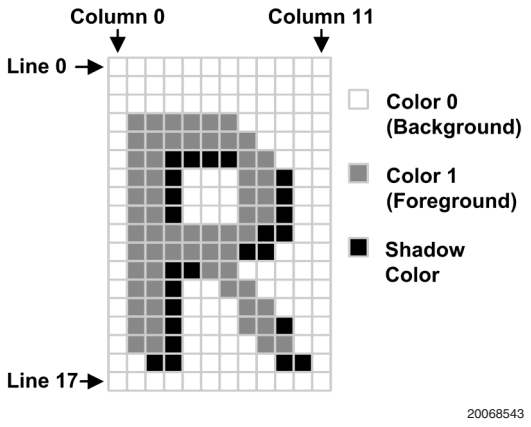


FIGURE 27. Operation of the Shadow Feature

Operation of the Bordering Feature

Borders are created in a similar manner to the shadows, using the pixel override system to overwrite pixel data with a pixel color set by EF3. However, instead of comparing just the previous line to the current line, all pixels surrounding a given pixel are examined.

The pixel override is created as follows: As each 12-bit line in the character is called from ROM, the character line immediately above and the line immediately below are also called. A "Pixel Override" output mask is then created by looking at

Attribute Table and Enhanced Features (Continued)

all pixels surrounding the pixel. When a black override output is 1 for a given pixel position, X, the color of that pixel changed to the color code stored in the register EF3.

Because the shadowing relies upon information about the pixels surrounding any given pixel, the bordering system may not operate correctly for pixels in the perimeter of the character (line 0 and 17, columns 0 and 11).

Constant Character Height Mechanism

The CRT monitor scan circuits ensure that the height of the displayed image remains constant so the physical height of a single displayed pixel row will decrease as the total number of image scan lines increases. As the OSD character matrix has a fixed number of lines, C, (where C = 18), then the character height will reduce as the number of scan lines increase, assuming a constant image height. To prevent this, the OSD generator repeats some of the lines in the OSD character in order to maintain a constant height percentage of the vertical image size.

In the LM1247, an approximation method is used to determine which lines are repeated, and how many times each line is repeated. The constant character height mechanism will not decrease the OSD character matrix to less than 18 lines.

Display Window 1 to Display Window 2 Spacing

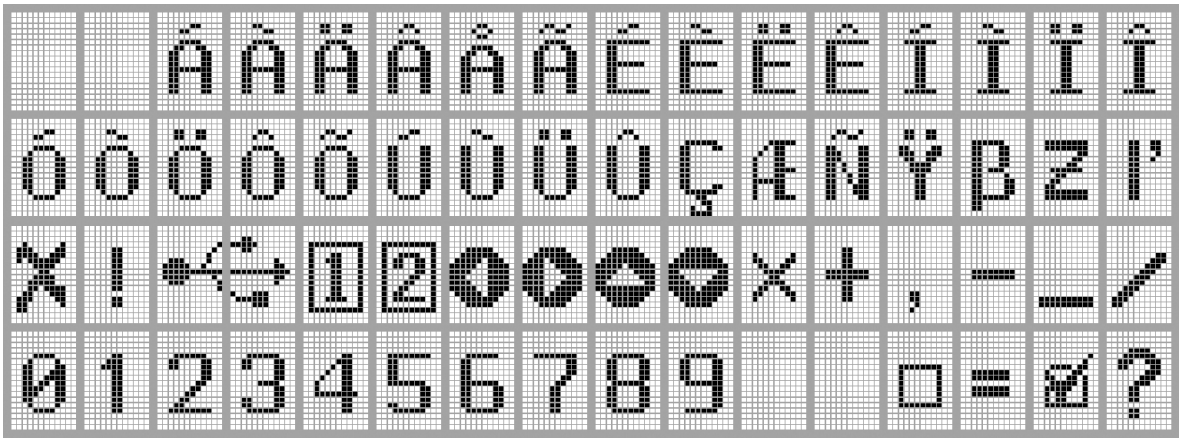
There is no required vertical spacing between Display Window 1 and Display Window 2, but they should not overlap. There must be a two-character horizontal space between Display Window 1 and Display Window 2 for proper operation of both windows or undefined results may occur.

Evaluation Character Fonts

The character font for evaluation of the LM1246 is shown in *Figure 28* through *Figure 35*, where each represents one of the 8 available ROM banks. Each bank is shown with increasing character address going from upper left to lower right. The actual font will depend on customer customization requirements.

Note that the first two character codes of the two-color font in ROM bank 4 (0x00 and 0x01) are carried over from the LM1237 ROM where they were reserved for the End-Of-Screen (EOS) and End-Of-Line (EOL) codes respectively.

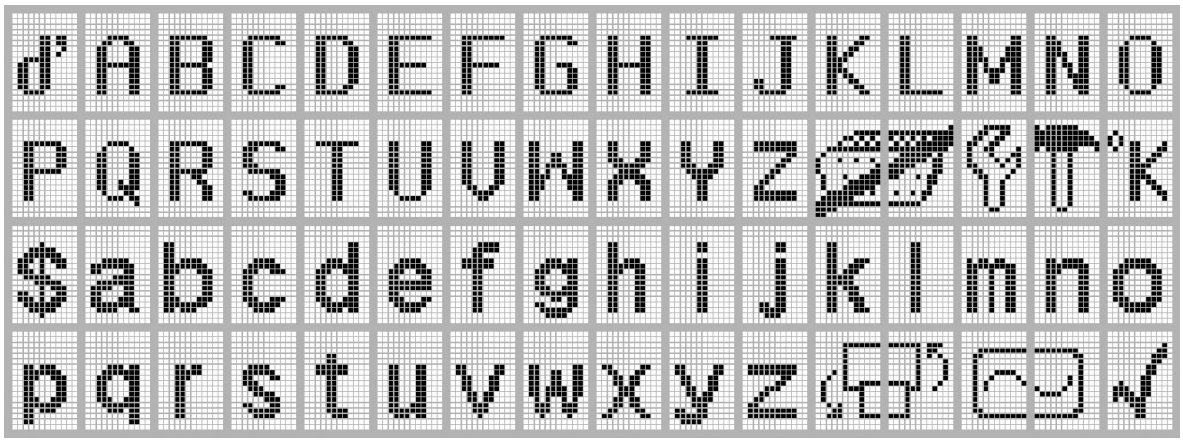
In the case of the LM1246, these two locations can be used for displayable characters as long as they are not needed when this bank is addressed from Bank Select Register 0. If it is addressed from Bank Select Registers 1, 2 or 3, then these two lower characters will be usable. Please see the section “END-OF-LINE AND END-OF-SCREEN CODES”. Similarly, the first two characters in any bank, which is addressed from Bank Select Register 0 will not be usable since those addresses will be interpreted as the EOL and EOS codes.



20068544

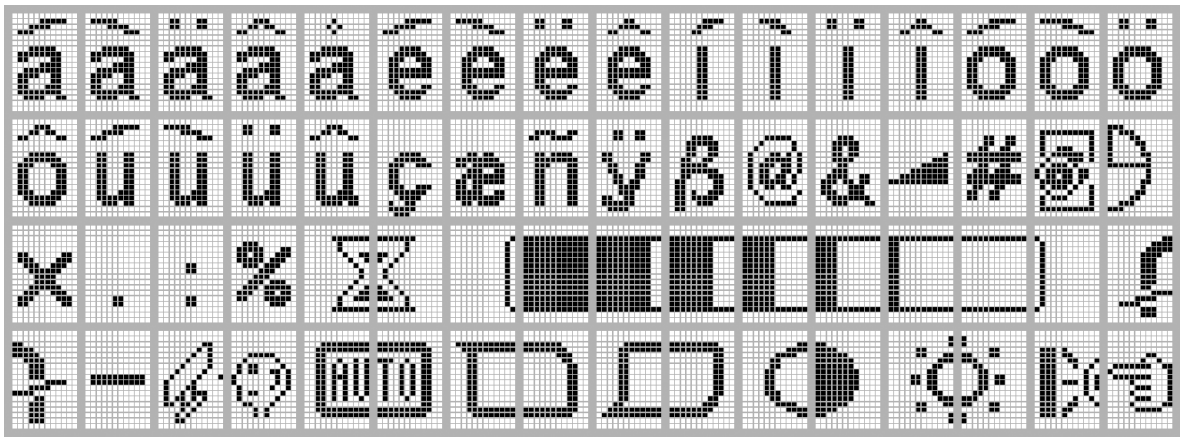
FIGURE 28. ROM Bank 0 Two Color Character Font

Attribute Table and Enhanced Features (Continued)



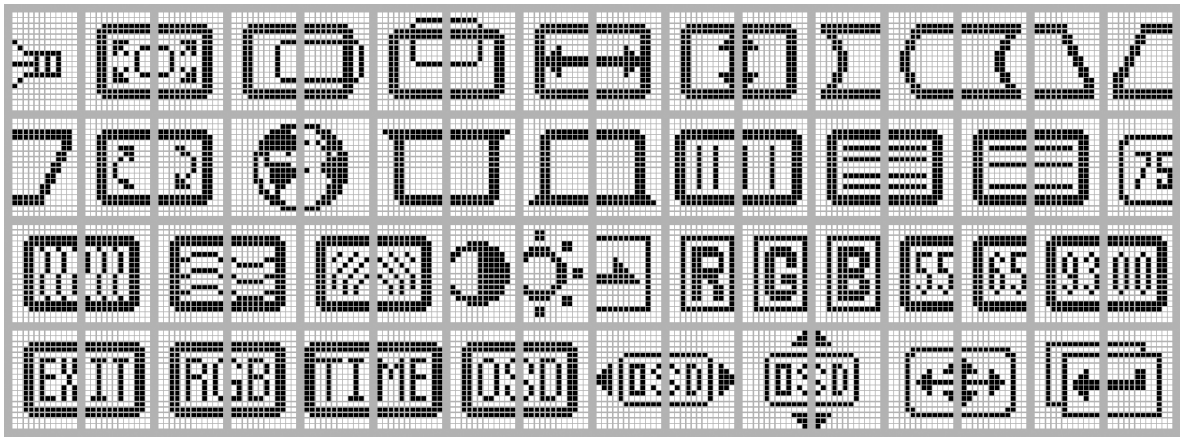
20068545

FIGURE 29. ROM Bank 1 Two Color Character Font



20068546

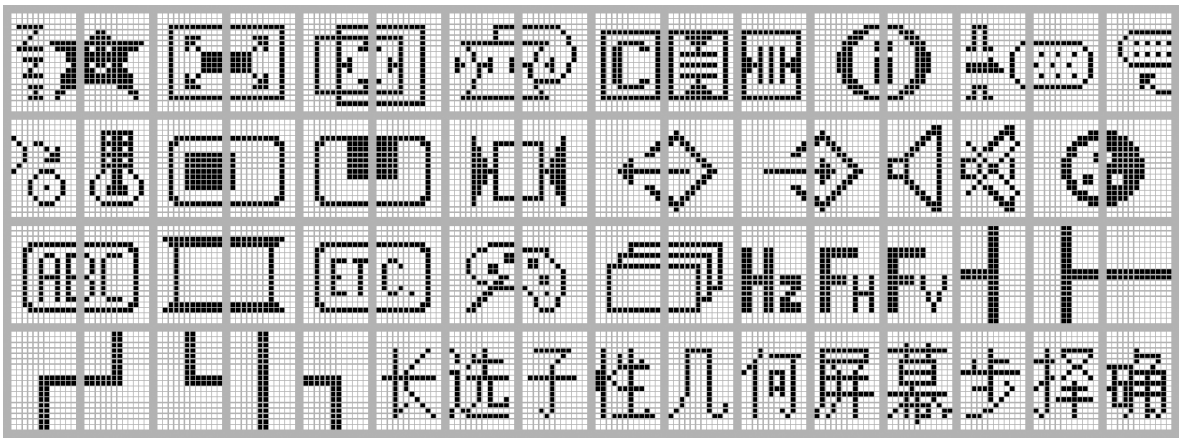
FIGURE 30. ROM Bank 2 Two Color Character Font



20068547

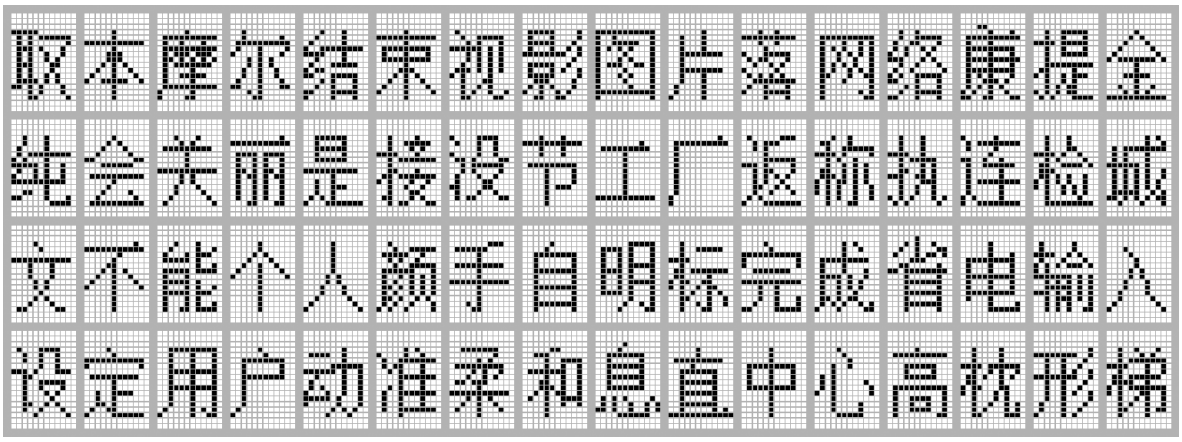
FIGURE 31. ROM Bank 3 Four Color Character Font

Attribute Table and Enhanced Features (Continued)



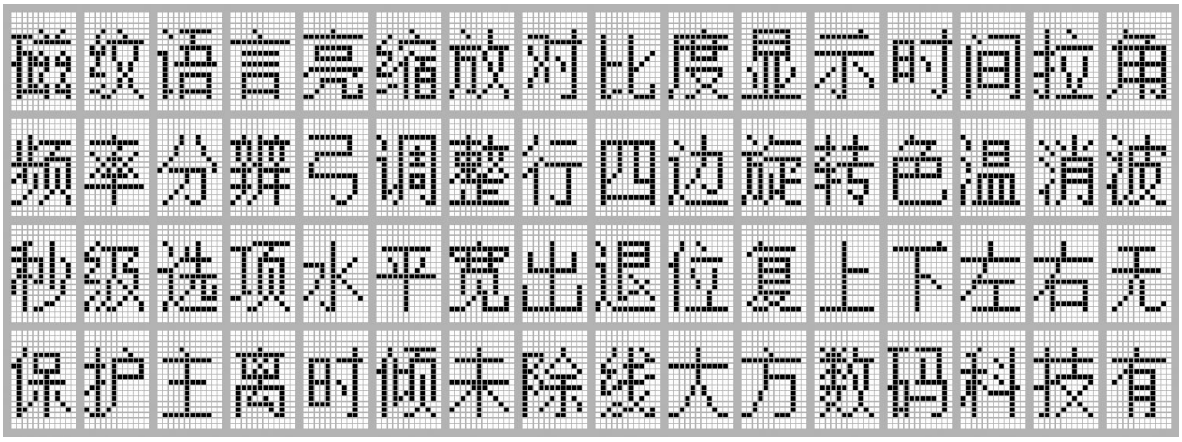
20068548

FIGURE 32. ROM Bank 4 Two Color Character Font



20068549

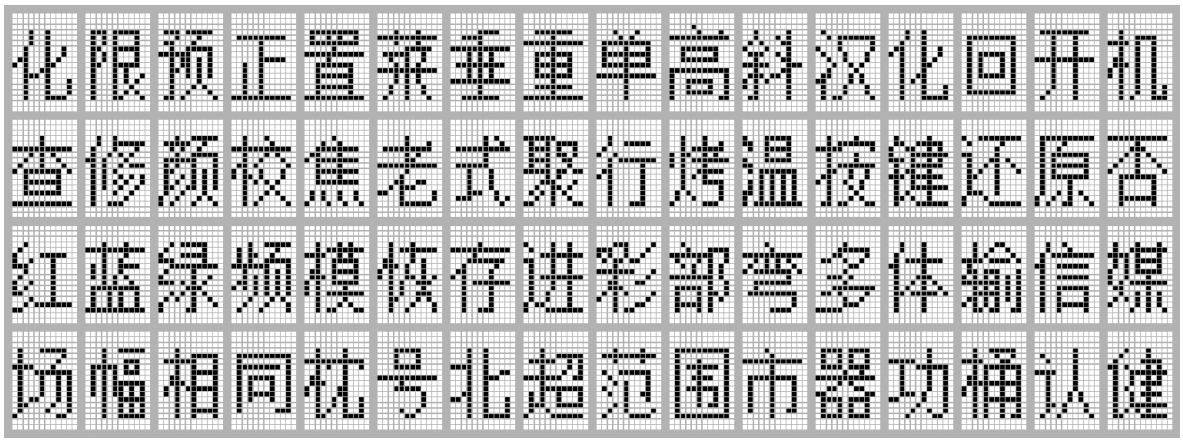
FIGURE 33. ROM Bank 5 Two Color Character Font



20068550

FIGURE 34. ROM Bank 6 Two Color Character Font

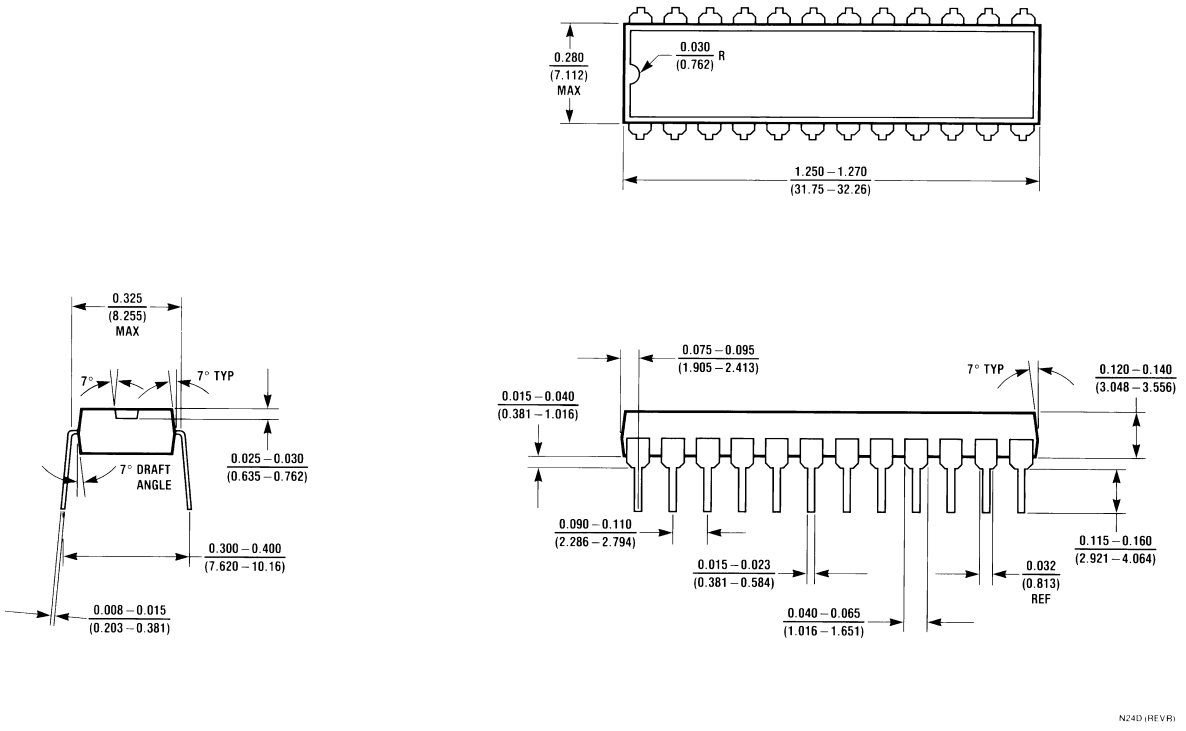
Attribute Table and Enhanced Features (Continued)



20068551

FIGURE 35. ROM Bank 7 Four Color Character Font

Physical Dimensions inches (millimeters) unless otherwise noted



24-Lead DIP Molded Plastic
Package Order Number LM1246AAA/NA
NS Package Number N24D

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