National Semiconductor

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LM3311
Step-Up PWM DC/DC Converter with Integrated LDO, Op-Amp, and Gate Pulse Modulation Switch

General Description

The LM3311 is a step-up DC/DC converter integrated with an LDO, an Operational Amplifier, and a gate pulse modulation switch. The boost (step-up) converter is used to generate an adjustable output voltage and features a low R_{DSON} internal switch for maximum efficiency. The operating frequency is selectable between 660kHz and 1.28MHz allowing for the use of small external components. An external soft-start pin enables the user to tailor the soft-start time to a specific application and limit the inrush current. The LDO also has an adjustable output voltage and is stable using ceramic output capacitors. The Op-Amp is capable of sourcing/sinking 135mA of current (typical). The gate pulse modulation switch can operate with a VGH voltage of 5V to 30V. The LM3311 is available in a low profile 24-lead LLP package.

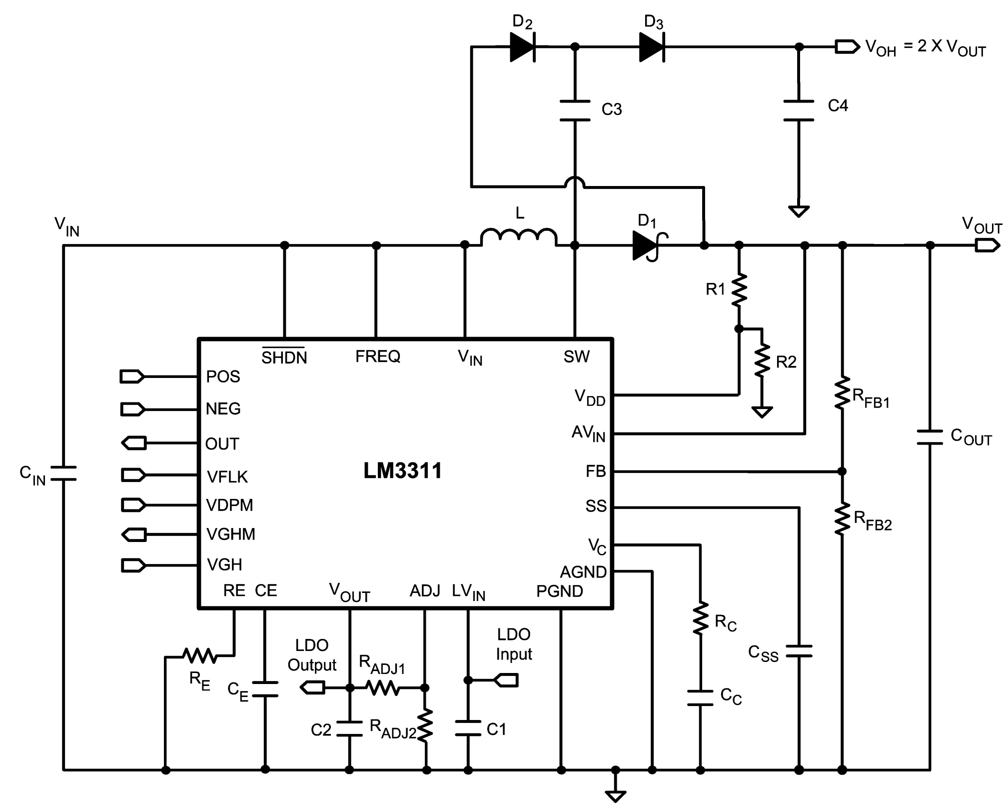
Features

- Boost converter with a 2A, 0.18Ω switch
- Boost output voltage adjustable up to 20V
- Operating voltage range of 2.5V to 7V
- 660kHz/1.28MHz pin selectable switching frequency
- Adjustable soft-start function
- Input undervoltage protection
- Over temperature protection
- Adjustable low dropout linear regulator (LDO)
- Integrated Op-Amp
- Integrated gate pulse modulation (GPM) switch
- 24-Lead LLP package

Applications

- TFT Bias Supplies
- Portable Applications

Typical Application Circuit



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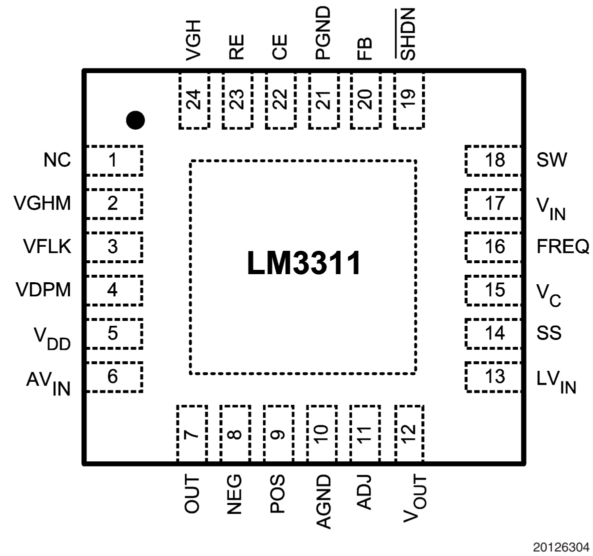
Connection Diagram



LLP-24 (Top View)
θ_{JA}=37˚C/W

Ordering Information

Order Number	Spec.	Package Type	NSC Package Drawing	Supplied As
LM3311SQ		LLP-24	SQA24A	1000 units/reel tape and reel
LM3311SQX		LLP-24	SQA24A	4500 units/reel tape and reel
LM3311SQ	NOPB	LLP-24	SQA24A	1000 units/reel tape and reel
LM3311SQX	NOPB	LLP-24	SQA24A	4500 units/reel tape and reel

Pin Descriptions

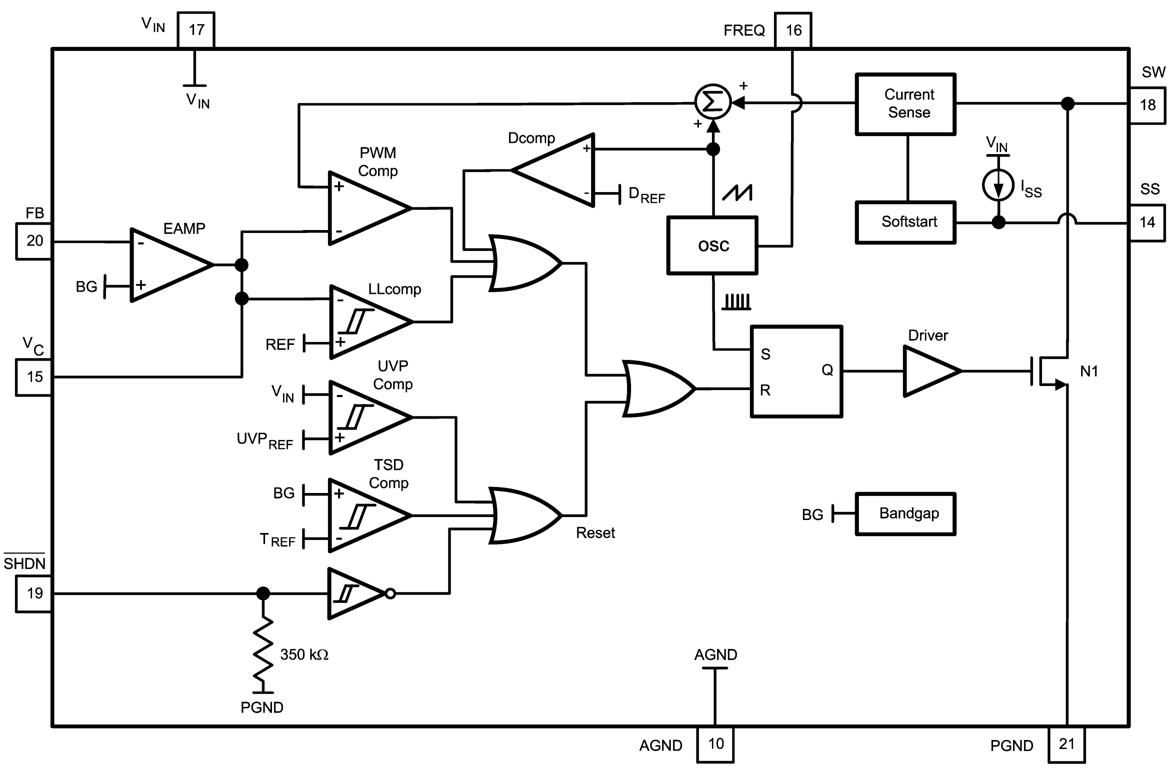
Pin	Name	Function
1	NC	Not internally connected.
2	VGHM	Output of GPM circuit. This output directly drives the supply for the gate driver circuits.
3	VFLK	Determines when the TFT LCD is on or off. This is controlled by the timing controller in the LCD module.
4	VDPM	VDPM pin is the enable signal for the GPM block. Pulling this pin high enables the GPM while pulling this pin low disables it. VDPM is used for timing sequence control.
5	V_{DD}	Reference input for gate pulse modulation (GPM) circuit. The voltage at V_{DD} is used to set the lower VGHM voltage.
6	AV_{IN}	Op-Amp analog power input.
7	OUT	Output of the Op-Amp.
8	NEG	Negative input terminal of the Op-Amp.
9	POS	Positive input terminal of the Op-Amp.
10	AGND	Analog ground for the step-up regulator, LDO, and Op-Amp. Connect directly to DAP and PGND beneath the device.
11	ADJ	LDO output voltage feedback input.
12	V_{OUT}	LDO regulator output.

Pin Descriptions (Continued)

Pin	Name	Function
13	LV_{IN}	LDO power input.
14	SS	Boost converter soft start pin.
15	V_C	Boost compensation network connection. Connected to the output of the voltage error amplifier.
16	FREQ	Switching frequency select input. Connect this pin to V_{IN} for 1.28MHz operation and AGND for 660kHz operation.
17	V_{IN}	Boost converter and GPM power input.
18	SW	Boost power switch input. Switch connected between SW pin and PGND pin.
19	$\overline{SHDN}$	Shutdown pin. Active low, pulling this pin low will disable the LM3311.
20	FB	Boost output voltage feedback input.
21	PGND	Power Ground. Source connection of the step-up regulator NMOS switch and ground for the GPM circuit. Connect AGND and PGND directly to the DAP beneath the device.
22	CE	Connect capacitor from this pin to AGND.
23	RE	Connect a resistor between RE and PGND.
24	VGH	GPM power supply input. VGH range is 5V to 30V.
DAP		Die Attach Pad. Internally connected to GND. Connect AGND and PGND pins directly to this pad beneath the device.

Block Diagrams

Boost Converter



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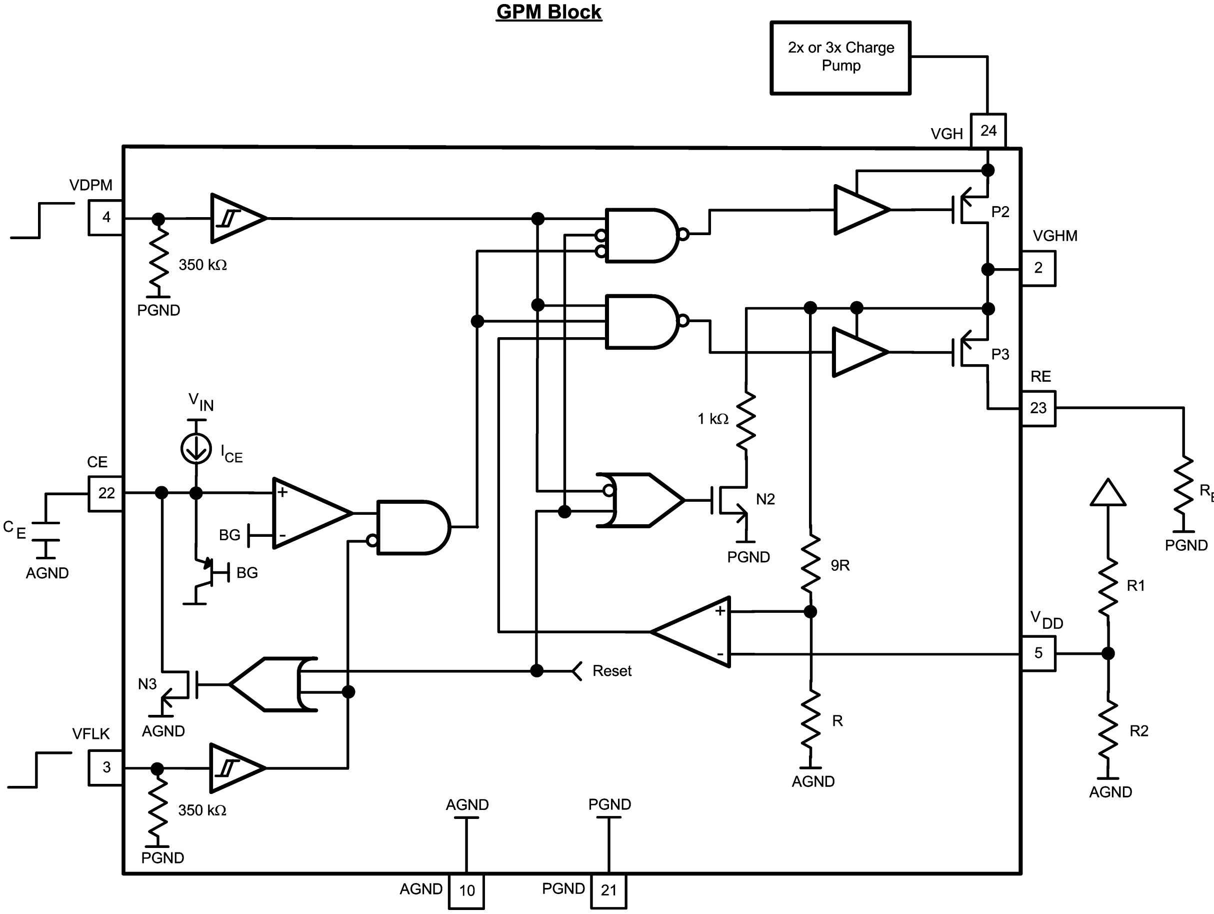
Block Diagrams (Continued)

GPM Block



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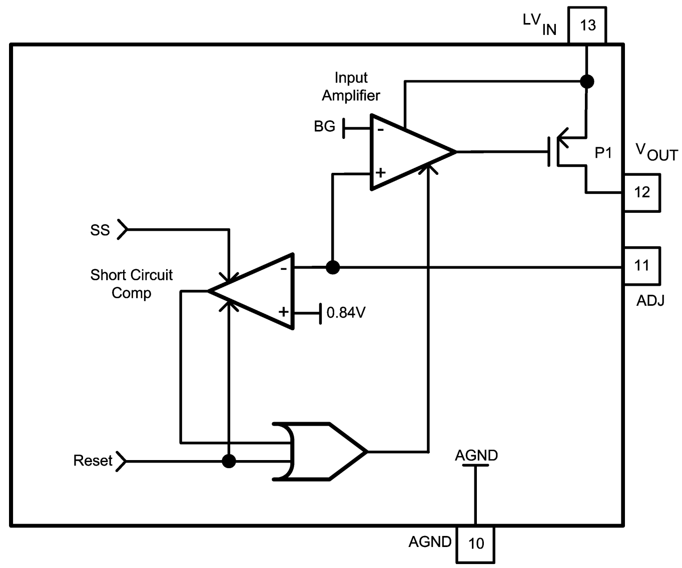
Block Diagrams (Continued)

LDO



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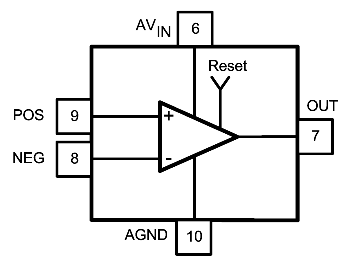
Op-Amp



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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

V_{IN}	7.5V
SW Voltage	21V
FB Voltage	V_{IN}
V_C Voltage (Note 2)	1.265V ± 0.3V
$\overline{SHDN}$ Voltage	7.5V
FREQ	V_{IN}
AV_{IN}	12V
Amplifier Inputs/Output	Rail-to-Rail
LV_{IN}	7.5V
ADJ Voltage	LV_{IN}
V_{OUT}	LV_{IN}
VGH Voltage	31V
VGHM Voltage	VGH
VFLK, VDPM, V_{DD} Voltage	7.5V
CE Voltage (Note 2)	1.265 + 0.3V
RE Voltage	VGH
Maximum Junction Temperature	150˚C
Power Dissipation(Note 3)	Internally Limited
Lead Temperature	300˚C
Vapor Phase (60 sec.)	215˚C
Infrared (15 sec.)	220˚C
ESD Susceptibility (Note 4)	
Human Body Model	2kV

Operating Conditions

Operating Junction Temperature Range (Note 5)	–40˚C to +125˚C
Storage Temperature	–65˚C to +150˚C
Supply Voltage	2.5V to 7V
Maximum SW Voltage	20V
VGH Voltage Range	5V to 30V
Op-Amp Supply, AV_{IN}	4V to 12V
LDO Supply, LV_{IN}	2.5V to 7V

Electrical Characteristics

Specifications in standard type face are for T_J = 25˚C and those with **boldface type** apply over the full **Operating Temperature Range** (T_J = –40˚C to +125˚C). Unless otherwise specified, V_{IN} = LV_{IN} = 2.5V and I_L = 0A.

Symbol	Parameter	Conditions	Min (Note 5)	Typ (Note 6)	Max (Note 5)	Units
I_Q	Quiescent Current	FB = 2V (Not Switching)		690	**1100**	µA
		$V_{\overline{SHDN}}$ = 0V		0.04	0.5 **8.5**	
		660kHz Switching		2.1	**2.8**	mA
		1.28MHz Switching		3.1	**4.0**	
V_{FB}	Feedback Voltage		**1.231**	1.263	**1.287**	V
$\%V_{FB}/\Delta V_{IN}$	Feedback Voltage Line Regulation	2.5V ≤ V_{IN} ≤ 7V	**-0.26**	0.089	**0.42**	%/V
I_{CL}	Switch Current Limit (Note 7)	(Note 8)	**2.0**	2.6		A
I_B	FB Pin Bias Current (Note 9)			27	**160**	nA
I_{SS}	SS Pin Current		**8.5**	11	**13.5**	µA
V_{SS}	SS Pin Voltage		**1.20**	1.24	**1.28**	V
V_{IN}	Input Voltage Range		**2.5**		**7**	V
g_m	Error Amp Transconductance	ΔI = 5µA	**26**	74	**133**	µmho
A_V	Error Amp Voltage Gain			69		V/V
D_{MAX}	Maximum Duty Cycle	f_S = 660kHz	**80**	91		%
		f_S = 1.28MHz	**80**	89		
f_S	Switching Frequency	FREQ = Ground	**440**	660	**760**	kHz
		FREQ = V_{IN}	**1.0**	1.28	**1.5**	MHz
$I_{\overline{SHDN}}$	Shutdown Pin Current	$V_{\overline{SHDN}}$ = 2.5V		8	**13.5**	µA
		$V_{\overline{SHDN}}$ = 0.3V		1	**2**	
I_L	Switch Leakage Current	V_{SW} = 20V		0.03	**5**	µA
R_{DSON}	Switch R_{DSON}	I_{SW} = 500mA		0.18	**0.35**	Ω
Th_{SHDN}	$\overline{SHDN}$ Threshold	Output High, V_{IN} = 2.5V to 7V	**1.4**			V
		Output Low, V_{IN} = 2.5V to 7V			**0.4**	

Electrical Characteristics (Continued)

Specifications in standard type face are for T_J = 25˚C and those with **boldface type** apply over the full **Operating Temperature Range** (T_J = −40˚C to +125˚C). Unless otherwise specified, V_{IN} = LV_{IN} = 2.5V and I_L = 0A.

Symbol	Parameter	Conditions	Min (Note 5)	Typ (Note 6)	Max (Note 5)	Units
UVP	Undervoltage Protection Threshold	On Threshold (Switch On)	**2.5**	2.4		V
		Off Threshold (Switch Off)		2.3	**2.1**	
I_{FREQ}	FREQ Pin Current	FREQ = V_{IN} = 2.5V		2.7	**13.5**	µA

Electrical Characteristics

Specifications in standard type face are for T_J = 25˚C and those with **boldface type** apply over the full **Operating Temperature Range** (T_J = −40˚C to +125˚C). Unless otherwise specified V_{IN} = LV_{IN} = 2.5V and AV_{IN} = 8V.

Operational Amplifier

Symbol	Parameter	Conditions	Min (Note 5)	Typ (Note 6)	Max (Note 5)	Units
V_{OS}	Input Offset Voltage	Buffer configuration, V_O = AV_{IN}/2, no load		5.7	**15**	mV
I_B	Input Bias Current (POS Pin)	Buffer configuration, V_O = AV_{IN}/2, no load (Note 9)		200	**550**	nA
V_{OUT} Swing		Buffer, R_L=2kΩ, V_O min.		0.001	**0.03**	V
		Buffer, R_L=2kΩ, V_O max.	**7.9**	7.97		
AV_{IN}	Supply Voltage		**4**		**12**	V
Is+	Supply Current	Buffer, V_O = AV_{IN}/2, No Load		1.5	**7.8**	mA
I_{OUT}	Output Current	Source	**90**	138	**195**	mA
		Sink	**105**	135	**175**	

Electrical Characteristics

Specifications in standard type face are for T_J = 25˚C and those with **boldface type** apply over the full **Operating Temperature Range** (T_J = −40˚C to +125˚C). Unless otherwise specified V_{IN} = LV_{IN} = 2.5V.

Gate Pulse Modulation

Symbol	Parameter	Conditions	Min (Note 5)	Typ (Note 6)	Max (Note 5)	Units
VFLK	VFLK Voltage Levels	Rising edge threshold			**1.4**	V
		Falling edge threshold	**0.4**			
VDPM	VDPM Voltage Levels	Rising edge threshold			**1.4**	V
		Falling edge threshold	**0.4**			
$V_{DD(TH)}$	V_{DD} Threshold	VGHM = 30V	**2.8**	3	**3.3**	V
		VGHM = 5V	**0.4**	0.5	**0.7**	
I_{VFLK}	VFLK Current	VFLK = 1.5V		4.8	**11**	µA
		VFLK = 0.3V		1.1	**2.5**	
I_{VDPM}	VDPM Current	VDPM = 1.5V		4.8	**11**	µA
		VDPM = 0.3V		1.1	**2.5**	
I_{VGH}	VGH Bias Current	VGH = 30V, VFLK High		59	**300**	µA
		VGH = 30V, VFLK Low		11	**35.5**	
$R_{VGH-VGHM}$	VGH to VGHM Resistance	20mA Current, VGH = 30V		14	**28.5**	Ω
$R_{VGHM-RE}$	VGHM to RE Resistance	20mA Current, VGH = VGHM = 30V		27	**55**	
$R_{VGHM(OFF)}$	VGH Resistance	VDPM is Low, VGHM = 2V		1.2	**1.7**	kΩ
I_{CE}	CE Current	CE = 0V	**40**	57	**71**	µA
$V_{CE(TH)}$	CE Voltage Threshold		**1.16**	1.22	**1.30**	V

Electrical Characteristics

Specifications in standard type face are for T_J = 25˚C and those with **boldface type** apply over the full **Operating Temperature Range** (T_J = −40˚C to +125˚C). Unless otherwise specified V_{IN} = LV_{IN} =2.5V.

Low Dropout Linear Regulator (LDO)

Symbol	Parameter	Conditions	Min (Note 5)	Typ (Note 6)	Max (Note 5)	Units
LV_{IN}	Input Voltage Range		**2.5**		**7**	V
V_{ADJ}	ADJ Pin Voltage	LV_{IN} = 3V and 7V	**1.197**	1.263	**1.289**	V
I_{ADJ}	ADJ Pin Current (Note 9)			28	**380**	nA
$\%V_{ADJ}/\Delta V_{IN}$	ADJ Voltage Line Regulation	LV_{IN} = 3V to 7V, LDO_{OUT} = 2.8V, no load	**-2.6**	0.032	**1.4**	%
$\%V_{ADJ}/\Delta I_L$	LDO_{OUT} Load Regulation	I_{OUT} = 10mA to 300mA, LV_{IN} = 3.3V, LDO_{OUT} = 2.8V	**-11.6**	2.931	**8**	%
I_{QL}	LV_{IN} Quiescent Current	Device enabled		290	**425**	µA
		Device shut down			**10.5**	µA
V_{DO}	Dropout Voltage	350mA load, LDO_{OUT} = 2.8V	**218**	409	**674**	mV
$V_{ADJ(LOW)}$	V_{ADJ} Short Circuit Disable Threshold	LV_{IN} = 3.3V		0.85	**0.9**	V

Note 1: Absolute maximum ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions for which the device is intended to be functional, but device parameter specifications may not be guaranteed. For guaranteed specifications and test conditions, see the Electrical Characteristics.

Note 2: Under normal operation the V_C and CE pins may go to voltages above this value. The maximum rating is for the possibility of a voltage being applied to the pin, however the V_C and CE pins should never have a voltage directly applied to them.

Note 3: The maximum allowable power dissipation is a function of the maximum junction temperature, T_J(MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. See the Electrical Characteristics table for the thermal resistance of various layouts. The maximum allowable power dissipation at any ambient temperature is calculated using: P_D (MAX) = ($T_{J(MAX)}$ − T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown.

Note 4: The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin per JEDEC standard JESD22-A114.

Note 5: All limits guaranteed at room temperature (standard typeface) and at temperature extremes (bold typeface). All room temperature limits are 100% production tested. All limits at temperature extremes are guaranteed via correlation using standard Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL).

Note 6: Typical numbers are at 25˚C and represent the most likely norm.

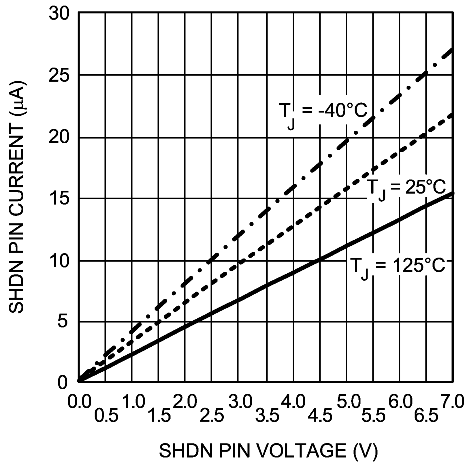
Note 7: Duty cycle affects current limit due to ramp generator.

Note 8: Current limit at 0% duty cycle. See TYPICAL PERFORMANCE section for Switch Current Limit vs. V_{IN}

Note 9: Bias current flows into pin.

Typical Performance Characteristics

$\overline{SHDN}$ Pin Current vs. $\overline{SHDN}$ Pin Voltage



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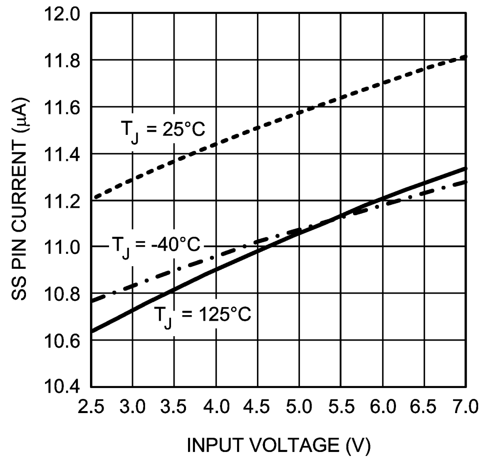
SS Pin Current vs. Input Voltage



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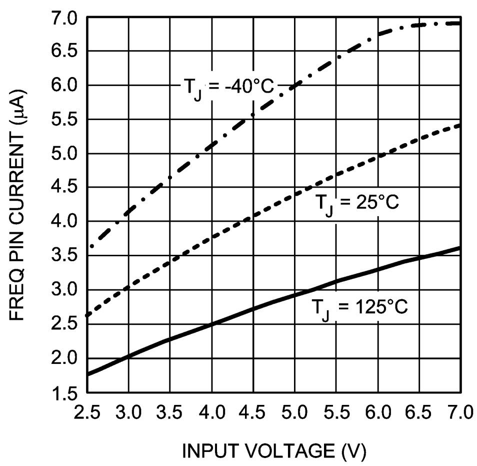
FREQ Pin Current vs. Input Voltage



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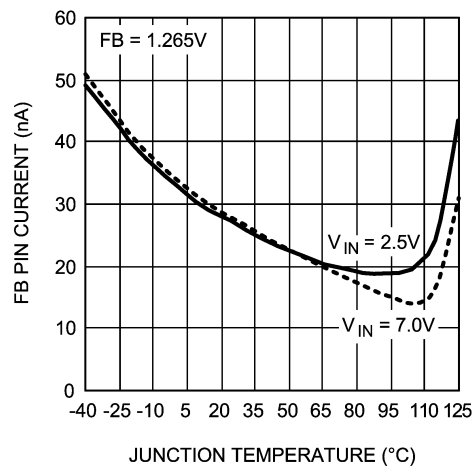
FB Pin Current vs. Temperature



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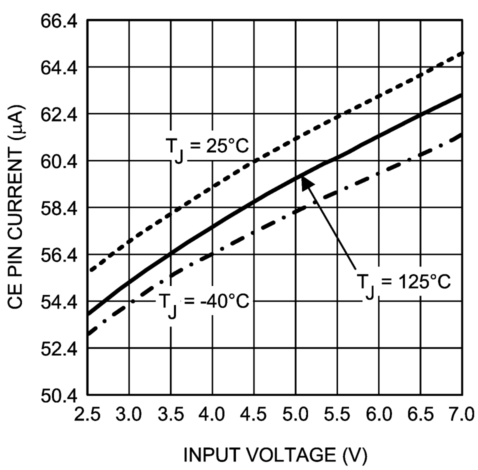
CE Pin Current vs. Input Voltage



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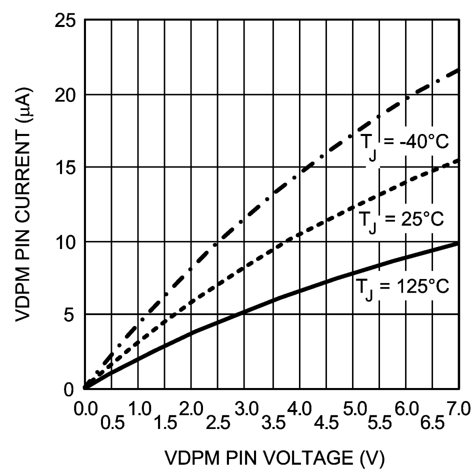
VDPM Pin Current vs. VDPM Pin Voltage



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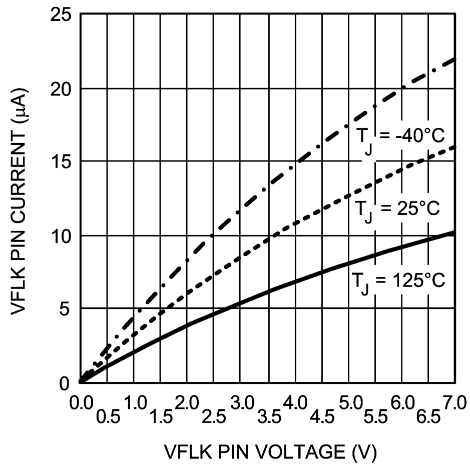
Typical Performance Characteristics (Continued)

VFLK Pin Current vs. VFLK Pin Voltage



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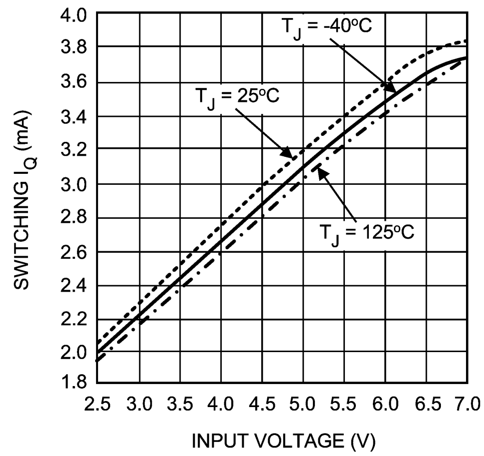
660kHz Switching Quiescent Current vs. Input Voltage



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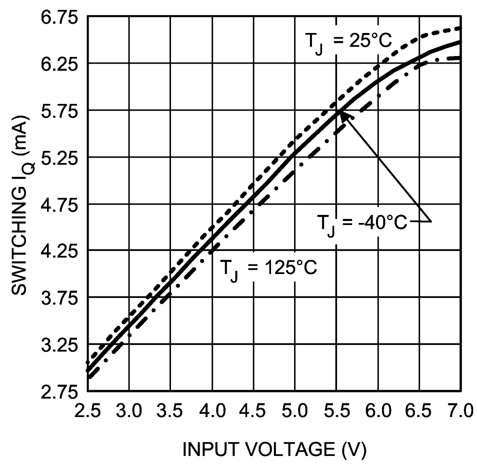
1.28MHz Switching Quiescent Current vs. Input Voltage



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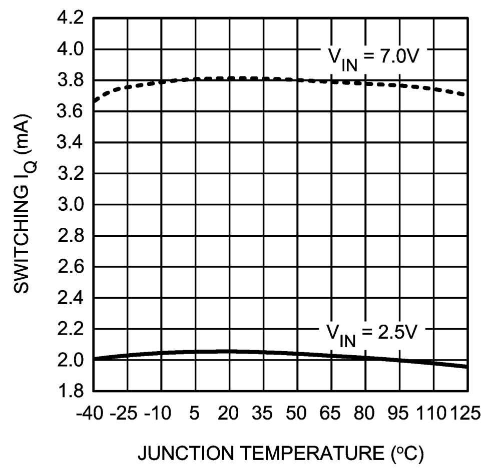
660kHz Switching Quiescent Current vs. Temperature



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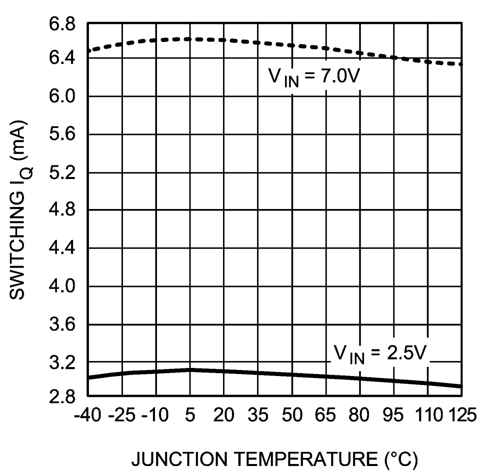
1.28MHz Switching Quiescent Current vs. Temperature



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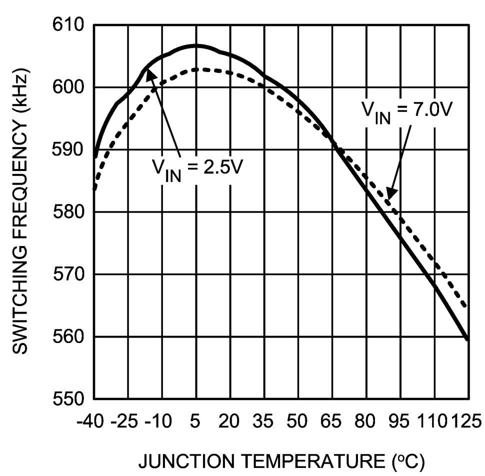
660kHz Switching Frequency vs. Temperature



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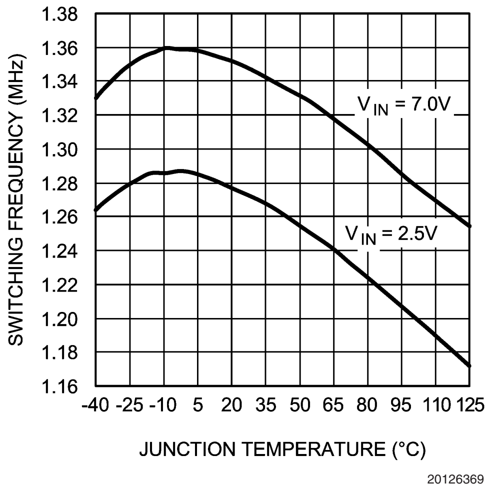
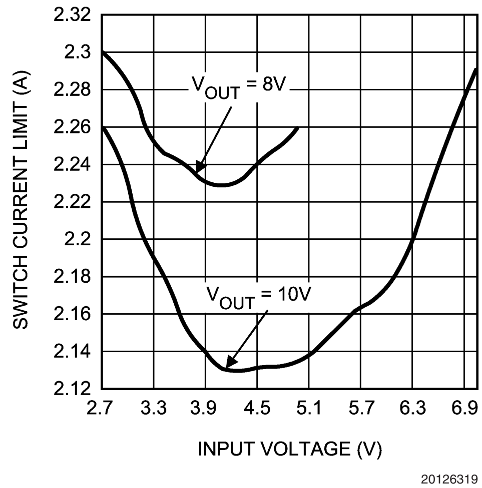
Typical Performance Characteristics (Continued)

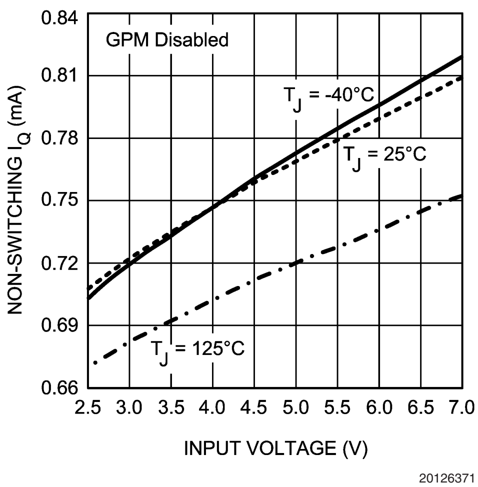
1.28MHz Switching Frequency vs. Temperature



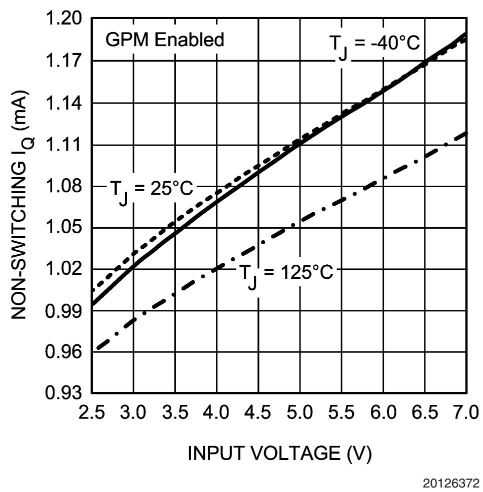
Switch Current Limit vs. Input Voltage



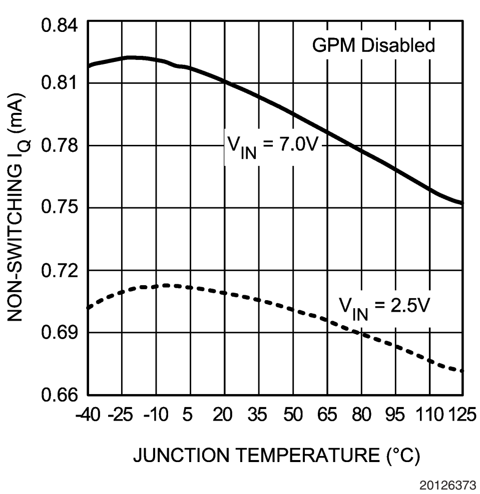
Non-Switching Quiescent Current vs. Input Voltage GPM Disabled



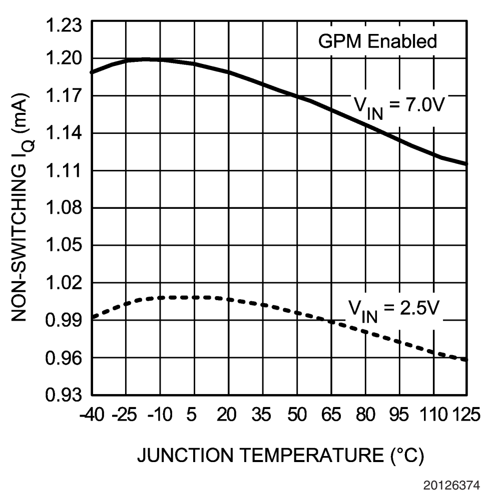
Non-Switching Quiescent Current vs. Input Voltage GPM Enabled



Non-Switching Quiescent Current vs. Temperature GPM Disabled

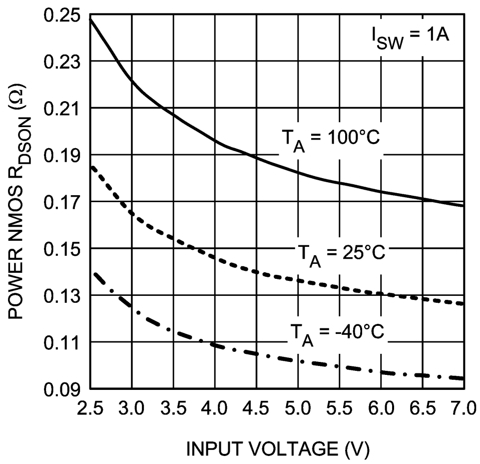


Non-Switching Quiescent Current vs. Temperature GPM Enabled



Typical Performance Characteristics (Continued)

Power NMOS R_{DSON} vs. Input Voltage



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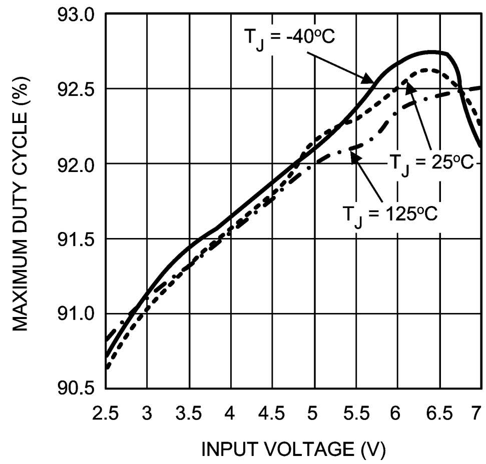
660kHz Max. Duty Cycle vs. Input Voltage



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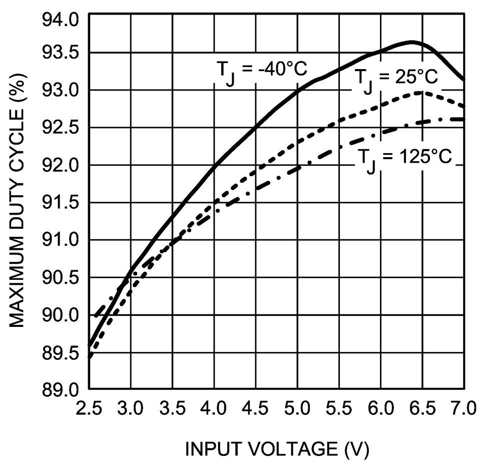
1.28MHz Max. Duty Cycle vs. Input Voltage



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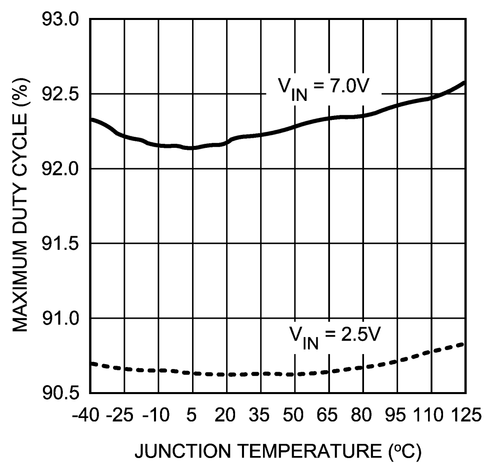
660kHz Max. Duty Cycle vs. Temperature



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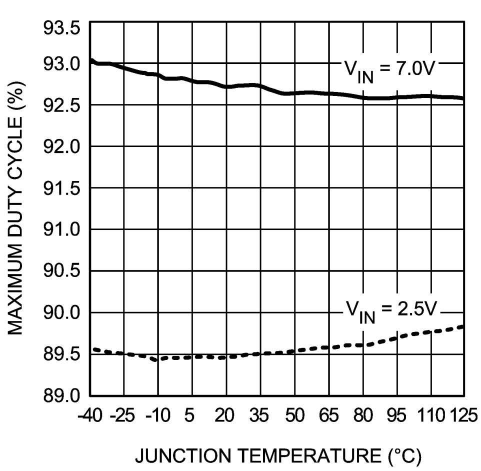
1.28MHz Max. Duty Cycle vs. Temperature



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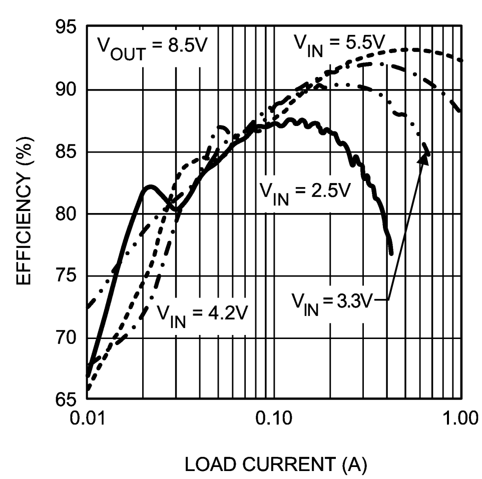
1.28MHz Application Efficiency



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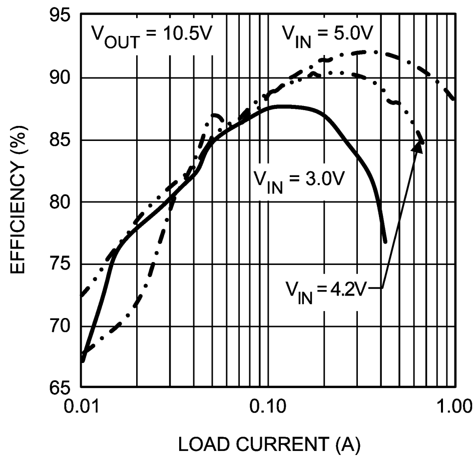
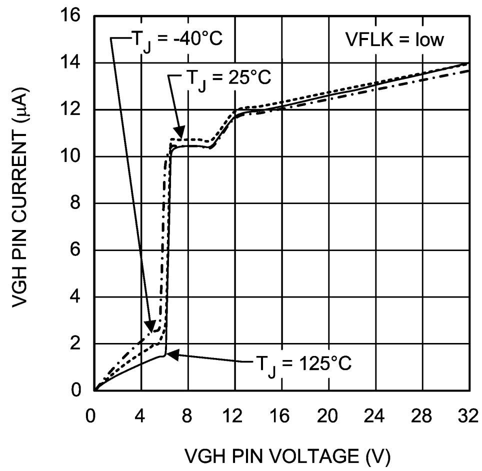
Typical Performance Characteristics (Continued)

1.28MHz Application Efficiency



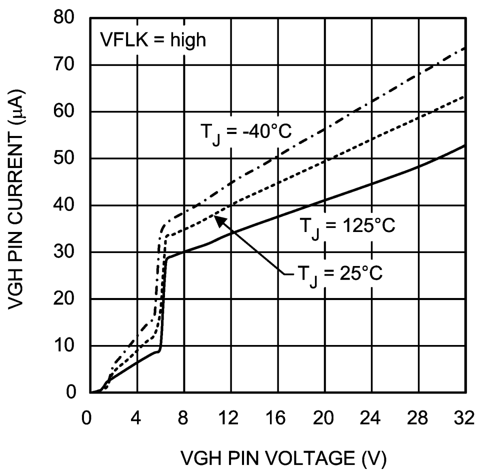
20126326

VGH Pin Bias Current vs. VGH Pin Voltage



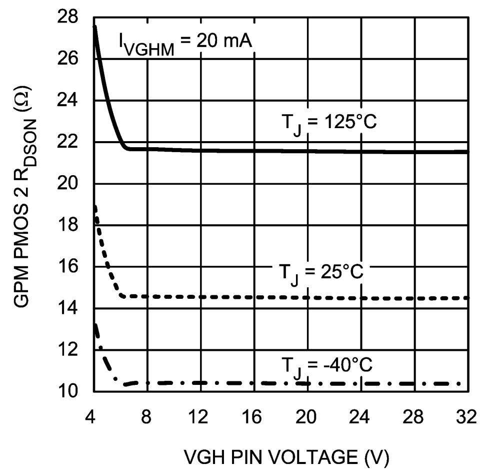
20126377

VGH Pin Bias Current vs. VGH Pin Voltage



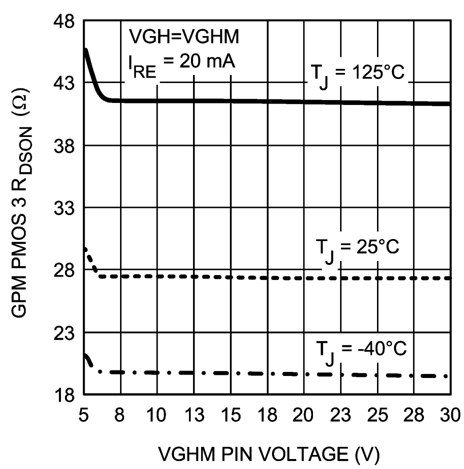
20126378

VGH-VGHM PMOS R_{DSON} vs. VGH Pin Voltage



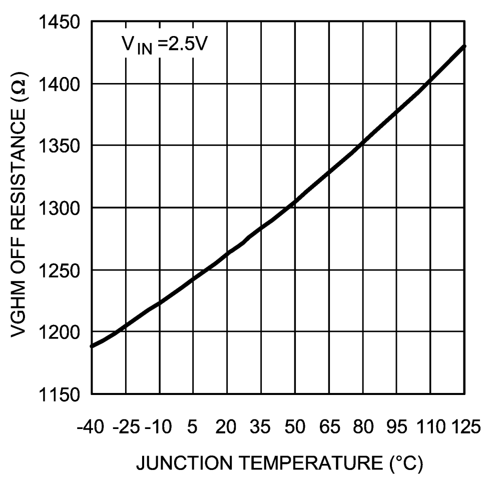
20126379

VGHM-RE PMOS R_{DSON} vs. VGHM Pin Voltage



20126380

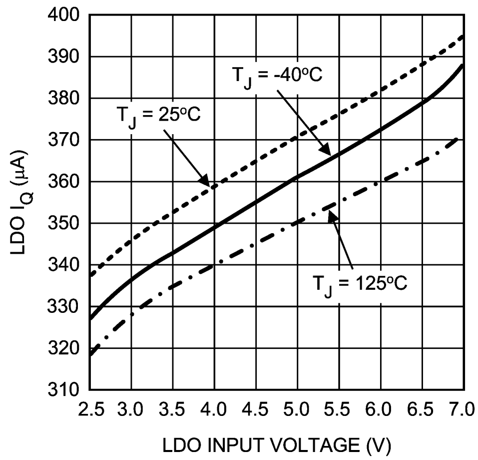
VGHM OFF Resistance vs. Temperature



20126381

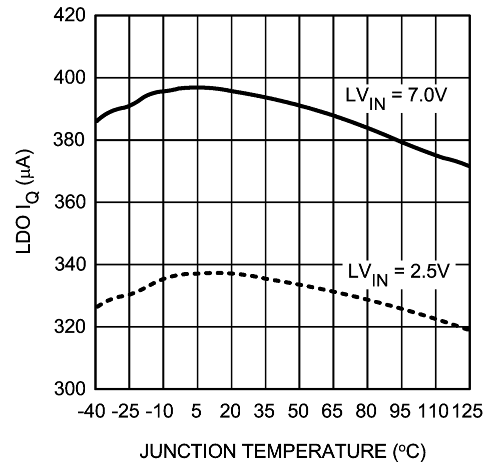
Typical Performance Characteristics (Continued)

LV_{IN} Quiescent Current vs. LV_{IN} Voltage



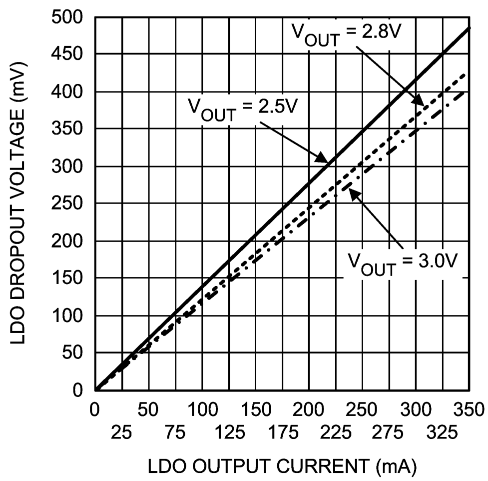
20126392

LV_{IN} Quiescent Current vs. Temperature



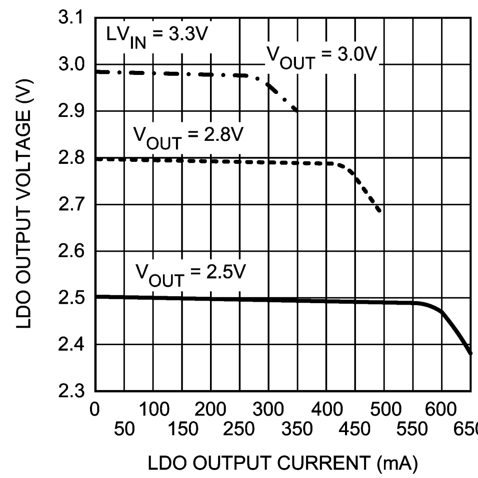
20126393

LDO Dropout Voltage vs. Load Current



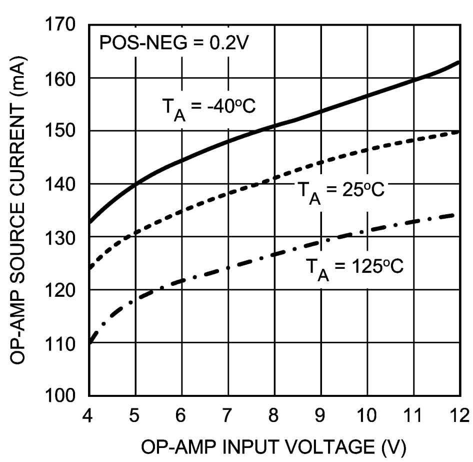
20126394

LDO V_{OUT} vs. Load Current



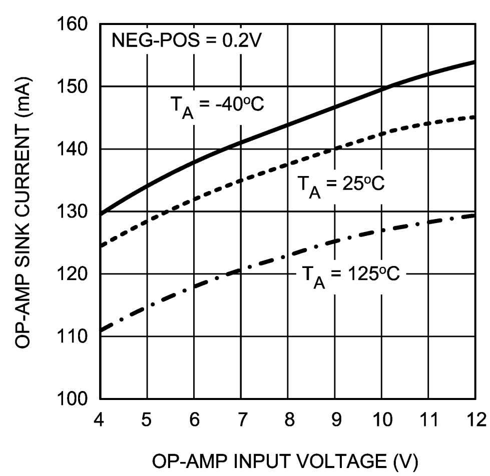
20126395

Op-Amp Source Current vs. AV_{IN}



20126396

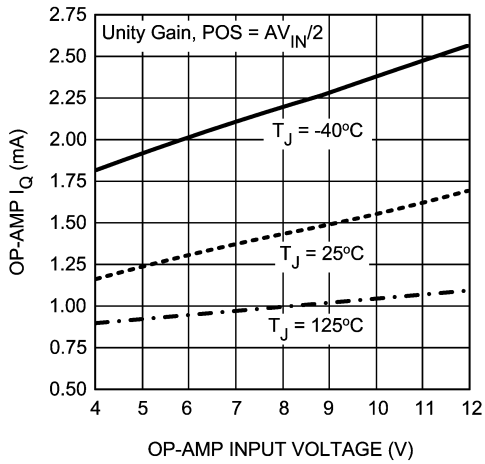
Op-Amp Sink Current vs. AV_{IN}



20126397

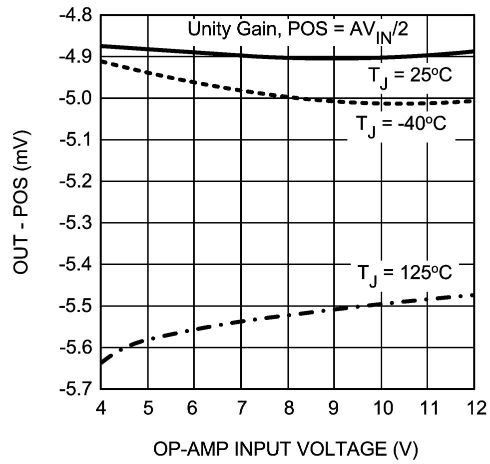
Typical Performance Characteristics (Continued)

Op-Amp Quiescent Current vs. AV_{IN}



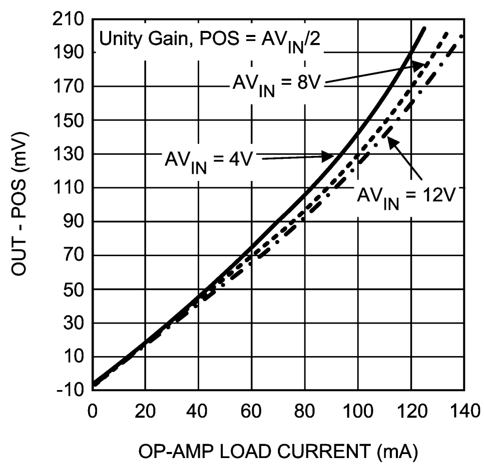
20126316

Op-Amp Offset Voltage Current vs. AV_{IN} (No Load)



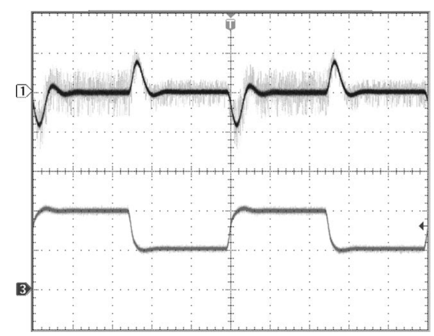
20126317

Op-Amp Offset Voltage Current vs. Load Current



20126318

1.28MHz, 8.5V Application Boost Load Step



20126351

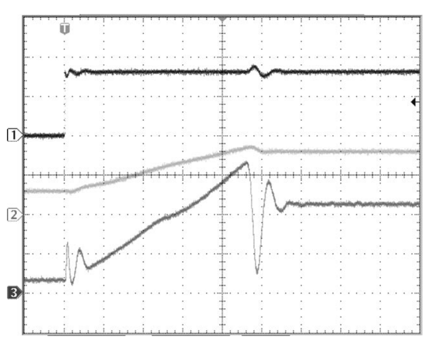
V_{OUT} = 8.5V, V_{IN} = 3.3V, C_{OUT} = 20µF

1) V_{OUT}, 200mV/div, AC

3) I_{LOAD}, 200mA/div, DC

T = 200µs/div

1.28MHz, 8.5V Application Boost Startup Waveform



20126352

V_{OUT} = 8.5V, V_{IN} = 3.3V, C_{OUT} = 20µF, R_{LOAD} = 20Ω, C_{SS} = 10nF

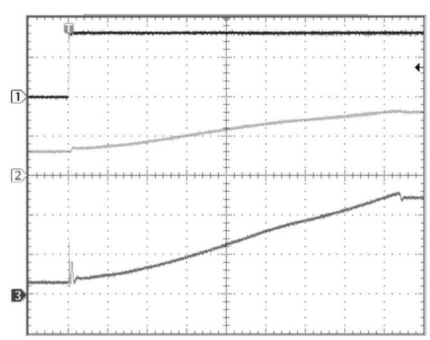
1) V_{SHDN}, 2V/div, DC

2) V_{OUT}, 5V/div, DC

3) I_{IN}, 500mA/div, DC

T = 200µs/div

1.28MHz, 8.5V Application Boost Startup Waveform



20126353

V_{OUT} = 8.5V, V_{IN} = 3.3V, C_{OUT} = 20µF, R_{LOAD} = 20Ω, C_{SS} = 100nF

1) V_{SHDN}, 2V/div, DC

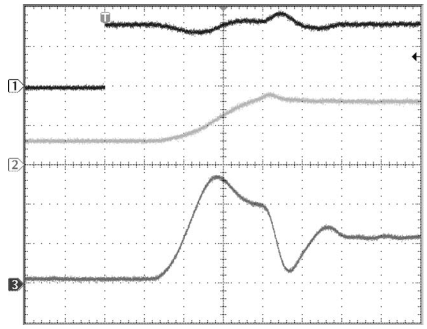
2) V_{OUT}, 5V/div, DC

3) I_{IN}, 500mA/div, DC

T = 1ms/div

Typical Performance Characteristics (Continued)

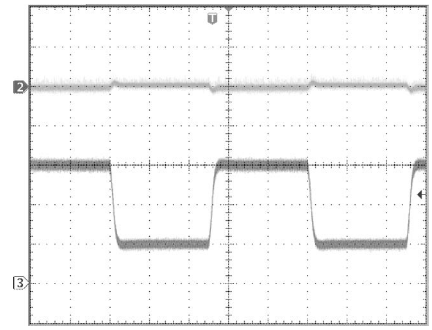
1.28MHz, 8.5V Application Boost Startup Waveform



20126354

V_{OUT} = 8.5V, V_{IN} = 3.3V, C_{OUT} = 20µF, R_{LOAD} = 20Ω, C_{SS} = open
1) V_{SHDN}, 2V/div, DC
2) V_{OUT}, 5V/div, DC
3) I_{IN}, 1A/div, DC
T = 40µs/div

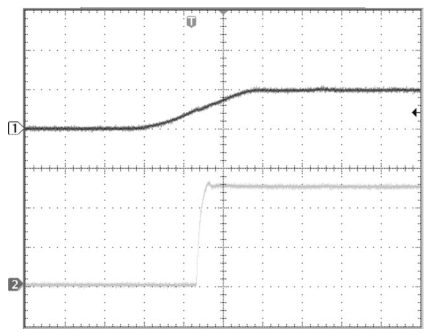
LDO Load Transient Waveform



20126355

LDO_{OUT} = 2.5V, LV_{IN} = 5V, C_{OUT} = 2.2µF
2) LDO_{OUT}, 100mV/div, AC
3) I_{LOAD}, 100mA/div, DC
T = 200µs/div

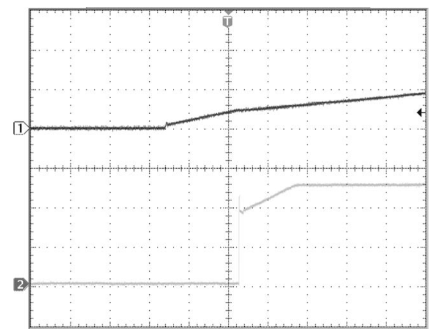
LDO Startup Waveform (LV_{IN} Fast Rising Edge)



20126356

LDO_{OUT} = 2.5V, LV_{IN} = 5V, C_{OUT} = 2.2µF, I_{LOAD} = 300mA
1) LV_{IN}, 5V/div, DC
2) LDO_{OUT}, 1V/div, DC
T = 100µs/div

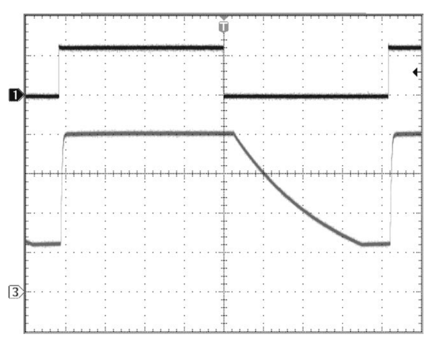
LDO Startup Waveform (LV_{IN} Slow Rising Edge)



20126308

LDO_{OUT} = 2.5V, LV_{IN} = 5V, C_{OUT} = 2.2µF, I_{LOAD} = 300mA
1) LV_{IN}, 5V/div, DC
2) LDO_{OUT}, 1V/div, DC
T = 4ms/div

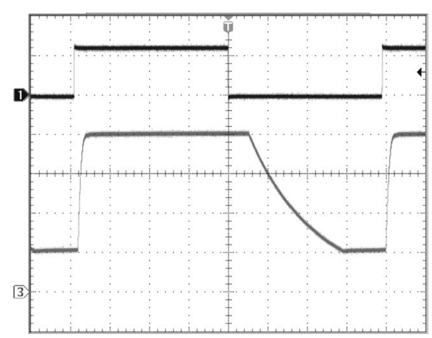
GPM Transient Waveforms



20126327

VGH = 20V, VDPM = 3.3V, C_{VGHM} = 4.7nF, R_E = 2.4kΩ, C_E = 33pF, R1 = 13kΩ, R2 = 1.2kΩ, VFLK at 50% duty cycle and 30kHz
1) VFLK, 2V/div, DC
3) VGHM, 5V/div, DC
T = 4µs/div

GPM Transient Waveforms

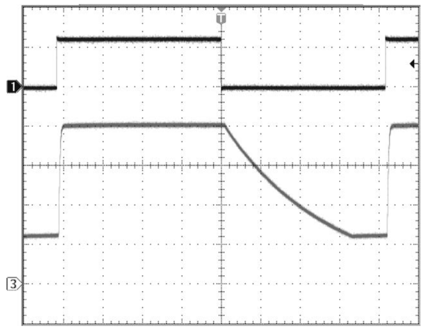


20126328

VGH = 20V, VDPM = 3.3V, C_{VGHM} = 4.7nF, R_E = 750Ω, C_E = 33pF, R1 = 13kΩ, R2 = 1.2kΩ, VFLK at 50% duty cycle and 64kHz
1) VFLK, 2V/div, DC
3) VGHM, 5V/div, DC
T = 2µs/div

Typical Performance Characteristics (Continued)

GPM Transient Waveforms



20126398

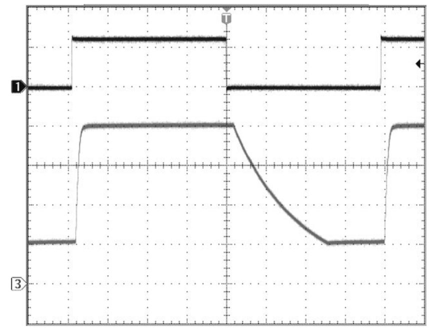
VGH = 20V, VDPM = 3.3V, C_{VGHM} = 4.7nF, R_E = 2.4kΩ, C_E = open, R1 = 13kΩ, R2 = 1.2kΩ, VFLK at 50% duty cycle and 30kHz

1) VFLK, 2V/div, DC

3) VGHM, 5V/div, DC

T = 4µs/div

GPM Transient Waveforms



20126310

VGH = 20V, VDPM = 3.3V, C_{VGHM} = 4.7nF, R_E = 750Ω, C_E = open, R1 = 13kΩ, R2 = 1.2kΩ, VFLK at 50% duty cycle and 64kHz

1) VFLK, 2V/div, DC

3) VGHM, 5V/div, DC

T = 2µs/div

Operation

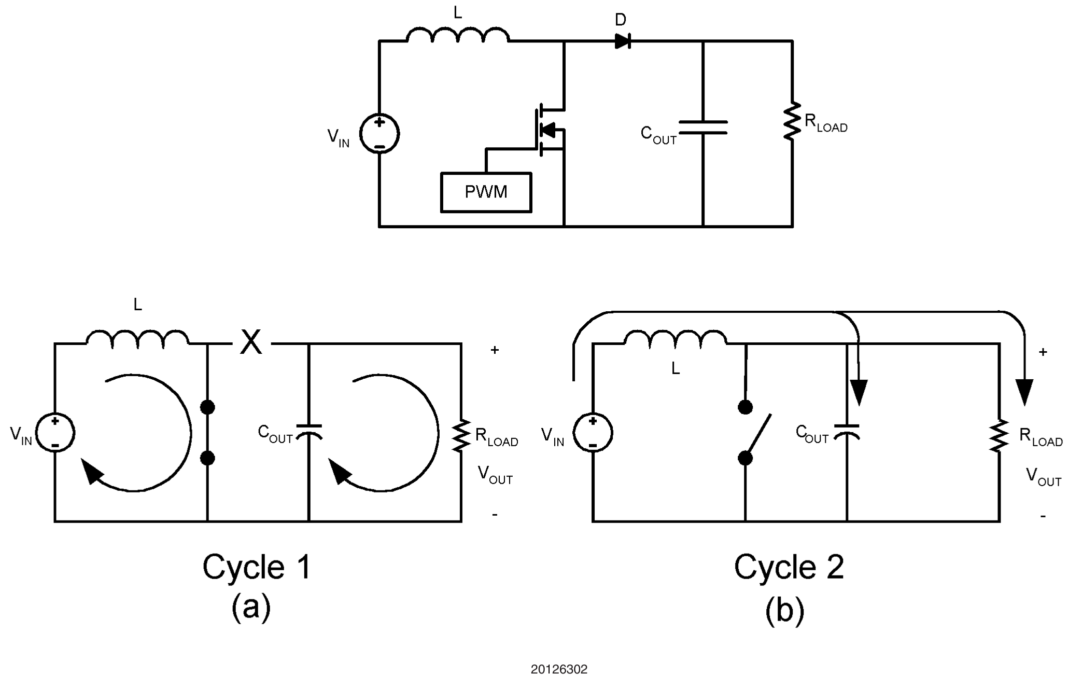


FIGURE 1. Simplified Boost Converter Diagram
(a) First Cycle of Operation (b) Second Cycle Of Operation

CONTINUOUS CONDUCTION MODE

The LM3311 contains a current-mode, PWM boost regulator. A boost regulator steps the input voltage up to a higher output voltage. In continuous conduction mode (when the inductor current never reaches zero at steady state), the boost regulator operates in two cycles.

In the first cycle of operation, shown in *Figure 1* (a), the transistor is closed and the diode is reverse biased. Energy is collected in the inductor and the load current is supplied by C_{OUT}.

The second cycle is shown in *Figure 1* (b). During this cycle, the transistor is open and the diode is forward biased. The energy stored in the inductor is transferred to the load and output capacitor.

The ratio of these two cycles determines the output voltage. The output voltage is defined approximately as:

$$V_{OUT} = \frac{V_{IN}}{1\text{-}D},\ D' = (1\text{-}D) = \frac{V_{IN}}{V_{OUT}}$$

where D is the duty cycle of the switch, D and D' will be required for design calculations.

SETTING THE OUTPUT VOLTAGE (BOOST CONVERTER AND LDO)

The output voltage is set using the feedback pin and a resistor divider connected to the output as shown in the typical operating circuit. The feedback pin voltage is 1.263V for both the boost regulator and the LDO, so the ratio of the feedback resistors sets the output voltage according to the following equations:

$$R_{FB1} = R_{FB2} \times \frac{V_{OUT} - 1.263}{1.263}\ \Omega\ \text{(Boost)}$$

$$R_{ADJ1} = R_{ADJ2} \times \frac{\text{LDO out} - 1.263}{1.263}\ \Omega\ \text{(LDO)}$$

SOFT-START CAPACITOR

The LM3311 has a soft-start pin that can be used to limit the inductor inrush current on start-up. The external SS pin is used to tailor the soft-start for a specific application (see the *Linear Regulator (LDO)* section for the minimum value of C_{SS}). When used, a current source charges the external soft-start capacitor C_{SS} until it reaches its typical clamp voltage, V_{SS}. The soft-start time can be estimated as:

$$T_{SS} = C_{SS} * V_{SS} / I_{SS}$$

THERMAL SHUTDOWN

The LM3311 includes thermal shutdown. If the die temperature reaches 145˚C the device will shut down until it cools to a safe temperature at which point the device will resume operation. If the adverse condition that is heating the device is not removed (ambient temperature too high, short circuit conditions, etc...) the device will continue to cycle on and off to keep the die temperature below 145˚C. The thermal shutdown has approximately 20˚C of hysteresis. When in thermal shutdown the boost regulator, LDO, Op-Amp, and GPM blocks will all be disabled.

Operation (Continued)

INPUT UNDER-VOLTAGE PROTECTION

The LM3311 includes input under-voltage protection (UVP). The purpose of the UVP is to protect the device both during start-up and during normal operation from trying to operate with insufficient input voltage. During start-up using a ramping input voltage the UVP circuitry ensures that the device does not begin switching until the input voltage reaches the UVP On threshold. If the input voltage is present and the shutdown pin is pulled high the UVP circuitry will prevent the device from switching if the input voltage present is lower than the UVP On threshold. During normal operation the UVP circuitry will disable the device if the input voltage falls below the UVP Off threshold for any reason. In this case the device will not turn back on until the UVP On threshold voltage is exceeded.

LINEAR REGULATOR (LDO)

The LM3311 includes a Low Dropout Linear Regulator. The LDO is designed to operate with ceramic input and output capacitors with values as low as 2.2µF. The efficiency of the LDO is approximately the output voltage divided by the input voltage. When using higher input voltages special care should be taken to not dissipate too much power and cause excessive heating of the die. The power dissipated in the LDO section is approximately:

$$P_{D(LDO)} = (V_{IN} - V_{OUT})*I_{OUT}$$

The LDO has an output undervoltage lockout feature. This feature is to ensure the LDO will shut itself down in the event of an output overload or short condition. When the output is overloaded the output voltage will fall causing the ADJ voltage to fall. When the ADJ voltage falls to $V_{ADJ(LOW)}$ the LDO will shut off. In this event the $\overline{SHDN}$ pin or the input UVP must be cycled to turn the LDO back on.

The LDO output undervoltage lockout is controlled by the SS voltage. The LDO startup time must be less than the following:

$$T_S = C_{SS}*0.5V/I_{SS}$$

When SS is less than 0.5V the output undervoltage lockout is disabled and allows the LDO to start up. When SS is greater than 0.5V the undervoltage lockout is active. If the LDO feedback voltage is not greater than $V_{ADJ(LOW)}$ when SS reaches 0.5V the LDO may enter an undervoltage lockout condition. In most cases C_{SS} = 10nF or greater is sufficient. If a supply other than that used to power V_{IN} is used to power LV_{IN} care must be taken to apply the input voltage to LV_{IN} prior to applying voltage to V_{IN}.

OPERATIONAL AMPLIFIER

Compensation:

The architecture used for the amplifier in the LM3311 requires external compensation on the output. Depending on the equivalent resistive and capacitive distributed load of the TFT-LCD panel, external components at the amplifier outputs may or may not be necessary. If the capacitance presented by the load is equal to or greater than an equivalent distibutive load of 50Ω in series with 4.7nF no external components are needed as the TFT-LCD panel will act as compensation itself. Distributed resistive and capacitive loads enhance stability and increase performance of the amplifiers. If the capacitance and resistance presented by the load is less than 50Ω in series with 4.7nF, external components will be required as the load itself will not ensure stability. No external compensation in this case will lead to oscillation of the amplifier and an increase in power consumption. A good choice for compensation in this case is to add a 50Ω in series with a 4.7nF capacitor from the output of the amplifier to ground. This allows for driving zero to infinite capacitance loads with no oscillations, minimal overshoot, and a higher slew rate than using a single large capacitor. The high phase margin created by the external compensation will guarantee stability and good performance for all conditions.

Layout and Filtering considerations:

When the power supply for the amplifier (AV_{IN}) is connected to the output of the switching regulator, the output ripple of the regulator will produce ripple at the output of the amplifiers. This can be minimized by directly bypassing the AV_{IN} pin to ground with a low ESR ceramic capacitor. For best noise reduction a resistor on the order of 5Ω to 20Ω from the supply being used to the AV_{IN} pin will create and RC filter and give you a cleaner supply to the amplifier. The bypass capacitor should be placed as close to the AV_{IN} pin as possible and connected directly to the AGND plane.

For best noise immunity all bias and feedback resistors should be in the low kΩ range due to the high input impedance of the amplifier. It is good practice to use a small capacitance at the high impedance input terminals as well to reduce noise susceptibility. All resistors and capacitors should be placed as close to the input pins as possible.

Special care should also be taken in routing of the PCB traces. All traces should be as short and direct as possible. The output pin trace must never be routed near any trace going to the positive input. If this happens cross talk from the output trace to the positive input trace will cause the circuit to oscillate.

The op-amp is not a three terminal device it has 5 terminals: positive voltage power pin, AGND, positive input, negative input, and the output. The op-amp "routes" current from the power pin and AGND to the output pin. So in effect an opamp has not two inputs but four, all of which must be kept noise free relative to the external circuits which are being driven by the op-amp. The current from the power pins goes through the output pin and into the load and feedback loop. The current exiting the load and feedback loops then must have a return path back to the op-amp power supply pins. Ideally this return path must follow the same path as the output pin trace to the load. Any deviation that makes the loop area larger between the output current path and the return current path adds to the probability of noise pick up.

GATE PULSE MODULATION

The Gate Pulse Modulation (GPM) block is designed to provide a modulated voltage to the gate driver circuitry of a TFT LCD display. Operation is best understood by referring to the GPM block diagram in the *Block Diagrams* section, the drawing in *Figure 2* and the transient waveforms in *Figure 3* and *Figure 4*.

There are two control signals in the GPM block, VDPM and VFLK. VDPM is the enable pin for the GPM block. If VDPM is high, the GPM block is active and will respond to the VFLK drive signal from the timing controller. However, if VDPM is low, the GPM block will be disabled and both PMOS switches P2 and P3 will be turned off. The VGHM node will be discharged through a 1kΩ resistor and the NMOS switch N2.

When VDPM is high, typical waveforms for the GPM block can be seen in *Figure 2*. The pin VGH is typically driven by a 2x or 3x charge pump. In most cases, the 2x or 3x charge

Operation (Continued)

pump is a discrete solution driven from the SW pin and the output of the boost switching regulator. When VFLK is high, the PMOS switch P2 is turned on and the PMOS switch P3 is turned off. With P2 on, the VGHM pin is pulled to the same voltage applied to the VGH pin. This provides a high gate drive voltage, $VGHM_{MAX}$, and can source current to the gate drive circuitry. When VFLK is high, NMOS switch N3 is on which discharges the capacitor CE.

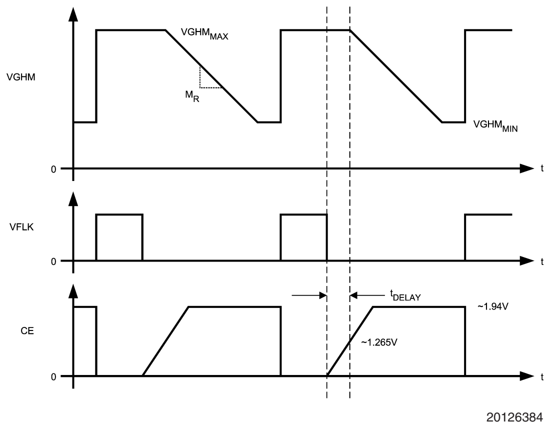


FIGURE 2.

When VFLK is low, the NMOS switch N3 is turned off which allows current to charge the C_E capacitor. This creates a delay, t_{DELAY}, given by the following equations:

$$t_{DELAY} \approxeq 1.265V(C_E + 15pF)/I_{CE}$$

When the voltage on CE reaches about 1.265V and the VFLK signal is low, the PMOS switch P2 will turn off and the PMOS switch P3 will turn on connecting resistor R3 to the VGHM pin through P3. This will discharge the voltage at VGHM at some rate determined by R3 creating a slope, M_R, as shown in *Figure 2*. The VGHM pin is no longer a current source, it is now sinking current from the gate drive circuitry.

As VGHM is discharged through R3, the comparator connected to the pin V_{DD} monitors the VGHM voltage. PMOS switch P3 will turn off when the following is true:

$$VGHM_{MIN} \approxeq 10V_X R2/(R1 + R2)$$

where V_X is some voltage connected to the resistor divider on pin V_{DD}. V_X is typically connected to the output of the boost switching regulator. When PMOS switch P3 turns off, VGHM will be high impedance until the VFLK pin is high again.

Figure 3 and *Figure 4* give typical transient waveforms for the GPM block. Waveform (1) is the VGHM pin, (2) is the VFLK and (3) is the VDPM. The output of the boost switching regulator is operating at 8.5V and there is a 3x discrete charge pump (~23.5V) supplying the VGH pin. In *Figure 3* and *Figure 4*, the VGHM pin is driving a purely capacitive load, 4.7nF. The value of resistor R1 is 15kohm, R2 is 1.1kΩ and R3 is 750Ω. In both transient plots, there is no C_E delay capacitor.

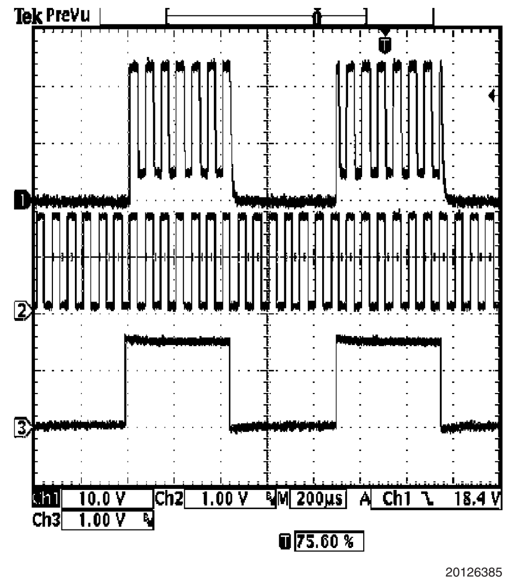


FIGURE 3.

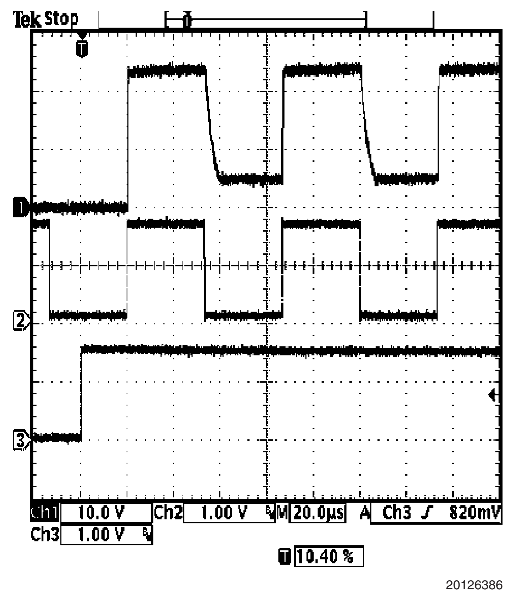


FIGURE 4.

In the GPM block diagram, a signal called “Reset” is shown. This signal is generated from the V_{IN} under-voltage lockout, thermal shutdown, or the $\overline{SHDN}$ pin. If the V_{IN} supply voltage drops below 2.3V, typically, then the GPM block will be disabled and the VGHM pin will discharge through NMOS switch N2 and the 1kΩ resistor. This applies also if the junction temperature of the device exceeds 145˚C or if the $\overline{SHDN}$ signal is low. As shown in the block diagram, both VDPM and VFLK have internal 350kΩ pull down resistors. This puts both VDPM and VFLK in normally “off” states. Typical VDPM and VFLK pin currents can be found in the *Typical Performance Characteristics* section.

Operation (Continued)

INTRODUCTION TO COMPENSATION (BOOST CONVERTER)

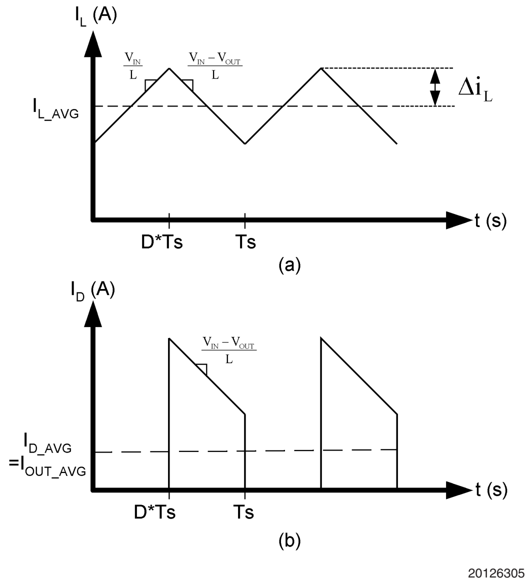


FIGURE 5. (a) Inductor current. (b) Diode current.

The LM3311 is a current mode PWM boost converter. The signal flow of this control scheme has two feedback loops, one that senses switch current and one that senses output voltage.

To keep a current programmed control converter stable above duty cycles of 50%, the inductor must meet certain criteria. The inductor, along with input and output voltage, will determine the slope of the current through the inductor (see *Figure 5* (a)). If the slope of the inductor current is too great, the circuit will be unstable above duty cycles of 50%. A 10µH inductor is recommended for most 660 kHz applications, while a 4.7µH inductor may be used for most 1.28 MHz applications. If the duty cycle is approaching the maximum of 85%, it may be necessary to increase the inductance by as much as 2X. See *Inductor and Diode Selection* for more detailed inductor sizing.

The LM3311 provides a compensation pin (V_C) to customize the voltage loop feedback. It is recommended that a series combination of R_C and C_C be used for the compensation network, as shown in the typical application circuit. For any given application, there exists a unique combination of R_C and C_C that will optimize the performance of the LM3311 circuit in terms of its transient response. The series combination of R_C and C_C introduces a pole-zero pair according to the following equations:

$$f_{ZC} = \frac{1}{2\pi R_C C_C} \text{ Hz}$$

$$f_{PC} = \frac{1}{2\pi (R_C + R_O) C_C} \text{ Hz}$$

where R_O is the output impedance of the error amplifier, approximately 900kΩ. For most applications, performance can be optimized by choosing values within the range 5kΩ ≤ R_C ≤ 100kΩ (R_C can be higher values if C_{C2} is used, see *High Output Capacitor ESR Compensation*) and 68pF ≤ C_C ≤ 4.7nF. Refer to the *Applications Information* section for recommended values for specific circuits and conditions. Refer to the *Compensation* section for other design requirement.

COMPENSATION

This section will present a general design procedure to help insure a stable and operational circuit. The designs in this datasheet are optimized for particular requirements. If different conversions are required, some of the components may need to be changed to ensure stability. Below is a set of general guidelines in designing a stable circuit for continuous conduction operation, in most all cases this will provide for stability during discontinuous operation as well. The power components and their effects will be determined first, then the compensation components will be chosen to produce stability.

INDUCTOR AND DIODE SELECTION

Although the inductor sizes mentioned earlier are fine for most applications, a more exact value can be calculated. To ensure stability at duty cycles above 50%, the inductor must have some minimum value determined by the minimum input voltage and the maximum output voltage. This equation is:

$$L > \frac{V_{IN} R_{DSON}}{0.144 \text{ fs}} \left[\frac{D}{D'} - 1 \right] \text{ (in H)}$$

where fs is the switching frequency, D is the duty cycle, and R_{DSON} is the ON resistance of the internal power switch. This equation is only good for duty cycles greater than 50% (D>0.5), for duty cycles less than 50% the recommended values may be used. The value given by this equation is the inductance necessary to supress sub-harmonic oscillations. In some cases the value given by this equation may be too small for a given application. In this case the average inductor current and the inductor current ripple must be considered.

The corresponding inductor current ripple, average inductor current, and peak inductor current as shown in *Figure 5* (a) is given by:

$$\Delta i_L = \frac{V_{IN} D}{2 L f s} \text{ (in Amps)}$$

$$i_{L(AVE)} \approx \frac{I_{OUT}}{\eta D'}$$

$$i_{L(PEAK)} \approx i_{L(AVE)} + \Delta i_L$$

Continuous conduction mode occurs when Δi_L is less than the average inductor current and discontinuous conduction mode occurs when Δi_L is greater than the average inductor current. Care must be taken to make sure that the switch will not reach its current limit during normal operation. The inductor must also be sized accordingly. It should have a saturation current rating higher than the peak inductor current expected. The output voltage ripple is also affected by the total ripple current.

Operation (Continued)

The output diode for a boost regulator must be chosen correctly depending on the output voltage and the output current. The typical current waveform for the diode in continuous conduction mode is shown in *Figure 5* (b). The diode must be rated for a reverse voltage equal to or greater than the output voltage used. The average current rating must be greater than the maximum load current expected, and the peak current rating must be greater than the peak inductor current. During short circuit testing, or if short circuit conditions are possible in the application, the diode current rating must exceed the switch current limit. Using Schottky diodes with lower forward voltage drop will decrease power dissipation and increase efficiency.

DC GAIN AND OPEN-LOOP GAIN

Since the control stage of the converter forms a complete feedback loop with the power components, it forms a closed-loop system that must be stabilized to avoid positive feedback and instability. A value for open-loop DC gain will be required, from which you can calculate, or place, poles and zeros to determine the crossover frequency and the phase margin. A high phase margin (greater than 45˚) is desired for the best stability and transient response. For the purpose of stabilizing the LM3311, choosing a crossover point well below where the right half plane zero is located will ensure sufficient phase margin.

To ensure a bandwidth of ½ or less of the frequency of the RHP zero, calculate the open-loop DC gain, A_{DC}. After this value is known, you can calculate the crossover visually by placing a −20dB/decade slope at each pole, and a +20dB/decade slope for each zero. The point at which the gain plot crosses unity gain, or 0dB, is the crossover frequency. If the crossover frequency is less than ½ the RHP zero, the phase margin should be high enough for stability. The phase margin can also be improved by adding C_{C2} as discussed later in this section. The equation for A_{DC} is given below with additional equations required for the calculation:

$$A_{DC(DB)} = 20\log_{10}\left\langle\left(\frac{R_{FB2}}{R_{FB1}+R_{FB2}}\right)\frac{g_m R_O D'}{R_{DSON}}\{[(\omega cLeff)//\ R_L]//R_L\}\right\rangle \text{ (in dB)}$$

$$\omega c \cong \frac{2fs}{nD'} \text{ (in rad/s)}$$

$$Leff = \frac{L}{(D')^2}$$

$$n = 1 + \frac{2mc}{m1} \text{ (no unit)}$$

$$mc \cong 0.072fs \text{ (in V/s)}$$

$$m1 \cong \frac{V_{IN}R_{DSON}}{L} \text{ (in V/s)}$$

where R_L is the minimum load resistance, V_{IN} is the minimum input voltage, g_m is the error amplifier transconductance found in the *Electrical Characteristics* table, and R_{DSON} is the value chosen from the graph "NMOS R_{DSON} vs. Input Voltage" in the *Typical Performance Characteristics* section.

INPUT AND OUTPUT CAPACITOR SELECTION

The switching action of a boost regulator causes a triangular voltage waveform at the input. A capacitor is required to reduce the input ripple and noise for proper operation of the regulator. The size used is dependant on the application and board layout. If the regulator will be loaded uniformly, with very little load changes, and at lower current outputs, the input capacitor size can often be reduced. The size can also be reduced if the input of the regulator is very close to the source output. The size will generally need to be larger for applications where the regulator is supplying nearly the maximum rated output or if large load steps are expected. A minimum value of 10µF should be used for the less stressful condtions while a 22µF to 47µF capacitor may be required for higher power and dynamic loads. Larger values and/or lower ESR may be needed if the application requires very low ripple on the input source voltage.

The choice of output capacitors is also somewhat arbitrary and depends on the design requirements for output voltage ripple. It is recommended that low ESR (Equivalent Series Resistance, denoted R_{ESR}) capacitors be used such as ceramic, polymer electrolytic, or low ESR tantalum. Higher ESR capacitors may be used but will require more compensation which will be explained later on in the section. The ESR is also important because it determines the peak to peak output voltage ripple according to the approximate equation:

$$\Delta V_{OUT} \cong 2\Delta i_L R_{ESR} \text{ (in Volts)}$$

A minimum value of 10µF is recommended and may be increased to a larger value. After choosing the output capacitor you can determine a pole-zero pair introduced into the control loop by the following equations:

$$f_{P1} = \frac{1}{2\pi(R_{ESR}+R_L)C_{OUT}} \text{ (in Hz)}$$

$$f_{Z1} = \frac{1}{2\pi R_{ESR}C_{OUT}} \text{ (in Hz)}$$

Where R_L is the minimum load resistance corresponding to the maximum load current. The zero created by the ESR of the output capacitor is generally very high frequency if the ESR is small. If low ESR capacitors are used it can be neglected. If higher ESR capacitors are used see the *High Output Capacitor ESR Compensation* section. Some suitable capacitor vendors include Vishay, Taiyo-Yuden, and TDK.

RIGHT HALF PLANE ZERO

A current mode control boost regulator has an inherent right half plane zero (RHP zero). This zero has the effect of a zero in the gain plot, causing an imposed +20dB/decade on the rolloff, but has the effect of a pole in the phase, subtracting another 90˚ in the phase plot. This can cause undesirable effects if the control loop is influenced by this zero. To ensure the RHP zero does not cause instability issues, the control loop should be designed to have a bandwidth of less than ½ the frequency of the RHP zero. This zero occurs at a frequency of:

$$RHPzero = \frac{V_{OUT}(D')^2}{2\pi I_{LOAD}L} \text{ (in Hz)}$$

where I_{LOAD} is the maximum load current.

Operation (Continued)

SELECTING THE COMPENSATION COMPONENTS

The first step in selecting the compensation components R_C and C_C is to set a dominant low frequency pole in the control loop. Simply choose values for R_C and C_C within the ranges given in the *Introduction to Compensation* section to set this pole in the area of 10Hz to 500Hz. The frequency of the pole created is determined by the equation:

$$f_{PC} = \frac{1}{2\pi(R_C + R_O)C_C} \text{ (in Hz)}$$

where R_O is the output impedance of the error amplifier, approximately 900kΩ. Since R_C is generally much less than R_O, it does not have much effect on the above equation and can be neglected until a value is chosen to set the zero f_{ZC}. f_{ZC} is created to cancel out the pole created by the output capacitor, f_{P1}. The output capacitor pole will shift with different load currents as shown by the equation, so setting the zero is not exact. Determine the range of f_{P1} over the expected loads and then set the zero f_{ZC} to a point approximately in the middle. The frequency of this zero is determined by:

$$f_{ZC} = \frac{1}{2\pi C_C R_C} \text{ (in Hz)}$$

Now R_C can be chosen with the selected value for C_C. Check to make sure that the pole f_{PC} is still in the 10Hz to 500Hz range, change each value slightly if needed to ensure both component values are in the recommended range.

HIGH OUTPUT CAPACITOR ESR COMPENSATION

When using an output capacitor with a high ESR value, or just to improve the overall phase margin of the control loop, another pole may be introduced to cancel the zero created by the ESR. This is accomplished by adding another capacitor, C_{C2}, directly from the compensation pin V_C to ground, in parallel with the series combination of R_C and C_C. The pole should be placed at the same frequency as f_{Z1}, the ESR zero. The equation for this pole follows:

$$f_{PC2} = \frac{1}{2\pi C_{C2}(R_C // R_O)} \text{ (in Hz)}$$

To ensure this equation is valid, and that C_{C2} can be used without negatively impacting the effects of R_C and C_C, f_{PC2} must be greater than $10f_{ZC}$.

CHECKING THE DESIGN

With all the poles and zeros calculated the crossover frequency can be checked as described in the section *DC Gain and Open-loop Gain*. The compensation values can be changed a little more to optimize performance if desired. This is best done in the lab on a bench, checking the load step response with different values until the ringing and overshoot on the output voltage at the edge of the load steps is minimal. This should produce a stable, high performance circuit. For improved transient response, higher values of R_C should be chosen. This will improve the overall bandwidth which makes the regulator respond more quickly to transients. If more detail is required, or the most optimum performance is desired, refer to a more in depth discussion of compensating current mode DC/DC switching regulators.

POWER DISSIPATION

The output power of the LM3311 is limited by its maximum power dissipation. The maximum power dissipation is determined by the formula

$$P_D = (T_{jmax} - T_A)/\theta_{JA}$$

where T_{jmax} is the maximum specified junction temperature (125˚C), T_A is the ambient temperature, and θ_{JA} is the thermal resistance of the package.

LAYOUT CONSIDERATIONS

The input bypass capacitor C_{IN}, as shown in the typical operating circuit, must be placed close to the IC. This will reduce copper trace resistance which effects input voltage ripple of the IC. For additional input voltage filtering, a 100nF bypass capacitor can be placed in parallel with C_{IN}, close to the V_{IN} pin, to shunt any high frequency noise to ground. The output capacitor, C_{OUT}, should also be placed close to the IC. Any copper trace connections for the C_{OUT} capacitor can increase the series resistance, which directly effects output voltage ripple. The feedback network, resistors R_{FB1} and R_{FB2}, should be kept close to the FB pin, and away from the inductor, to minimize copper trace connections that can inject noise into the system. R_E and C_E should also be close to the RE and CE pins to minimize noise in the GPM circuitry. Trace connections made to the inductor and schottky diode should be minimized to reduce power dissipation and increase overall efficiency. For more detail on switching power supply layout considerations see Application Note AN-1149: *Layout Guidelines for Switching Power Supplies*.

The input capacitor, output capacitor, and feedback resistors for the LDO should be placed as close to the device as possible to minimize noise and increase stability. Keep the feedback traces short and connect R_{ADJ2} directly to AGND close to the device.

For Op-Amp layout please refer to the *Operational Amplifier* section.

Figure 6, *Figure 7*, and *Figure 8* in the Application Information section following show the schematic and an example of a good layout as used in the LM3310/11 evaluation board.

Application Information

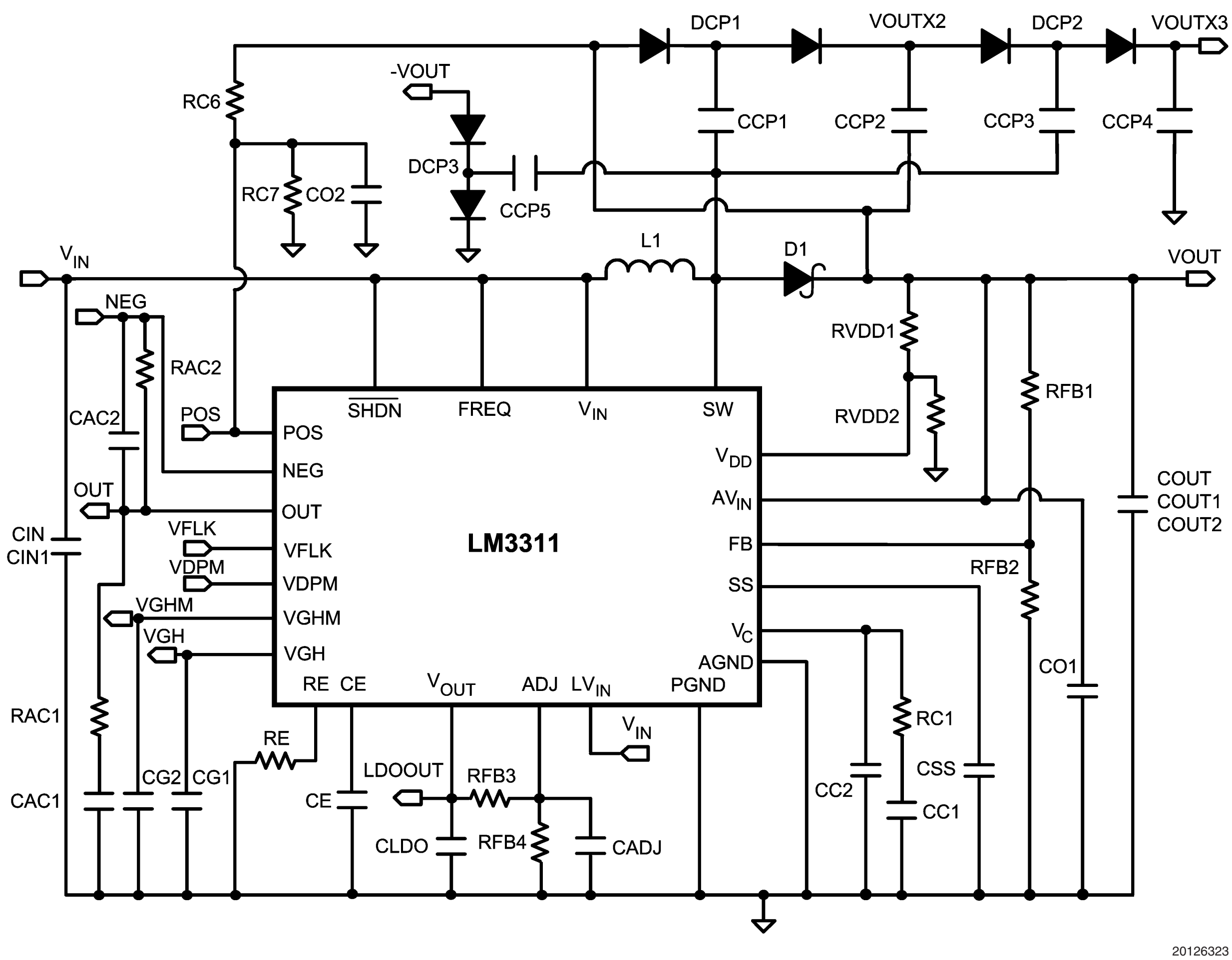


FIGURE 6. Evaluation Board Schematic

Application Information (Continued)

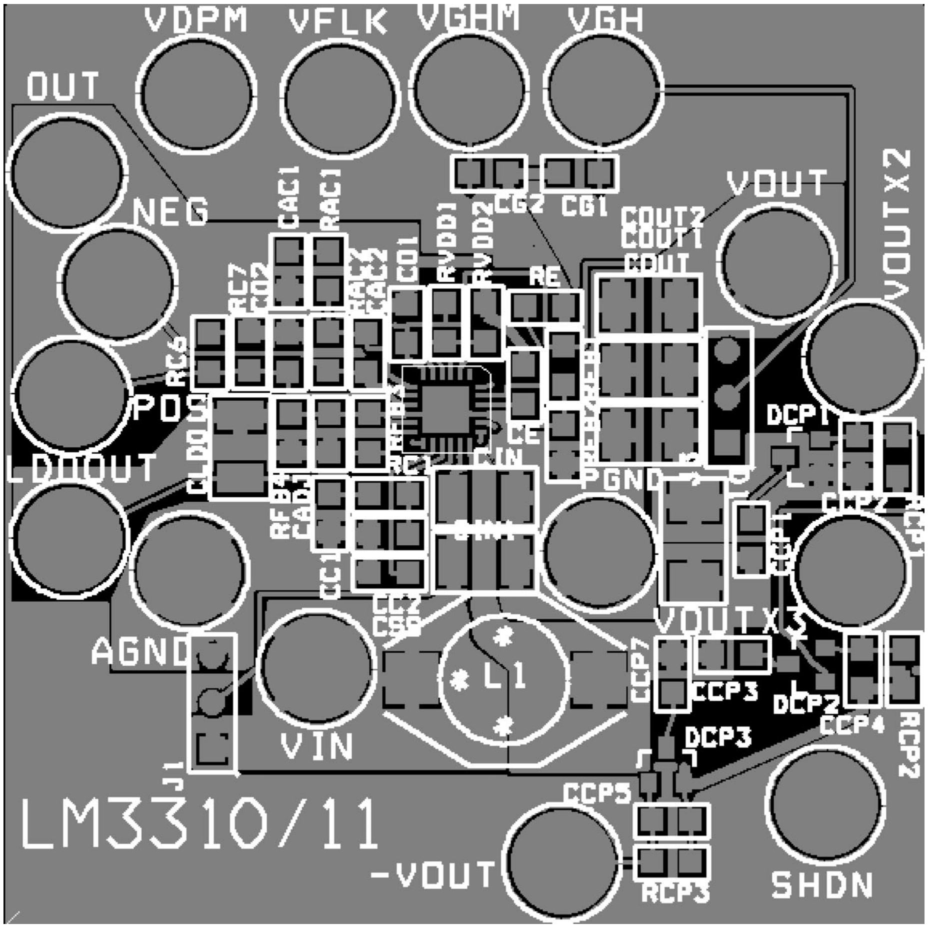


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FIGURE 7. Evaluation Board Layout (top layer)

Application Information (Continued)

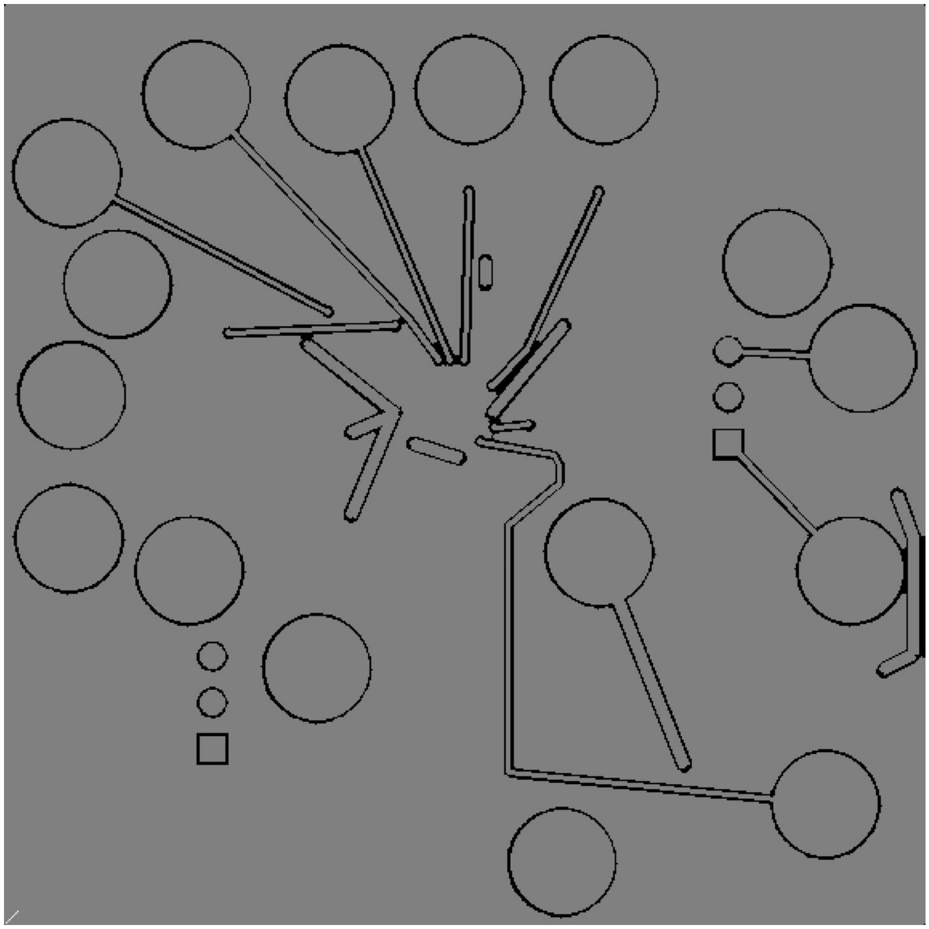

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FIGURE 8. Evaluation Board Layout (bottom layer)

Application Information (Continued)

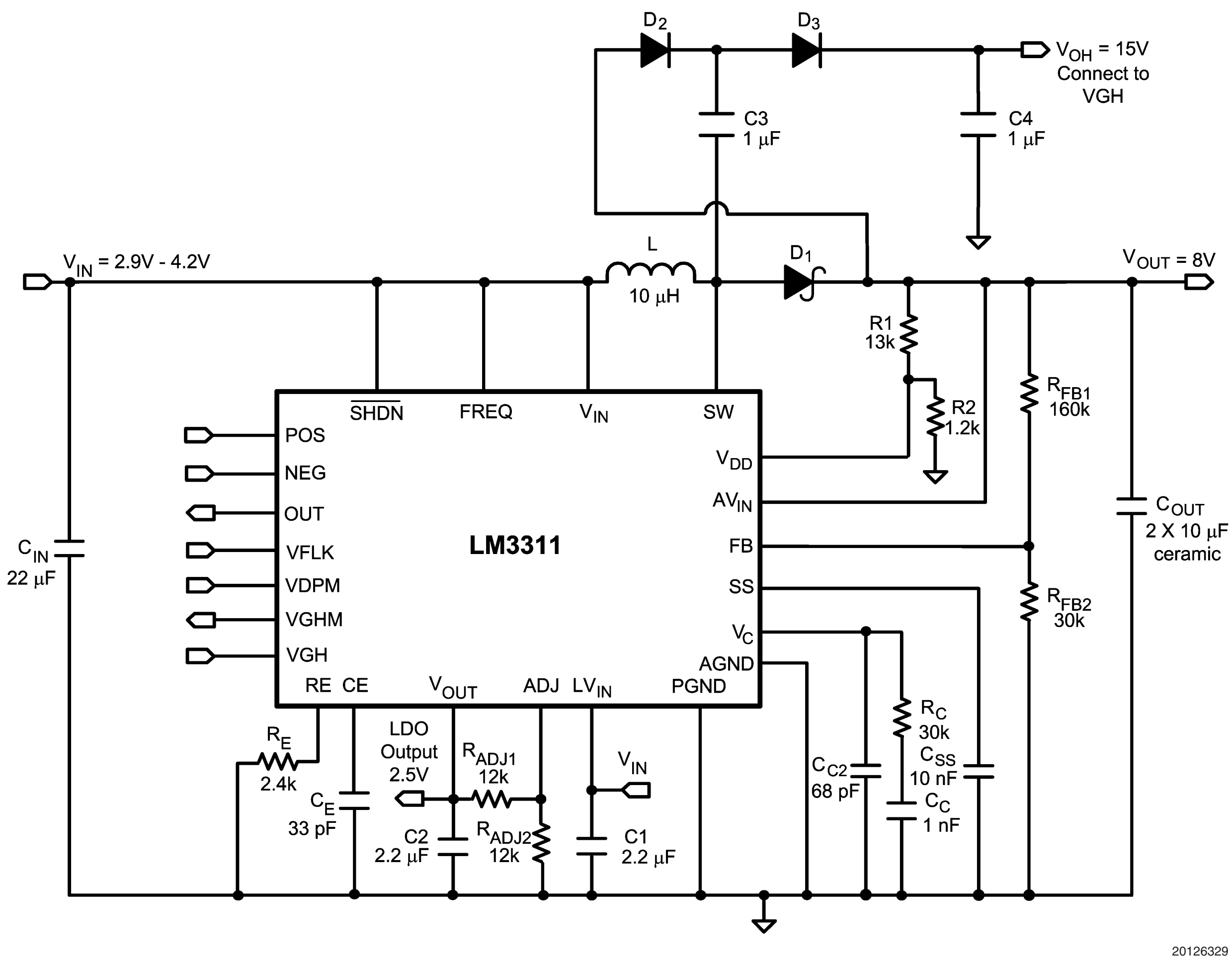


FIGURE 9. Li-Ion to 8V, 1.28MHz Application

Application Information (Continued)

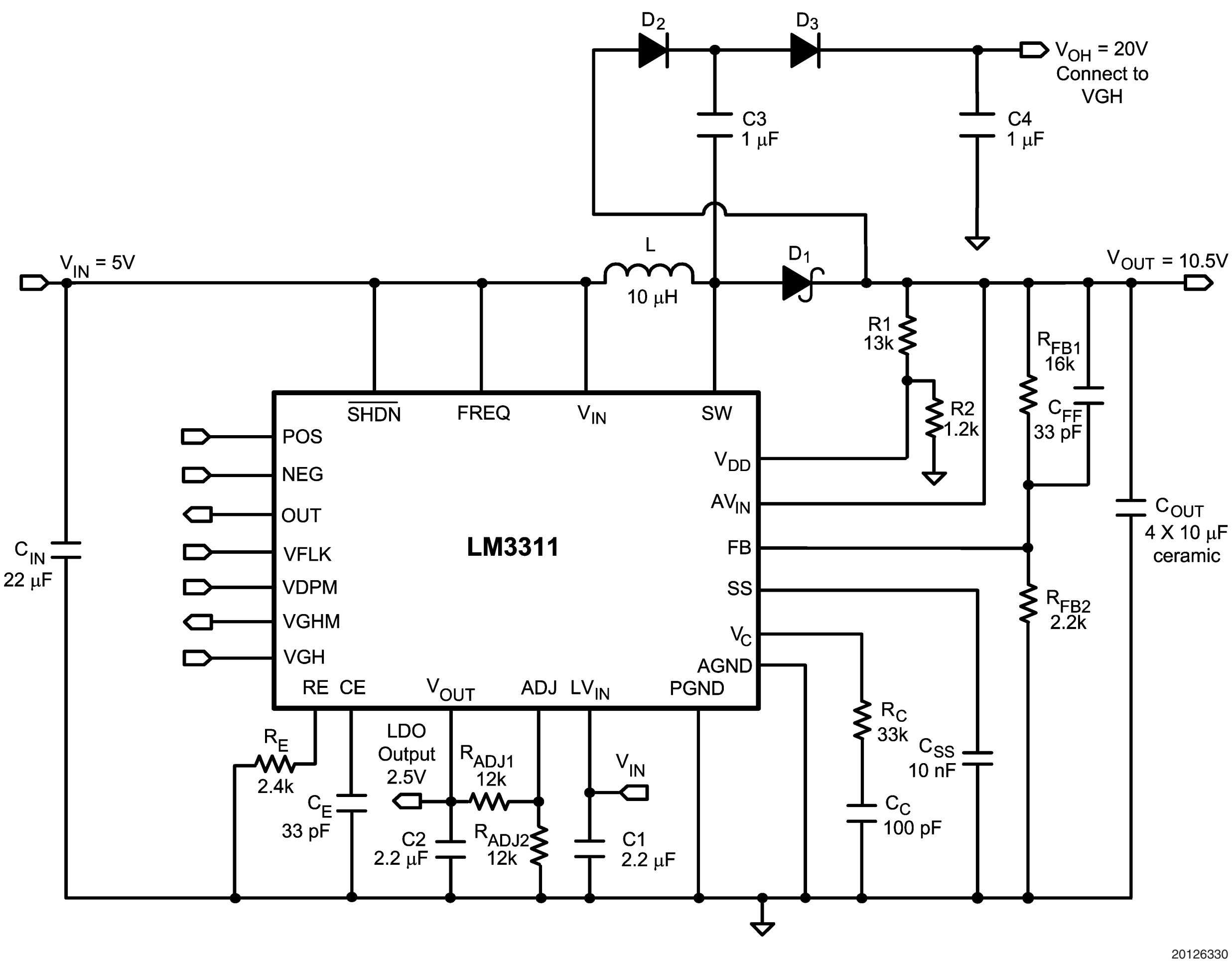


FIGURE 10. 5V to 10.5V, 1.28MHz Application

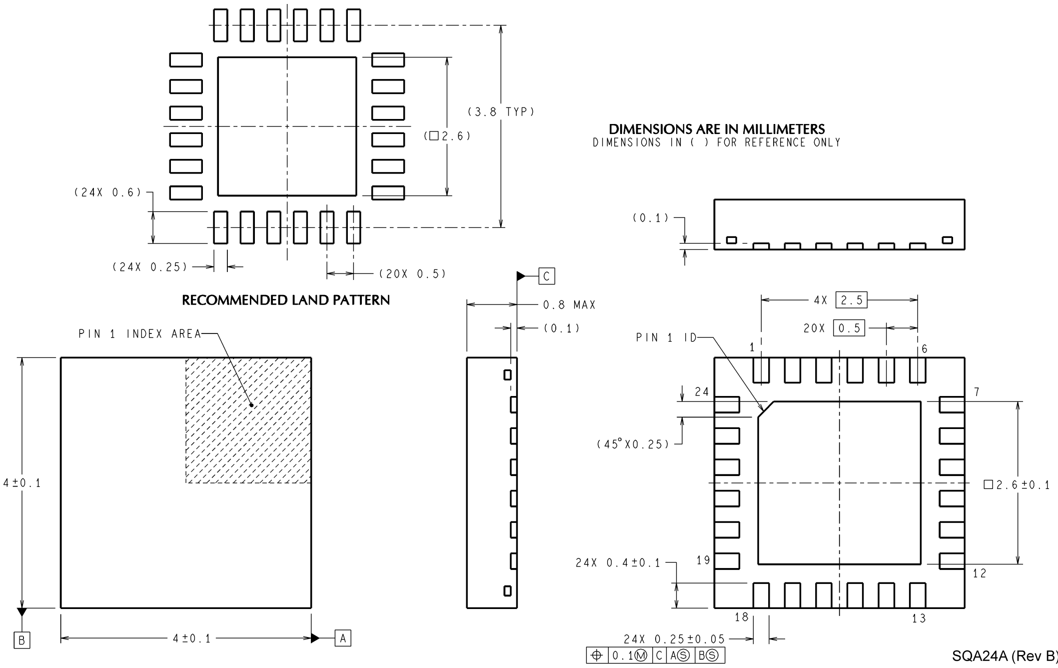
Some recommended Inductors (others may be used)

Manufacturer	Inductor	Contact Information
Coilcraft	DO3316 and DT3316 series	www.coilcraft.com 800-3222645
TDK	SLF10145 series	www.component.tdk.com 847-803-6100
Pulse	P0751 and P0762 series	www.pulseeng.com
Sumida	CDRH8D28 and CDRH8D43 series	www.sumida.com

Some recommended Input and Output Capacitors (others may be used)

Manufacturer	Capacitor	Contact Information
Vishay Sprague	293D, 592D, and 595D series tantalum	www.vishay.com 407-324-4140
Taiyo Yuden	High capacitance MLCC ceramic	www.t-yuden.com 408-573-4150
Cornell Dubilier	ESRD seriec Polymer Aluminum Electrolytic SPV and AFK series V-chip series	www.cde.com
Panasonic	High capacitance MLCC ceramic EEJ-L series tantalum	www.panasonic.com

Physical Dimensions inches (millimeters) unless otherwise noted



LLP-24 Pin Package (SQA)
For Ordering, Refer to Ordering Information Table
NS Package Number SQA24A

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