

# LM4855 Boomer® Audio Power Amplifier Series

## Integrated Audio Amplifier System

### General Description

The LM4855 is an audio power amplifier system capable of delivering 1.1W (typ) of continuous average power into a mono 8Ω bridged-tied load (BTL) with 1% THD+N and 115mW (typ) per channel of continuous average power into stereo 32Ω BTL loads with 0.5% THD+N, using a 5V power supply.

The LM4855 features a 32 step digital volume control and eight distinct output modes. The digital volume control and output modes are programmed through a three-wire SPI serial control interface, that allows flexibility in routing and mixing audio channels.

The LM4855 is designed for cellular phone, PDA, and other portable handheld applications. It delivers high quality output power from a surface-mount package and requires only six external components.

The industry leading micro SMD package only utilizes 2mm x 2.3mm of PCB space, making the LM4855 the most space efficient audio sub system available today.

### Key Specifications

- THD+N at 1kHz, 1.1W into 8Ω BTL 1.0% (typ)
- THD+N at 1kHz, 115mW into 32Ω BTL 0.5% (typ)
- Single Supply Operation 2.6 to 5.0V

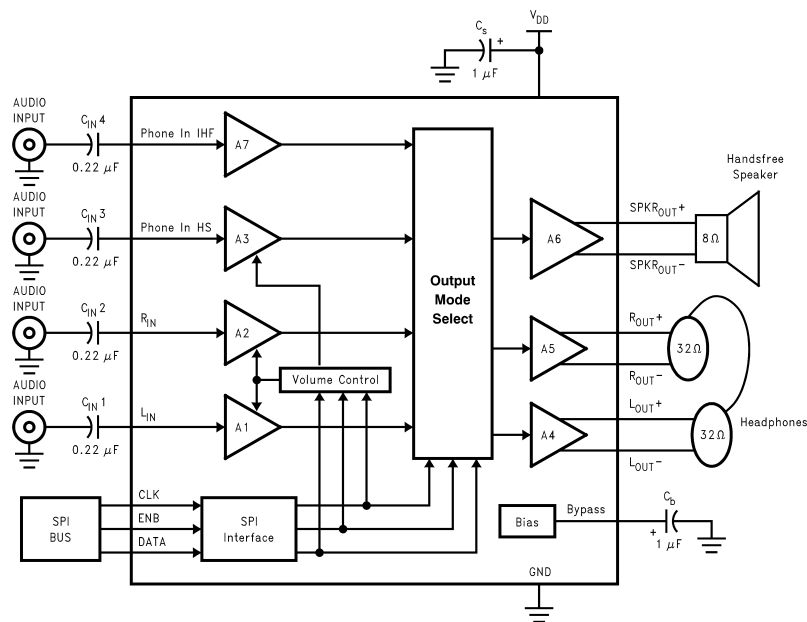
### Features

- 1.1W (typ) output power with 8Ω mono BTL load
- 115mW (typ) output power with stereo 32Ω BTL loads
- SPI programmable 32 step digital volume control
- Eight distinct output modes
- micro-SMD and LLP surface mount packaging
- "Click and Pop" suppression circuitry
- Thermal shutdown protection
- Low shutdown current (0.1uA, typ)

### Applications

- Mobile Phones
- PDAs

### Typical Application



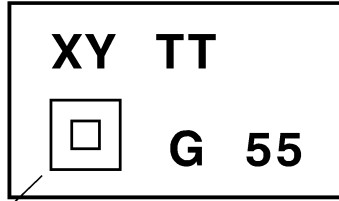
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FIGURE 1. Typical Audio Amplifier Application Circuit

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# Connection Diagrams

18-Bump micro SMD Marking (IBL)

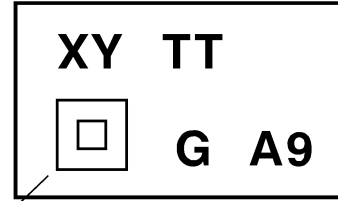


Pin A1

200395B0

**Top View**  
**XY- Date Code**  
**TT - Die Traceability**  
**G - Boomer Family**  
**55 - LM4855IBL**

18-Bump micro SMD Marking (ITL)

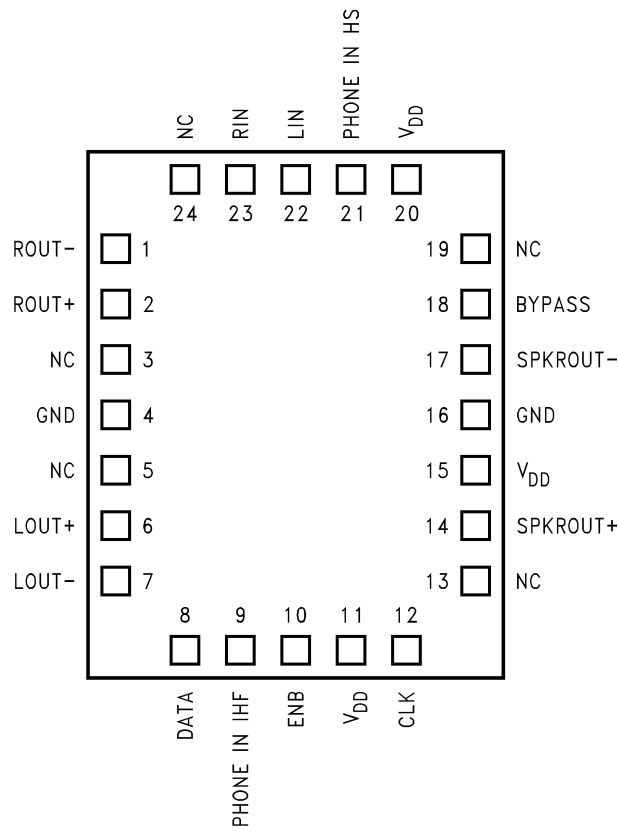


Pin A1

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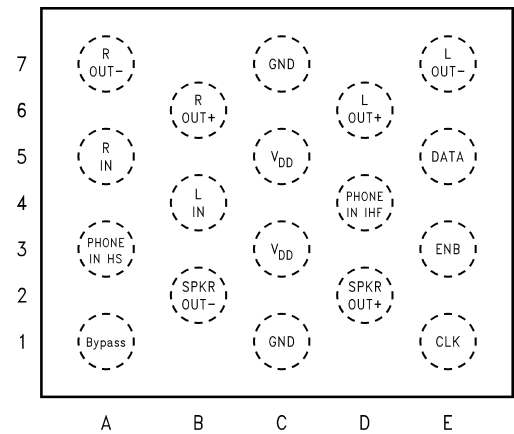
**Top View**  
**XY- Date Code**  
**TT - Die Traceability**  
**G - Boomer Family**  
**A9 - LM4855ITL**

LLP Package



**Top View**  
**Order Number LM4855LQ**  
**See NS Package Number LQA24A for Exposed-DAP LLP**

200395D3



**Top View**  
**(Bump-side down)**  
**Order Number LM4855ITL, LM4855IBL**  
**See NS Package Number TLA18AAA, BLA18AAB**

200395A9

**Absolute Maximum Ratings** (Note 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	6.0V
Storage Temperature	-65°C to +150°C
ESD Susceptibility (Note 4)	2.0kV
ESD Machine model (Note 7)	200V
Junction Temperature (T <sub>J</sub> )	150°C
Solder Information (Note 1)	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C
Thermal Resistance	

θ <sub>JA</sub> (typ) - LQA24A	42°C/W
θ <sub>JC</sub> (typ) - LQA24A	3.0°C/W
θ <sub>JA</sub> (typ) - BLA18AAB	48°C/W (Note 9)
θ <sub>JC</sub> (typ) - BLA18AAB	23°C/W (Note 9)
θ <sub>JA</sub> (typ) - TLA18AAA	48°C/W (Note 9)
θ <sub>JC</sub> (typ) - TLA18AAA	23°C/W (Note 9)

**Operating Ratings** (Note 3)

Temperature Range	-40°C to 85°C
Supply Voltage V <sub>DD</sub>	2.6V ≤ V <sub>DD</sub> ≤ 5.0V

**Note 1:** See AN-450 "Surface Mounting and their effects on Product Reliability" for other methods of soldering surface mount devices.

**Electrical Characteristics** (Notes 3, 8)

The following specifications apply for V<sub>DD</sub> = 5.0V, T<sub>A</sub> = 25°C unless otherwise specified.

Symbol	Parameter	Conditions	LM4855		Units (Limits)
			Typical (Note 5)	Limits (Note 6)	
I <sub>DD</sub>	Supply Current	Output mode 1 V <sub>IN</sub> = 0V; No loads	5.7	8	mA (max)
		Output mode 1 V <sub>IN</sub> = 0V; Loaded (Fig.1)	6.7	9	mA (max)
		Output modes 2, 3, 4, 5, 6, 7 V <sub>IN</sub> = 0V; No loads	7.5	11	mA (max)
		Output modes 2, 3, 4, 5, 6, 7 V <sub>IN</sub> = 0V; Loaded (Fig. 1)	8.5	12	mA (max)
I <sub>SD</sub>	Shutdown Current	Output mode 0	0.1	2.0	μA (max)
V <sub>OS</sub>	Output Offset Voltage	V <sub>IN</sub> = 0V	5.0	40	mV (max)
P <sub>O</sub>	Output Power	SPKR <sub>OUT</sub> ; R <sub>L</sub> = 4Ω THD+N = 1%; f = 1kHz, LM4855LQ	1.5		W
		SPKR <sub>OUT</sub> ; R <sub>L</sub> = 8Ω THD+N = 1%; f = 1kHz	1.1	0.8	W (min)
		R <sub>OUT</sub> and L <sub>OUT</sub> ; R <sub>L</sub> = 32Ω THD+N = 0.5%; f = 1kHz	115	70	mW (min)
THD+N	Total Harmonic Distortion Plus Noise	SPKR <sub>OUT</sub> f = 20Hz to 20kHz P <sub>OUT</sub> = 400mW; R <sub>L</sub> = 8Ω	0.5		%
		R <sub>OUT</sub> and L <sub>OUT</sub> f = 20Hz to 20kHz P <sub>OUT</sub> = 50mW; R <sub>L</sub> = 32Ω	0.5		%
N <sub>OUT</sub>	Output Noise	A-weighted (Note 10)	29		μV

**Electrical Characteristics** (Notes 3, 8) (Continued)The following specifications apply for  $V_{DD} = 5.0V$ ,  $T_A = 25^\circ C$  unless otherwise specified.

Symbol	Parameter	Conditions	LM4855		Units (Limits)	
			Typical (Note 5)	Limits (Note 6)		
PSRR	Power Supply Rejection Ratio SPKR <sub>OUT</sub>	$V_{RIPPLE} = 200mV_{PP}$ ; $f = 217Hz$ , $C_B = 1.0\mu F$ All audio inputs terminated into $50\Omega$ ; Output referred Gain (BTL) = 12dB Output Mode 1, 3, 5, 7	57	54	dB (min)	
	Power Supply Rejection Ratio R <sub>OUT</sub> and L <sub>OUT</sub>	$V_{RIPPLE} = 200mV_{PP}$ ; $f = 217Hz$ , $C_B = 1.0\mu F$ All audio inputs terminated into $50\Omega$ ; Output referred Maximum gain setting				
			Output Mode 2, 3	62	59	dB (min)
Output Mode 4, 5			57	54	dB (min)	
	Output Mode 6, 7	54	51	dB (min)		
V <sub>IH</sub>	Logic High Input Voltage			1.4 V <sub>DD</sub>	V (min) V (max)	
V <sub>IL</sub>	Logic Low Input Voltage			0.4 GND	V (max) V (min)	
	Digital Volume Range (R <sub>IN</sub> and L <sub>IN</sub> )	Input referred minimum gain	-34.5	-35.1 -33.9	dB (min) dB (max)	
		Input referred maximum gain	12.0	11.4 12.6	dB (min) dB (max)	
	Digital Volume Stepsize		1.5		dB	
	Digital Volume Stepsize Error		±0.1	±0.6	dB (max)	
	Phone_In_IHF Volume	BTL gain from Phone_In_IHF to SPKR <sub>OUT</sub>		12	11.4 12.6	dB (min) dB (max)
			Phone_In_IHF Mute Attenuation	Output Mode 2, 4, 6	80	72
	Phone_In_IHF Input Impedance			20	15 25	kΩ (min) kΩ (max)
			Phone_In_HS Input Impedance		Maximum gain setting	50
	Minimum gain setting	100			75 125	kΩ (min) kΩ (max)
	R <sub>IN</sub> and L <sub>IN</sub> Input Impedance		Maximum gain setting	33.5	25 42	kΩ (min) kΩ (max)
			Minimum gain setting	100	75 125	kΩ (min) kΩ (max)
	t <sub>SD</sub>	Thermal Shutdown Temperature		170	150	°C (min)
	t <sub>ES</sub>	Enable Setup Time (ENB)			20	ns (min)
t <sub>EH</sub>	Enable Hold Time (ENB)			20	ns (min)	
t <sub>EL</sub>	Enable Low Time (ENB)			30	ns (min)	
t <sub>DS</sub>	Data Setup Time (DATA)			20	ns (min)	
t <sub>DH</sub>	Data Hold Time (DATA)			20	ns (min)	
t <sub>CS</sub>	Clock Setup Time (CLK)			20	ns (min)	
t <sub>CH</sub>	Clock Logic High Time (CLK)			50	ns (min)	
t <sub>CL</sub>	Clock Logic Low Time (CLK)			50	ns (min)	
f <sub>CLK</sub>	Clock Frequency			DC 10	(min) MHz (max)	

**Electrical Characteristics** (Notes 2, 8)The following specifications apply for  $V_{DD} = 3.0V$ ,  $T_A = 25^\circ C$  unless otherwise specified.

Symbol	Parameter	Conditions	LM4855		Units (Limits)
			Typical (Note 5)	Limits (Note 6)	
$I_{DD}$	Supply Current	Output mode 1 $V_{IN} = 0V$ ; No loads	4.5	7	mA (max)
		Output mode 1 $V_{IN} = 0V$ ; Loaded (Fig.1)	5.0	8	mA (max)
		Output modes 2, 3, 4, 5, 6, 7 $V_{IN} = 0V$ ; No loads	6.5	10	mA (max)
		Output modes 2, 3, 4, 5, 6, 7 $V_{IN} = 0V$ ; Loaded (Fig. 1)	7	11	mA (max)
$I_{SD}$	Shutdown Current	Output mode 0	0.1	2.0	$\mu A$ (max)
$V_{OS}$	Output Offset Voltage	$V_{IN} = 0V$	5.0	40	mV (max)
$P_O$	Output Power	SPKR <sub>OUT</sub> ; $R_L = 4\Omega$ THD+N = 1%; $f = 1kHz$ , LM4855LQ	430		mW
		SPKR <sub>OUT</sub> ; $R_L = 8\Omega$ THD+N = 1%; $f = 1kHz$	340	300	mW (min)
		R <sub>OUT</sub> and L <sub>OUT</sub> ; $R_L = 32\Omega$ THD+N = 0.5%; $f = 1kHz$	25	20	mW (min)
THD+N	Total Harmonic Distortion Plus Noise	SPKR <sub>OUT</sub> $f = 20Hz$ to $20kHz$ $P_{OUT} = 250mW$ ; $R_L = 8\Omega$	0.5		%
		R <sub>OUT</sub> and L <sub>OUT</sub> $f = 20Hz$ to $20kHz$ $P_{OUT} = 20mW$ ; $R_L = 32\Omega$	0.5		%
$N_{OUT}$	Output Noise	A-weighted (Note 10)	29		$\mu V$
PSRR	Power Supply Rejection Ratio SPKR <sub>OUT</sub>	$V_{RIPPLE} = 200mV_{PP}$ ; $f = 217Hz$ , $C_B = 1.0\mu F$ All audio inputs terminated into $50\Omega$ ; Output referred Gain (BTL) = 12dB Output Mode 1, 3, 5, 7	58	55	dB (min)
	Power Supply Rejection Ratio R <sub>OUT</sub> and L <sub>OUT</sub>	$V_{RIPPLE} = 200mV_{PP}$ ; $f = 217Hz$ , $C_B = 1.0\mu F$ All audio inputs terminated into $50\Omega$ ; Output referred Maximum gain setting			
		Output Mode 2, 3	63	60	dB (min)
		Output Mode 4, 5	58	55	dB (min)
		Output Mode 6, 7	55	52	dB (min)
$V_{IH}$	Logic High Input Voltage			1.4 $V_{DD}$	V (min) V (max)
$V_{IL}$	Logic Low Input Voltage			0.4 GND	V (max) V (min)

## Electrical Characteristics (Notes 2, 8) (Continued)

The following specifications apply for  $V_{DD} = 3.0V$ ,  $T_A = 25^\circ C$  unless otherwise specified.

Symbol	Parameter	Conditions	LM4855		Units (Limits)
			Typical (Note 5)	Limits (Note 6)	
	Digital Volume Range ( $R_{IN}$ and $L_{IN}$ )	Input referred minimum gain	-34.5	-35.1 -33.9	dB (min) dB (max)
		Input referred maximum gain	12.0	11.4 12.6	dB (min) dB (max)
	Digital Volume Stepsize		1.5		dB
	Digital Volume Stepsize Error		$\pm 0.1$	$\pm 0.6$	dB ( max)
	Phone_In_IHF Volume	BTL gain from Phone_In_IHF to $SPKR_{OUT}$	12	11.4 12.6	dB (min) dB (max)
	Phone_In_IHF Mute Attenuation	Output Mode 2, 4, 6	80	72	dB (min)
	Phone_In_IHF Input Impedance		20	15 25	k $\Omega$ (min) k $\Omega$ (max)
	Phone_In_HS Input Impedance	Maximum gain setting	50	37.5 62.5	k $\Omega$ (min) k $\Omega$ (max)
		Minimum gain setting	100	75 125	k $\Omega$ (min) k $\Omega$ (max)
	$R_{IN}$ and $L_{IN}$ Input Impedance	Maximum gain setting	33.5	25 42	k $\Omega$ (min) k $\Omega$ (max)
		Minimum gain setting	100	75 125	k $\Omega$ (min) k $\Omega$ (max)
$t_{SD}$	Thermal Shutdown Temperature		170	150	$^\circ C$ (min)
$t_{ES}$	Enable Setup Time (ENB)			20	ns (min)
$t_{EH}$	Enable Hold Time (ENB)			20	ns (min)
$t_{EL}$	Enable Low Time (ENB)			30	ns (min)
$t_{DS}$	Data Setup Time (DATA)			20	ns (min)
$t_{DH}$	Data Hold Time (DATA)			20	ns (min)
$t_{CS}$	Clock Setup Time (CLK)			20	ns (min)
$t_{CH}$	Clock Logic High Time (CLK)			50	ns (min)
$t_{CL}$	Clock Logic Low Time (CLK)			50	ns (min)
$f_{CLK}$	Clock Frequency			DC 10	(min) MHz (max)

**Note 2:** Absolute Maximum Rating indicate limits beyond which damage to the device may occur.

**Note 3:** Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

**Note 4:** Human body model, 100pF discharged through a 1.5k $\Omega$  resistor.

**Note 5:** Typical specifications are specified at +25 $^\circ C$  and represent the most likely parametric norm.

**Note 6:** Tested limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

**Note 7:** Machine Model ESD test is covered by specification EIAJ IC-121-1981. A 200pF cap is charged to the specified voltage, then discharged directly into the IC with no external series resistor (resistance of discharge path must be under 50 $\Omega$ ).

**Note 8:** All voltages are measured with respect to the ground pin, unless otherwise specified.

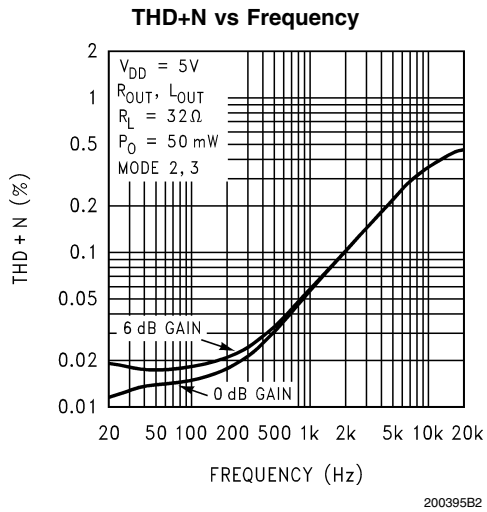
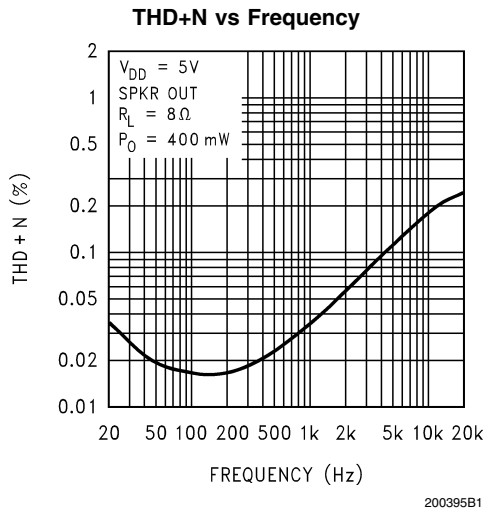
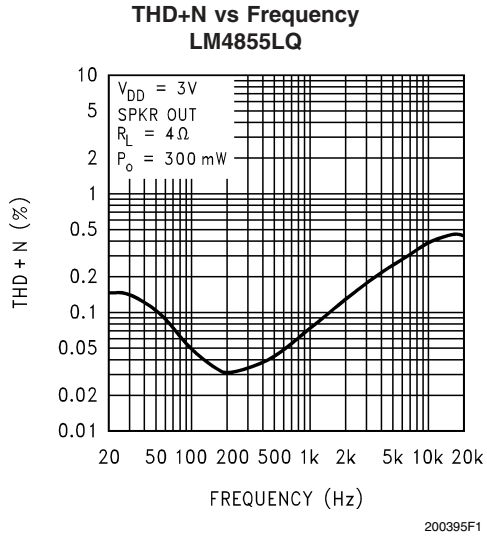
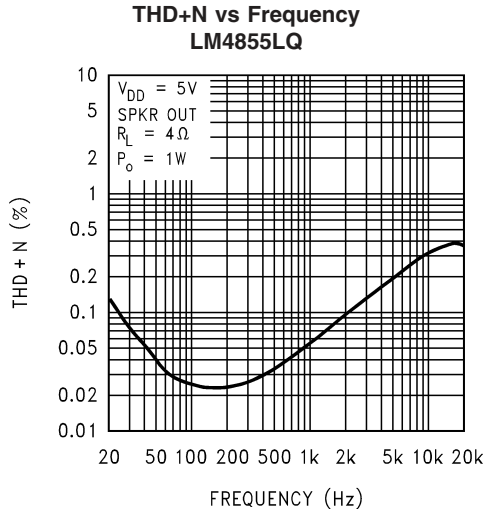
**Note 9:** The given  $\theta_{JA}$  and  $\theta_{JC}$  are for an LM4855 mounted on a demonstration board with a 4in<sup>2</sup> area of 1oz printed circuit board copper ground plane.

**Note 10:** Please refer to the Output Noise vs Output Mode table in the Typical Performance Characteristics section for more details.

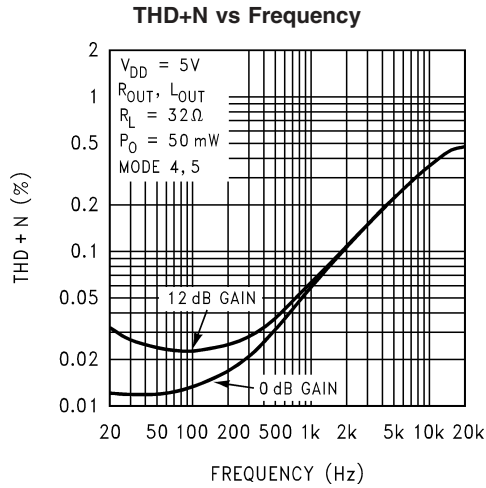
# External Components Description

Components	Functional Description
1. $C_{IN}$	This is the input coupling capacitor. It blocks the DC voltage and couples the input signal to the amplifier's input terminals. $C_{IN}$ also creates a highpass filter with the internal resistor $R_i$ (Input Impedance) at $f_c = 1/(2\pi R_i C_{IN})$ .
2. $C_S$	This is the supply bypass capacitor. It filters the supply voltage applied to the $V_{DD}$ pin and helps maintain the LM4855's PSRR.
3. $C_B$	This is the BYPASS pin capacitor. It filters the $V_{DD} / 2$ voltage and helps maintain the LM4855's PSRR.

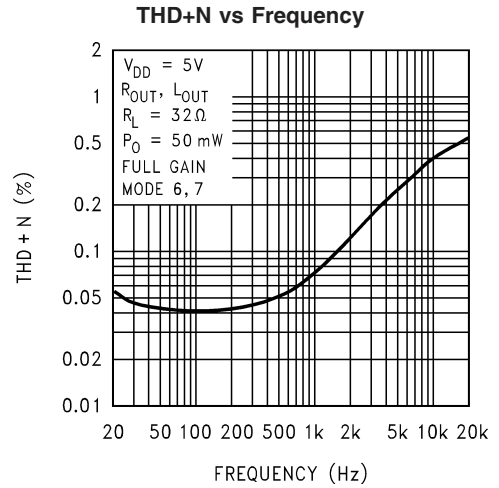
## Typical Performance Characteristics



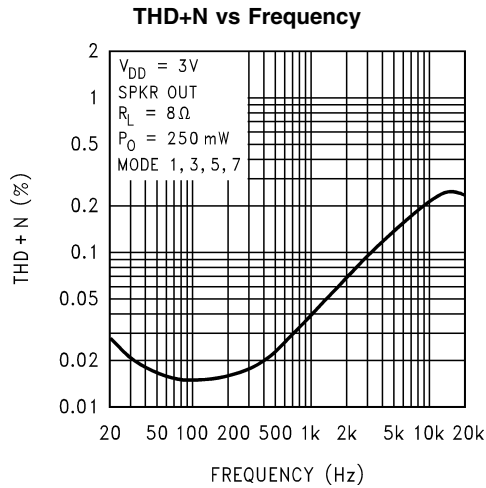
Typical Performance Characteristics (Continued)



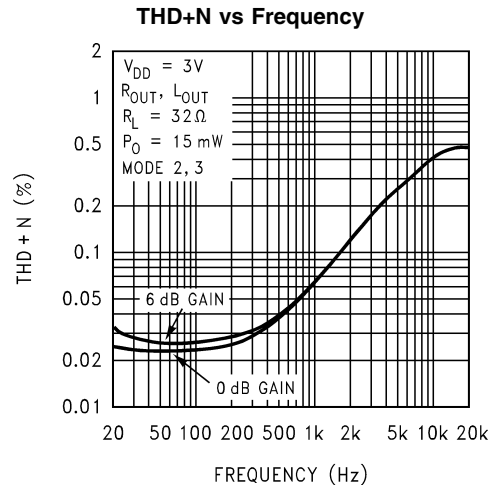
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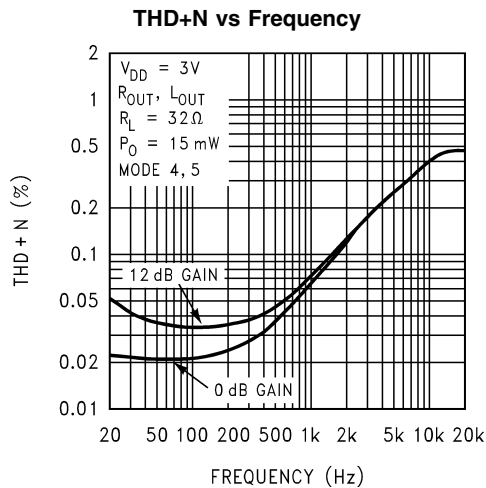
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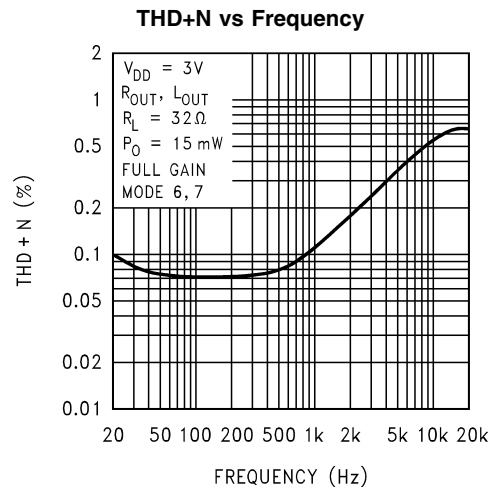
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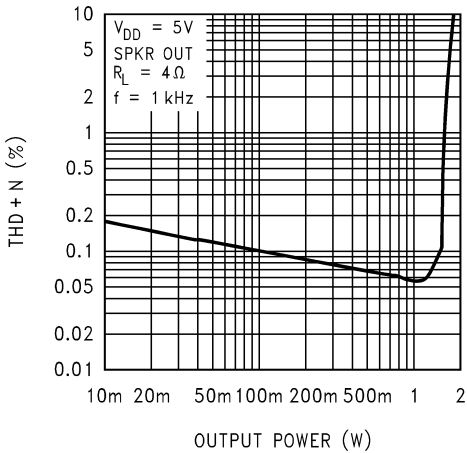
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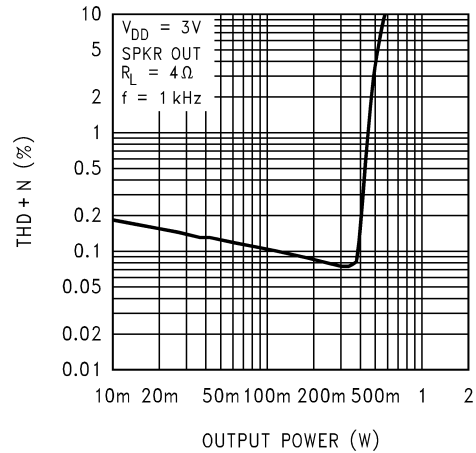
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Typical Performance Characteristics (Continued)

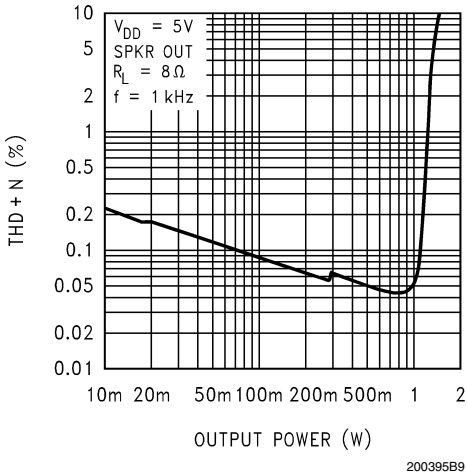
THD+N vs Output Power  
LM4855LQ



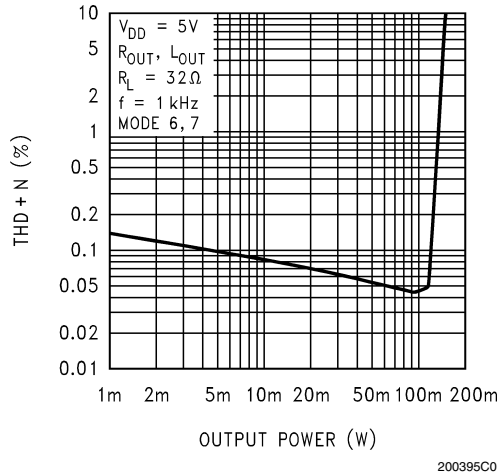
THD+N vs Output Power  
LM4855LQ



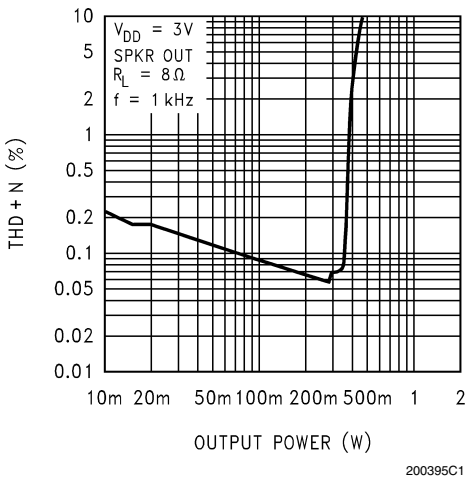
THD+N vs Output Power



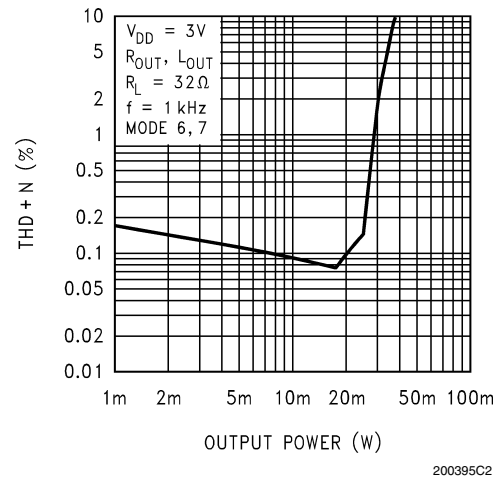
THD+N vs Output Power



THD+N vs Output Power

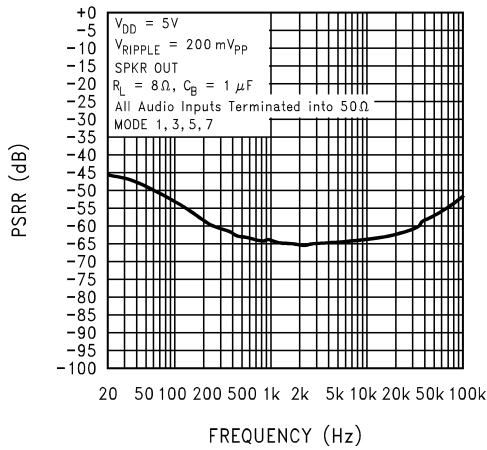


THD+N vs Output Power



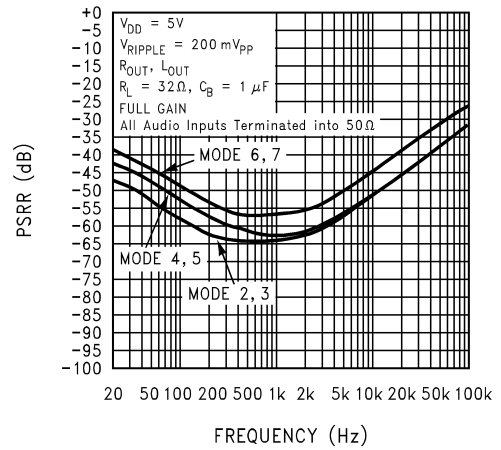
# Typical Performance Characteristics (Continued)

**Power Supply Rejection Ratio**



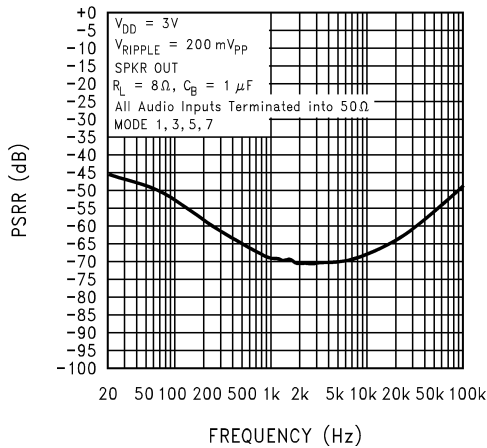
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**Power Supply Rejection Ratio**



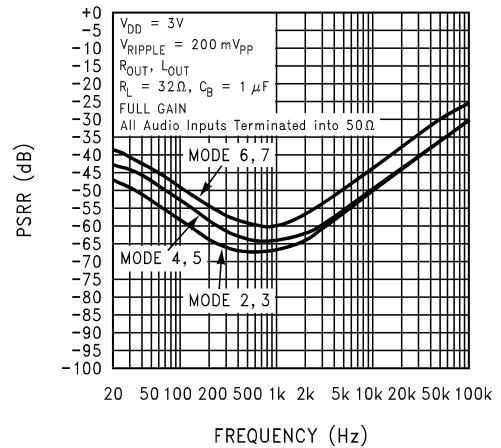
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**Power Supply Rejection Ratio**



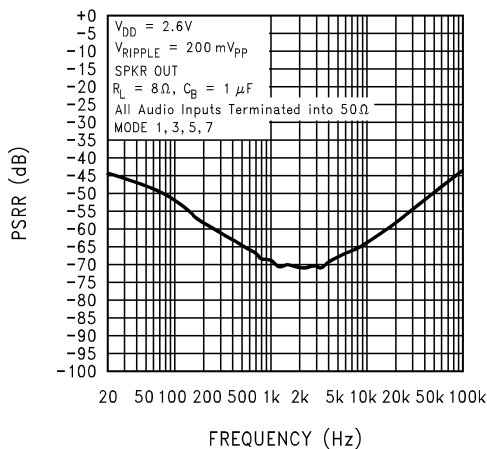
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**Power Supply Rejection Ratio**



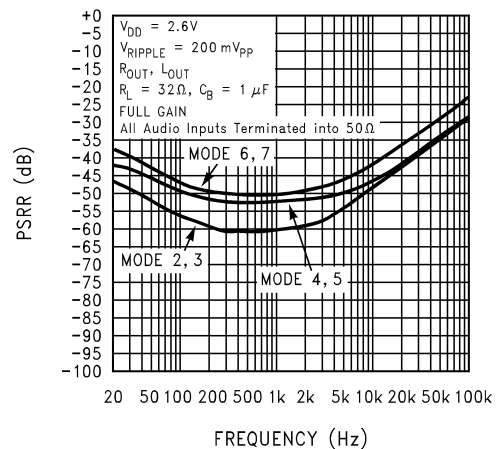
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**Power Supply Rejection Ratio**



200395C7

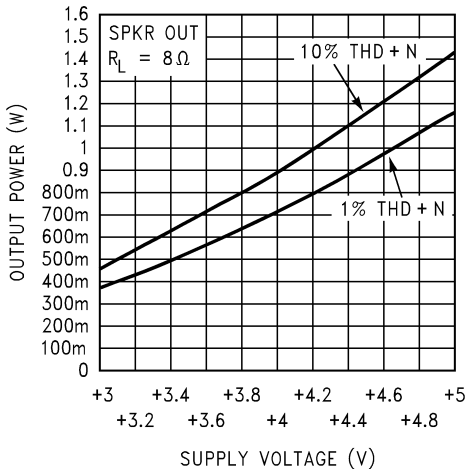
**Power Supply Rejection Ratio**



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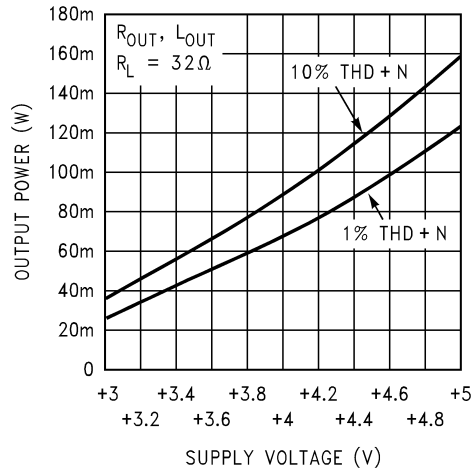
Typical Performance Characteristics (Continued)

Output Power vs Supply Voltage



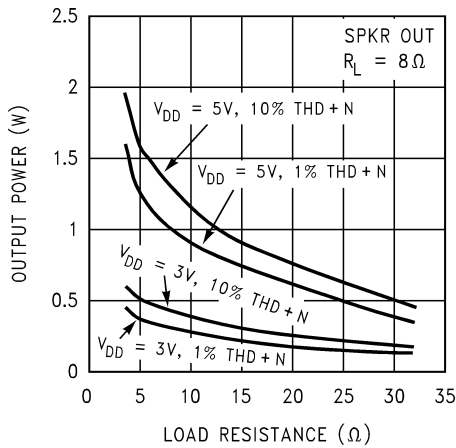
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Output Power vs Supply Voltage



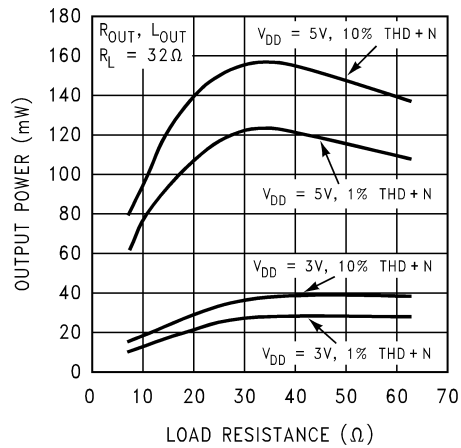
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Output Power vs Load Resistance



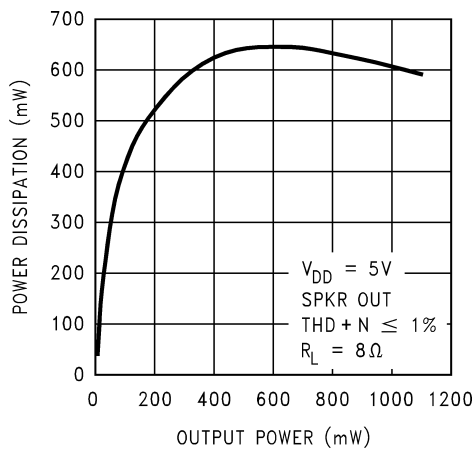
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Output Power vs Load Resistance



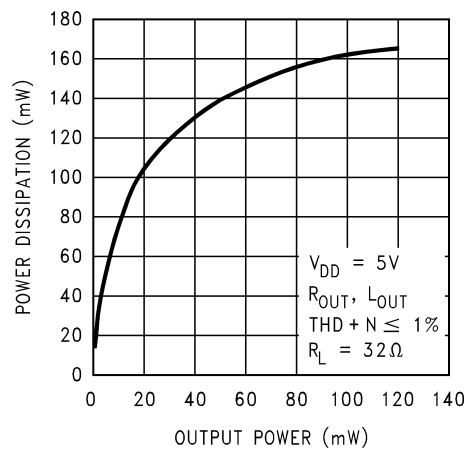
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Power Dissipation vs Output Power



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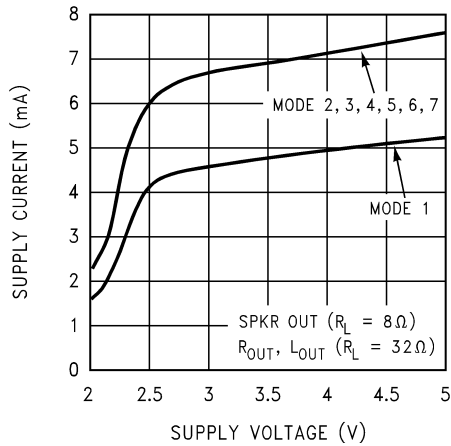
Power Dissipation vs Output Power



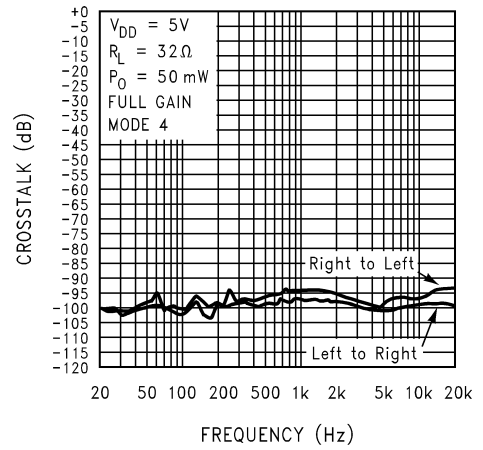
200395E2

# Typical Performance Characteristics (Continued)

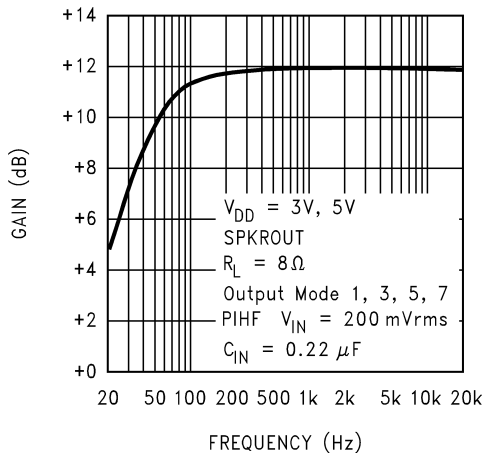
**Supply Current vs Supply Voltage**



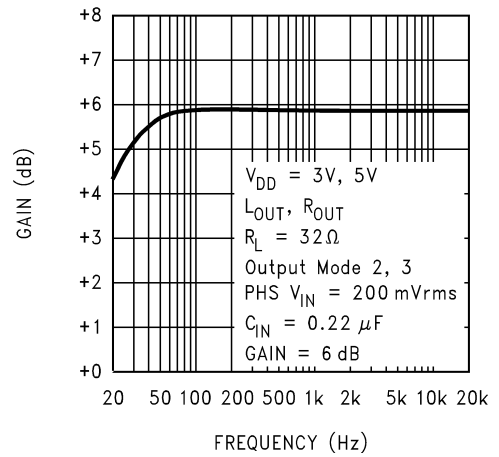
**Channel Separation**



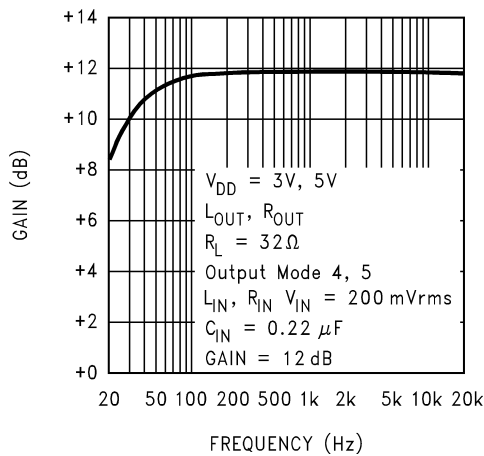
**Frequency Response**



**Frequency Response**



**Frequency Response**



## Typical Performance Characteristics (Continued)

### Output Noise vs Output Mode ( $V_{DD} = 3V, 5V$ )

Output Mode	SPKROUT Output Noise ( $\mu V$ )	LOUT/ROUT Output Noise ( $\mu V$ )
1	29	X
2	X	28 (G1 = 0dB) 31 (G1 = 6dB)
3	29	28 (G1 = 0dB) 31 (G1 = 6dB)
4	X	28 (G2 = 0dB) 38 (G2 = 12dB)
5	29	28 (G2 = 0dB) 38 (G2 = 12dB)
6	X	38 (G2 = 0dB) 41 (G1 = 0dB) 48 (G1 = 6dB)
7	29	38 (G2 = 0dB) 41 (G1 = 0dB) 48 (G1 = 6dB)

G1 = gain from P<sub>HS</sub> to LOUT/ROUT  
 G2 = gain from LIN/RIN to LOUT/ROUT  
 A - weighted filter used

## APPLICATION INFORMATION

### SPI PIN DESCRIPTION

DATA: This is the serial data input pin.

CLK: This is the clock input pin.

ENB: This is the SPI enable pin and is active-high.

### SPI OPERATION DESCRIPTION

The serial data bits are organized into a field which contains 8 bits of data defined by TABLE 1. The Data 0 to Data 2 bits determine the output mode of the LM4855 as shown in TABLE 2. The Data 3 to Data 7 bits determine the volume level setting as illustrated by TABLE 3. For each SPI transfer,

the data bits are written to the DATA pin with the least significant bit (LSB) first. All serial data are sampled at the rising edge of the CLK signal. Once all the data bits have been sampled, ENB transitions from logic-high to logic-low to complete the SPI sequence. All 8 bits must be received before any data latch can occur. Any excess CLK and DATA transitions will be ignored after the eighth rising clock edge has occurred. For any data sequence longer than 8 bits, only the first 8 bits will get loaded into the shift register and the rest of the bits will be disregarded.

**TABLE 1. Bit Allocation**

Data 0	Mode Select
Data 1	Mode Select
Data 2	Mode Select
Data 3	Volume Control
Data 4	Volume Control
Data 5	Volume Control
Data 6	Volume Control
Data 7	Volume Control

**TABLE 2. Output Mode Selection**

Output Mode #	Data 2	Data 1	Data 0	SPKR <sub>OUT</sub>	R <sub>OUT</sub>	L <sub>OUT</sub>
0	0	0	0	SD	SD	SD
1	0	0	1	12dB x P <sub>IHF</sub>	SD	SD
2	0	1	0	MUTE	G1 x P <sub>HS</sub>	G1 x P <sub>HS</sub>
3	0	1	1	12dB x P <sub>IHF</sub>	G1 x P <sub>HS</sub>	G1 x P <sub>HS</sub>
4	1	0	0	MUTE	G2 x R	G2 x L
5	1	0	1	12dB x P <sub>IHF</sub>	G2 x R	G2 x L
6	1	1	0	MUTE	(G1 x P <sub>HS</sub> ) + (G2 x R)	(G1 x P <sub>HS</sub> ) + (G2 x L)
7	1	1	1	12dB x P <sub>IHF</sub>	(G1 x P <sub>HS</sub> ) + (G2 x R)	(G1 x P <sub>HS</sub> ) + (G2 x L)

R = Rin

L = Lin

P<sub>IHF</sub> = Phone\_In\_IHF

P<sub>HS</sub> = Phone\_In\_HS

SD = Shutdown Mode

MUTE = Mute Mode

G1 = gain from P<sub>HS</sub> to LOUT/ROUT

G2 = gain from LIN/ RIN to LOUT/ROUT

Default Mode upon device power-up is Output Mode 0

## APPLICATION INFORMATION (Continued)

TABLE 3. Volume Control Settings

Gain (dB)		Data 7	Data 6	Data 5	Data 4	Data 3
G2	G1					
R <sub>IN</sub> , L <sub>IN</sub> to R <sub>OUT</sub> , L <sub>OUT</sub>	Phone_In_HS to R <sub>OUT</sub> , L <sub>OUT</sub>					
-34.5	-40.5	0	0	0	0	0
-33.0	-39.0	0	0	0	0	1
-31.5	-37.5	0	0	0	1	0
-30.0	-36.0	0	0	0	1	1
-28.5	-34.5	0	0	1	0	0
-27.0	-33.0	0	0	1	0	1
-25.5	-31.5	0	0	1	1	0
-24.0	-30.0	0	0	1	1	1
-22.5	-28.5	0	1	0	0	0
-21.0	-27.0	0	1	0	0	1
-19.5	-25.5	0	1	0	1	0
-18.0	-24.0	0	1	0	1	1
-16.5	-22.5	0	1	1	0	0
-15.0	-21.0	0	1	1	0	1
-13.5	-19.5	0	1	1	1	0
-12.0	-18.0	0	1	1	1	1
-10.5	-16.5	1	0	0	0	0
-9.0	-15.0	1	0	0	0	1
-7.5	-13.5	1	0	0	1	0
-6.0	-12.0	1	0	0	1	1
-4.5	-10.5	1	0	1	0	0
-3.0	-9.0	1	0	1	0	1
-1.5	-7.5	1	0	1	1	0
0.0	-6.0	1	0	1	1	1
1.5	-4.5	1	1	0	0	0
3.0	-3.0	1	1	0	0	1
4.5	-1.5	1	1	0	1	0
6.0	0	1	1	0	1	1
7.5	1.5	1	1	1	0	0
9.0	3.0	1	1	1	0	1
10.5	4.5	1	1	1	1	0
12.0	6.0	1	1	1	1	1

## APPLICATION INFORMATION

(Continued)

### SPI OPERATIONAL REQUIREMENTS

1. The data bits are transmitted with the LSB first.
2. The maximum clock rate is 10MHz for the CLK pin.
3. CLK must remain logic-high for at least 50ns ( $t_{CH}$ ) after the rising edge of CLK, and CLK must remain logic-low for at least 50ns ( $t_{CL}$ ) after the falling edge of CLK.
4. The serial data bits are sampled at the rising edge of CLK. Any transition on DATA must occur at least 20ns ( $t_{DS}$ ) before the rising edge of CLK. Also, any transition on DATA must occur at least 20ns ( $t_{DH}$ ) after the rising edge of CLK and stabilize before the next rising edge of CLK.
5. ENB should be logic-high only during serial data transmission.
6. ENB must be logic-high at least 20ns ( $t_{ES}$ ) before the first rising edge of CLK, and ENB has to remain logic-high at least 20ns ( $t_{EH}$ ) after the eighth rising edge of CLK.
7. If ENB remains logic-low for more than 10ns before all 8 bits are transmitted then the data latch will be aborted.
8. If ENB is logic-high for more than 8 CLK pulses then only the first 8 data bits will be latched and activated when ENB transitions to logic-low.
9. ENB must remain logic-low for at least 30ns ( $t_{EL}$ ) to latch in the data.
10. Coincidental rising or falling edges of CLK and ENB are not allowed. If CLK is to be held logic-high after the data transmission, the falling edge of CLK must occur at least 20ns ( $t_{CS}$ ) before ENB transitions to logic-high for the next set of data.

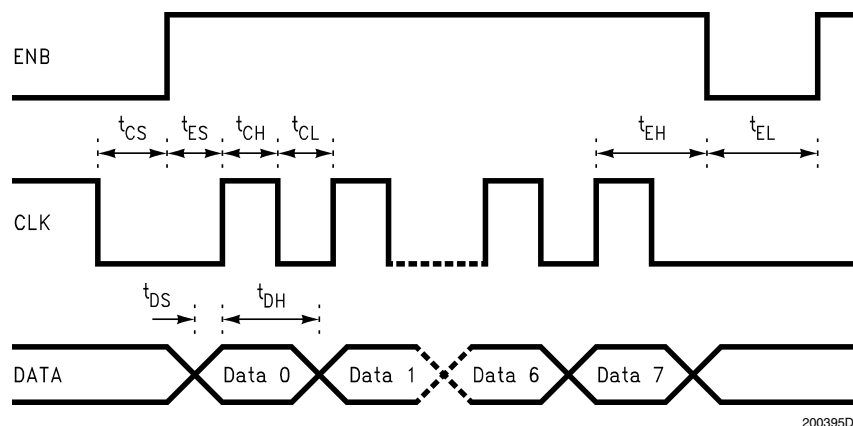


FIGURE 2. SPI Timing Diagram

### EXPOSED-DAP MOUNTING CONSIDERATIONS

The LM4855's exposed-DAP (die attach paddle) package (LD) provides a low thermal resistance between the die and the PCB to which the part is mounted and soldered. This allows rapid heat transfer from the die to the surrounding PCB copper area heatsink, copper traces, ground plane, and finally, surrounding air. The result is a low voltage audio power amplifier that produces 1.1W dissipation in a 8Ω load at  $\leq 1\%$  THD+N. This high power is achieved through careful consideration of necessary thermal design. Failing to optimize thermal design may compromise the LM4855's high power performance and activate unwanted, though necessary, thermal shutdown protection.

The LD package must have its DAP soldered to a copper pad on the PCB. The DAP's PCB copper pad is then, ideally, connected to a large plane of continuous unbroken copper. This plane forms a thermal mass, heat sink, and radiation area. Place the heat sink area on either outside plane in the case of a two-sided or multi-layer PCB. (The heat sink area can also be placed on an inner layer of a multi-layer board. The thermal resistance, however, will be higher.) Connect the DAP copper pad to the inner layer or backside copper heat sink area with 6 (3 X 2) (LD) vias. The via diameter should be 0.012in - 0.013in with a 1.27mm pitch. Ensure efficient thermal conductivity by plugging and tenting the vias with plating and solder mask, respectively.

Best thermal performance is achieved with the largest practical copper heat sink area. If the heatsink and amplifier

share the same PCB layer, a nominal 2.5in<sup>2</sup> (min) area is necessary for 5V operation with a 4Ω load. Heatsink areas not placed on the same PCB layer as the LM4855 should be 5in<sup>2</sup> (min) for the same supply voltage and load resistance. The last two area recommendations apply for 25°C ambient temperature. Increase the area to compensate for ambient temperatures above 25°C. In all circumstances and under all conditions, the junction temperature must be held below 150°C to prevent activating the LM4855's thermal shutdown protection. Further detailed and specific information concerning PCB layout and fabrication and mounting an LD (LLP) is found in National Semiconductor's AN1187.

### PCB LAYOUT AND SUPPLY REGULATION CONSIDERATIONS FOR DRIVING 3Ω AND 4Ω LOADS

Power dissipated by a load is a function of the voltage swing across the load and the load's impedance. As load impedance decreases, load dissipation becomes increasingly dependent on the interconnect (PCB trace and wire) resistance between the amplifier output pins and the load's connections. Residual trace resistance causes a voltage drop, which results in power dissipated in the trace and not in the load as desired. For example, 0.1Ω trace resistance reduces the output power dissipated by a 4Ω load from 1.7W to 1.6W. The problem of decreased load dissipation is exacerbated as load impedance decreases. Therefore, to maintain the

## APPLICATION INFORMATION

(Continued)

highest load dissipation and widest output voltage swing, PCB traces that connect the output pins to a load must be as wide as possible.

Poor power supply regulation adversely affects maximum output power. A poorly regulated supply's output voltage decreases with increasing load current. Reduced supply voltage causes decreased headroom, output signal clipping, and reduced output power. Even with tightly regulated supplies, trace resistance creates the same effects as poor supply regulation. Therefore, making the power supply traces as wide as possible helps maintain full output voltage swing.

### BRIDGE CONFIGURATION EXPLANATION

As shown in Figure 1, the LM4855 consists of three pairs of output amplifier blocks (A4-A6). A4, A5, and A6 consist of bridged-tied amplifier pairs that drive LOUT, ROUT, and SPKROUT respectively. The LM4855 drives a load, such as a speaker, connected between outputs, SPKROUT+ and SPKROUT-. In the amplifier block A6, the output of the amplifier that drives SPKROUT- serves as the input to the unity gain inverting amplifier that drives SPKROUT+.

This results in both amplifiers producing signals identical in magnitude, but 180° out of phase. Taking advantage of this phase difference, a load is placed between SPKROUT- and SPKROUT+ and driven differentially (commonly referred to as 'bridge mode'). This results in a differential or BTL gain of:

$$A_{VD} = 2(R_f/R_i) = 2 \quad (1)$$

Bridge mode amplifiers are different from single-ended amplifiers that drive loads connected between a single amplifier's output and ground. For a given supply voltage, bridge mode has a distinct advantage over the single-ended configuration: its differential output doubles the voltage swing across the load. Theoretically, this produces four times the output power when compared to a single-ended amplifier under the same conditions. This increase in attainable output power assumes that the amplifier is not current limited and that the output signal is not clipped.

Another advantage of the differential bridge output is no net DC voltage across the load. This is accomplished by biasing SPKROUT- and SPKROUT+ outputs at half-supply. This eliminates the coupling capacitor that single supply, single-ended amplifiers require. Eliminating an output coupling capacitor in a typical single-ended configuration forces a single-supply amplifier's half-supply bias voltage across the load. This increases internal IC power dissipation and may permanently damage loads such as speakers.

### POWER DISSIPATION

Power dissipation is a major concern when designing a successful single-ended or bridged amplifier.

A direct consequence of the increased power delivered to the load by a bridge amplifier is higher internal power dissipation. The LM4855 has a pair of bridged-tied amplifiers driving a handsfree speaker, SPKROUT. The maximum internal power dissipation operating in the bridge mode is twice that of a single-ended amplifier. From Equation (2), assuming a 5V power supply and an 8Ω load, the maximum SPKROUT power dissipation is 634mW.

$$P_{\text{DMAX-SPKROUT}} = 4(V_{\text{DD}})^2 / (2\pi^2 R_L): \text{ Bridge Mode} \quad (2)$$

The LM4855 also has 2 pairs of bridged-tied amplifiers driving stereo headphones, ROUT and LOUT. The maximum internal power dissipation for ROUT and LOUT is given by equation (3) and (4). From Equations (3) and (4), assuming a 5V power supply and a 32Ω load, the maximum power dissipation for LOUT and ROUT is 158mW, or 316mW total.

$$P_{\text{DMAX-LOUT}} = 4(V_{\text{DD}})^2 / (2\pi^2 R_L): \text{ Bridge Mode} \quad (3)$$

$$P_{\text{DMAX-ROUT}} = 4(V_{\text{DD}})^2 / (2\pi^2 R_L): \text{ Bridge Mode} \quad (4)$$

The maximum internal power dissipation of the LM4855 occurs when all 3 amplifier pairs are simultaneously on; and is given by Equation (5).

$$P_{\text{DMAX-TOTAL}} = P_{\text{DMAX-SPKROUT}} + P_{\text{DMAX-LOUT}} + P_{\text{DMAX-ROUT}} \quad (5)$$

The maximum power dissipation point given by Equation (5) must not exceed the power dissipation given by Equation (6):

$$P_{\text{DMAX}}' = (T_{\text{JMAX}} - T_A) / \theta_{\text{JA}} \quad (6)$$

The LM4855's  $T_{\text{JMAX}} = 150^\circ\text{C}$ . In the IBL package, the LM4855's  $\theta_{\text{JA}}$  is 48°C/W. In the LD package soldered to a DAP pad that expands to a copper area of 2.5in<sup>2</sup> on a PCB, the LM4855's  $\theta_{\text{JA}}$  is 42°C/W. At any given ambient temperature  $T_A$ , use Equation (6) to find the maximum internal power dissipation supported by the IC packaging. Rearranging Equation (6) and substituting  $P_{\text{DMAX-TOTAL}}$  for  $P_{\text{DMAX}}'$  results in Equation (7). This equation gives the maximum ambient temperature that still allows maximum stereo power dissipation without violating the LM4855's maximum junction temperature.

$$T_A = T_{\text{JMAX}} - P_{\text{DMAX-TOTAL}} \theta_{\text{JA}} \quad (7)$$

For a typical application with a 5V power supply and an 8Ω load, the maximum ambient temperature that allows maximum stereo power dissipation without exceeding the maximum junction temperature is approximately 104°C for the IBL package.

$$T_{\text{JMAX}} = P_{\text{DMAX-TOTAL}} \theta_{\text{JA}} + T_A \quad (8)$$

Equation (8) gives the maximum junction temperature  $T_{\text{JMAX}}$ . If the result violates the LM4855's 150°C, reduce the maximum junction temperature by reducing the power supply voltage or increasing the load resistance. Further allowance should be made for increased ambient temperatures.

The above examples assume that a device is a surface mount part operating around the maximum power dissipation point. Since internal power dissipation is a function of output power, higher ambient temperatures are allowed as output power or duty cycle decreases. If the result of Equation (5) is greater than that of Equation (6), then decrease the supply

## APPLICATION INFORMATION

(Continued)

voltage, increase the load impedance, or reduce the ambient temperature. If these measures are insufficient, a heat sink can be added to reduce  $\theta_{JA}$ . The heat sink can be created using additional copper area around the package, with connections to the ground pin(s), supply pin and amplifier output pins. External, solder attached SMT heatsinks such as the Thermalloy 7106D can also improve power dissipation. When adding a heat sink, the  $\theta_{JA}$  is the sum of  $\theta_{JC}$ ,  $\theta_{CS}$ , and  $\theta_{SA}$ . ( $\theta_{JC}$  is the junction-to-case thermal impedance,  $\theta_{CS}$  is the case-to-sink thermal impedance, and  $\theta_{SA}$  is the sink-to-ambient thermal impedance.) Refer to the Typical Performance Characteristics curves for power dissipation information at lower output power levels.

### POWER SUPPLY BYPASSING

As with any power amplifier, proper supply bypassing is critical for low noise performance and high power supply rejection. Applications that employ a 5V regulator typically use a 10 $\mu$ F in parallel with a 0.1 $\mu$ F filter capacitors to stabilize the regulator's output, reduce noise on the supply line, and improve the supply's transient response. However, their presence does not eliminate the need for a local 1.0 $\mu$ F tantalum bypass capacitance connected between the LM4855's supply pins and ground. Keep the length of leads and traces that connect capacitors between the LM4855's power supply pin and ground as short as possible. Connecting a 1 $\mu$ F capacitor,  $C_B$ , between the BYPASS pin and ground improves the internal bias voltage's stability and improves the amplifier's PSRR. The PSRR improvements increase as the bypass pin capacitor value increases. Too large, however, increases turn-on time and can compromise the amplifier's click and pop performance. The selection of bypass capacitor values, especially  $C_B$ , depends on desired PSRR requirements, click and pop performance (as explained in the section, Proper Selection of External Components), system cost, and size constraints.

## SELECTING EXTERNAL COMPONENTS

### Input Capacitor Value Selection

Amplifying the lowest audio frequencies requires high value input coupling capacitor ( $C_i$  in Figure 2). A high value capacitor can be expensive and may compromise space efficiency in portable designs. In many cases, however, the speakers used in portable systems, whether internal or external, have little ability to reproduce signals below 150Hz. Applications using speakers with this limited frequency response reap little improvement by using large input capacitor.

The internal input resistor ( $R_i$ ) and the input capacitor ( $C_i$ ) produce a high pass filter cutoff frequency that is found using Equation (9).

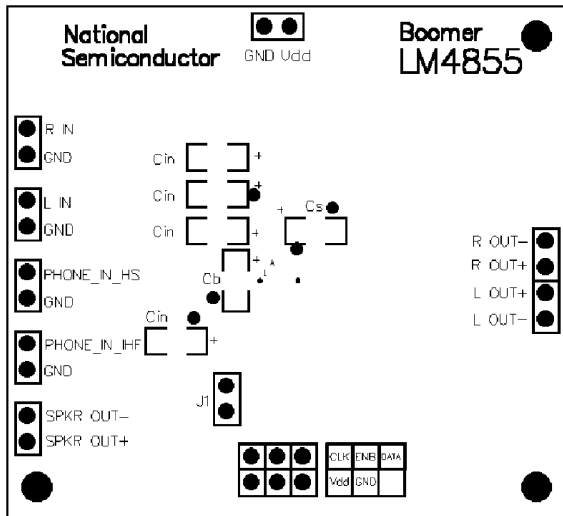
$$f_c = 1 / (2\pi R_i C_i) \quad (9)$$

As an example when using a speaker with a low frequency limit of 150Hz,  $C_i$ , using Equation (9) is 0.063 $\mu$ F. The 0.22 $\mu$ F  $C_i$  shown in Figure 1 allows the LM4855 to drive high efficiency, full range speaker whose response extends below 40Hz.

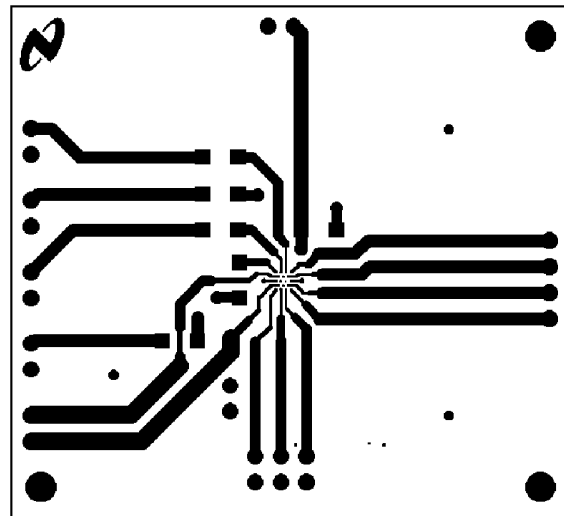
### Bypass Capacitor Value Selection

Besides minimizing the input capacitor size, careful consideration should be paid to value of  $C_B$ , the capacitor connected to the BYPASS pin. Since  $C_B$  determines how fast the LM4855 settles to quiescent operation, its value is critical when minimizing turn-on pops. The slower the LM4855's outputs ramp to their quiescent DC voltage (nominally  $V_{DD}/2$ ), the smaller the turn-on pop. Choosing  $C_B$  equal to 1.0 $\mu$ F along with a small value of  $C_i$  (in the range of 0.1 $\mu$ F to 0.39 $\mu$ F), produces a click-less and pop-less shutdown function. As discussed above, choosing  $C_i$  no larger than necessary for the desired bandwidth helps minimize clicks and pops.  $C_B$ 's value should be in the range of 5 times to 7 times the value of  $C_i$ . This ensures that output transients are eliminated when power is first applied or the LM4855 resumes operation after shutdown.

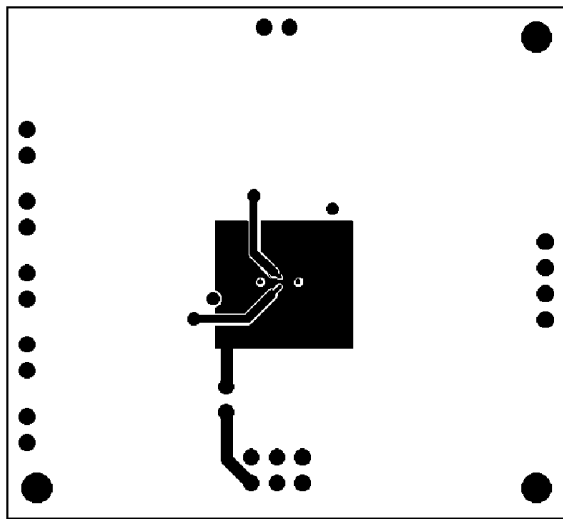
# Demonstration Board Layout



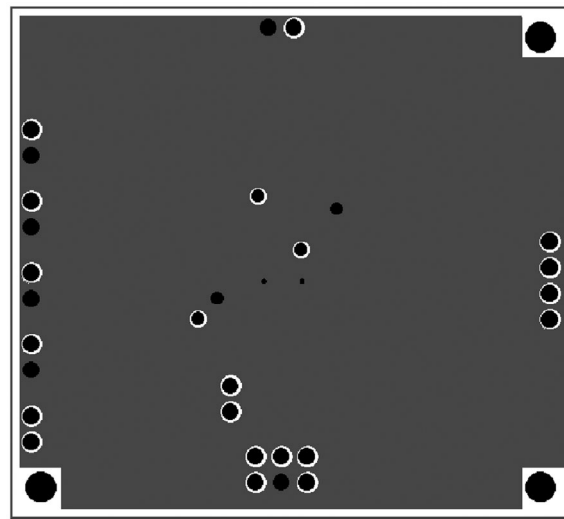
200395A7  
**FIGURE 3. Recommended IBL, ITL PC Board Layout: Top Silkscreen**



200395A6  
**FIGURE 4. Recommended IBL, ITL PC Board Layout: Top Layer**

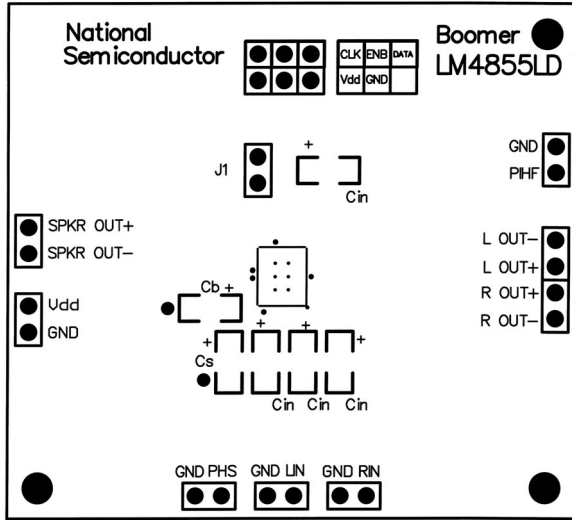


200395A5  
**FIGURE 5. Recommended IBL, ITL PC Board Layout: Middle Layer**

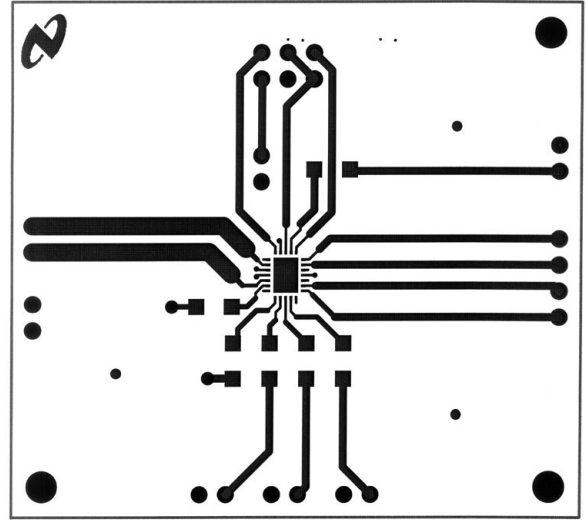


200395A4  
**FIGURE 6. Recommended IBL, ITL PC Board Layout: Bottom Layer**

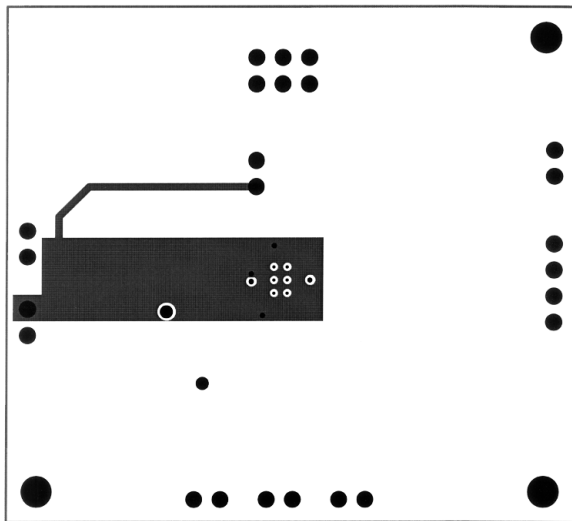
# Demonstration Board Layout (Continued)



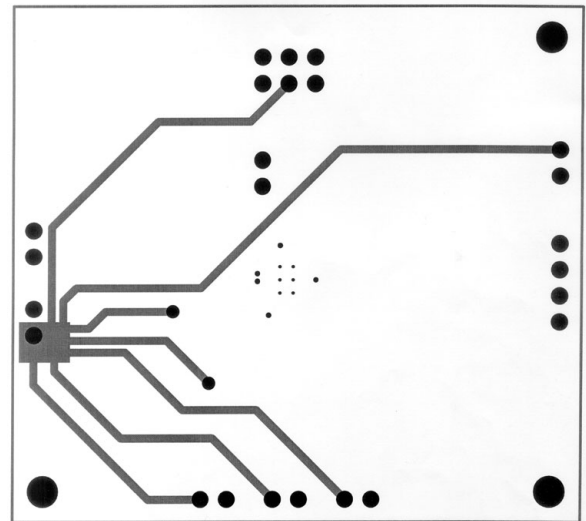
200395E5  
**FIGURE 7. Recommended LD PC Board Layout: Top Silkscreen Layer**



200395E6  
**FIGURE 8. Recommended LD PC Board Layout: Top Layer**

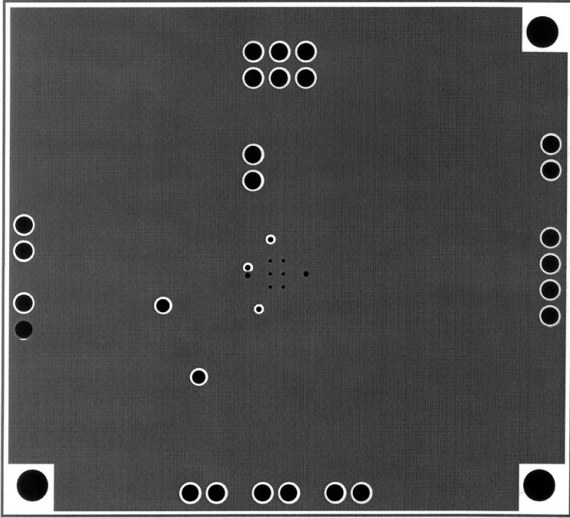


200395E7  
**FIGURE 9. Recommended LD PC Board Layout: Inner Layer 1**



200395E8  
**FIGURE 10. Recommended LD PC Board Layout: Inner Layer 2**

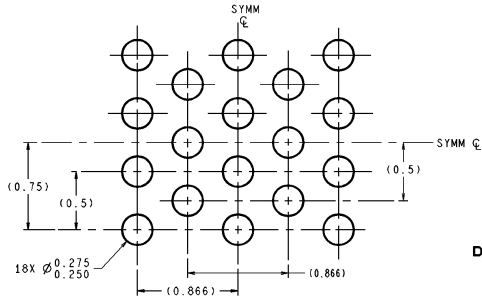
# Demonstration Board Layout (Continued)



200395E9

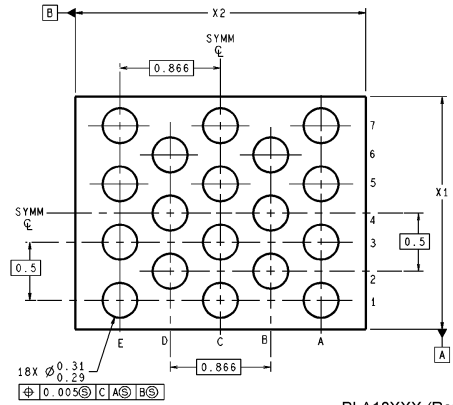
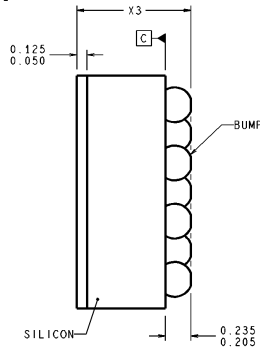
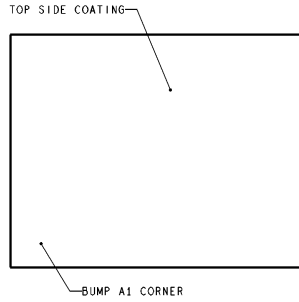
**FIGURE 11. Recommended LD PC Board Layout:  
Bottom Layer**

**Physical Dimensions** inches (millimeters) unless otherwise noted



DIMENSIONS ARE IN MILLIMETERS

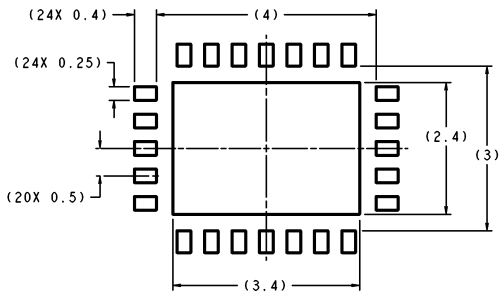
**LAND PATTERN RECOMMENDATION**



BLA18XXX (Rev B)

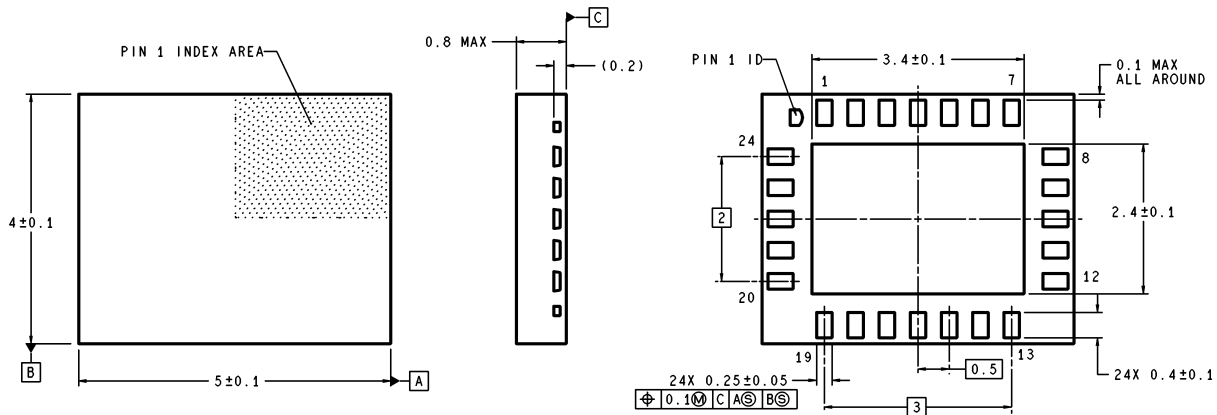
**18-Bump micro SMD**  
**Order Number LM4855IBL**  
**NS Package Number BLA18AAB**  
**Dimensions are in millimeters**  
 $X_1 = 1.996 \pm 0.03$   $X_2 = 2.225 \pm 0.03$   $X_3 = 0.945 \pm 0.01$

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



RECOMMENDED LAND PATTERN  
1:1 RATION WITH PKG SOLDER PADS

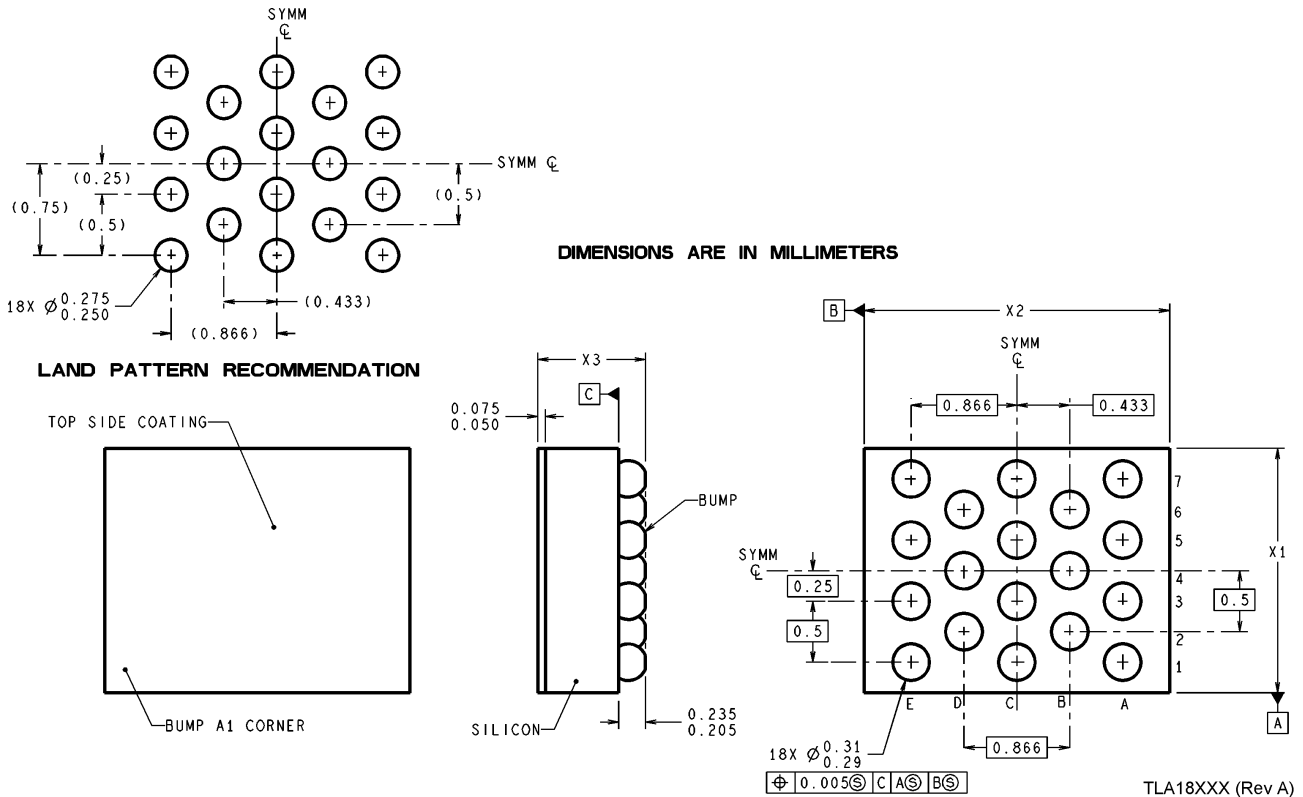
DIMENSIONS ARE IN MILLIMETERS



LQA24A (Rev A)

**24-Lead MOLDED PKG, Leadless Leadframe Package LLP**  
**Order Number LM4855LQ**  
**NS Package Number LQA24A**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**18-Bump micro SMD**  
**Order Number LM4855ITL**  
**NS Package Number TLA18AAA**  
**X<sub>1</sub> = 1.996 X<sub>2</sub> = 2.225 X<sub>3</sub> = 0.600**

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1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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