National Semiconductor

MICROCIRCUIT DATA SHEET

MNLMH6702-X REV 1A0

Original Creation Date: 01/16/04
Last Update Date: 03/08/04
Last Major Revision Date: 01/30/04

Ultra Low Distortion, Current Feedback Widedband OP AMP

General Description

The LMH6702 is a very wideband, DC coupled monolithic operational amplifier designed specifically for wide dynamic range systems requiring exceptional signal fidelity. Benefiting from National's current feedback architecture, the LMH6702 offers a unity gain stability at exceptional speed without need for external compensation.

With its 720MHz bandwidth (Av = 2V/V, Vo = 2Vpp), 10-bit distortion levels through 600MHz (Rl = 100 Ohms), 1.83nV/SqRtHz input referred noise and 12.5mA supply current, the LMH6702 is the ideal driver or buffer for high-speed flash A/D and D/A converters.

Wide dynamic range systems such as radar and communication receivers requiring a wideband amplifier offering exceptional signal purity, will find the LMH6702's low input referred noise and low harmonic and intermodulation distortion make it an attractive high speed solution.

The LMH6702 is constructed using National's VIP10 (TM) complimentary bipolar process and National's proven current feedback architecture.

Industry Part Number

LMH6702

NS Part Numbers

LMH6702J-QML
LMH6702WG-QML

Prime Die

LMH6702

Controlling Document

SEE FEATURES SECTION

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883, Method 5005

Subgrp	Description	Temp (°C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

Features

Vs = ±5V, Ta = 25 Degree C, Av = +2V/V, Rl = 100 Ohms, Vout = 2Vpp, Typical unless Noted:

- -3dB Bandwidth (Vout = 2Vpp) 720MHz
- Low Noise 1.83nV/SqRtHz
- Fast settling to 0.1% 13.4ns
- Fast slew rate 3100V/uS
- Supply current 12.5mA
- Output current 80mA
- Low Intermodulation Distortion (75MHz) -67dBc
- Improved Replacement for CLC409 and CLC449

CONTROLLING DOCUMENTS:

LMH6702J-QML	5962-0254601QPA
LMH6702WG-QML	5962-0254601QZA

Applications

- Flash A/D driver
- D/A transimpedance buffer
- Wide dynamic range IF amp
- Radar/communication receivers
- Line driver
- High resolution video

(Absolute Maximum Ratings)
(Note 1)

Supply Voltage (Vcc)	±6.75Vdc
Common Mode Input Voltage (Vcm)	V- to V+
Power Dissipation (Pd) (Note 2)	1W
Junction Temperature (Tj)	+175 C
Lead Temperature (soldering, 10 seconds)	+300 C
Storage Temperature Range	-65 C ≤ Ta ≤ +150 C
Thermal Resistance	
ThetaJA (Junction to Ambient)	
CERAMIC DIP (Still Air)	170 C/W
(500LF/Min Air Flow)	100 C/W
CERAMIC SOIC (Still Air)	220 C/W
(500LF/Min Air Flow)	150 C/W
ThetaJC (Junction to Case)	
CERAMIC DIP	35 C/W
CERAMIC SOIC	37 C/W
Package Weight (Typical)	
CERAMIC DIP	1078 mg
CERAMIC SOIC	227 mg
ESD Tolerance (Note 3)	1000V

Note 1: Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: The maximum power dissipation must be derated at elevated temperatures and is dictated by Tjmax (maximum junction temperature), ThetaJA (package junction to ambient thermal resistance, and TA (ambient temperature). The maximum allowable power dissipation at any temperature is Pdmax = (Tjmax - TA)/ThetaJA or the number given in the Absolute Maximum Ratings, whichever is lower.

Note 3: Human body model, 1.5K Ohms in series with 100pF.

Recommended Operating Conditions

Supply Voltage (Vcc)	±5Vdc to ±6Vdc
Gain Range	±1 to ±10
Ambient Operating Temperature Range (Ta)	-55 C to +125 C

Electrical Characteristics

DC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Rl - 100 Ohms, Vcc = ±5Vdc, Av = +2 feedback resistor (Rf) = 250 Ohms, gain resistor (Rg) - 250 (NOTE 1)

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Ibn	Input Bias Current, Noninverting				-15	+15	uA	1, 2
					-21	+21	uA	3
Ibi	Input Bias Current, Iverting				-30	+30	uA	1, 2
					-34	+34	uA	3
Vio	Input Offset Voltage				-4.5	+4.5	mV	1, 3
					-6.0	+6.0	mV	2
Icc	Supply Current, no load	Rl = infinity				15	mA	1, 2, 3
PSSR	Power Supply Rejection Ratio	-Vcc = -4.5V to -5.0V, +Vcc = +4.5V to +5.0V			45		dB	1, 2, 3

AC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: Rl - 100 Ohms, Vcc = ±5Vdc, Av = +2 feedback resistor (Rf) = 250 Ohms, gain resistor (Rg) - 250 (NOTE 1)

HD3	3rd Harmonic Distortion	2Vpp at 20MHz				-62	dBc	4
GFPL	Gain Flatness Peaking	0.1MHz to 75MHz, Vout < 0.5Vpp				0.4	dB	4
GFPH	Gain Flatness Peaking	> 75MHz, Vout < 0.5Vpp				2.0	dB	4
GFRH	Gain Flatness Rolloff	75MHz to 125MHz, Vout <0.5Vpp				0.2	dB	4
HD2	2nd Harmonic Distortion	2Vpp at 20MHz				-52	dBc	4

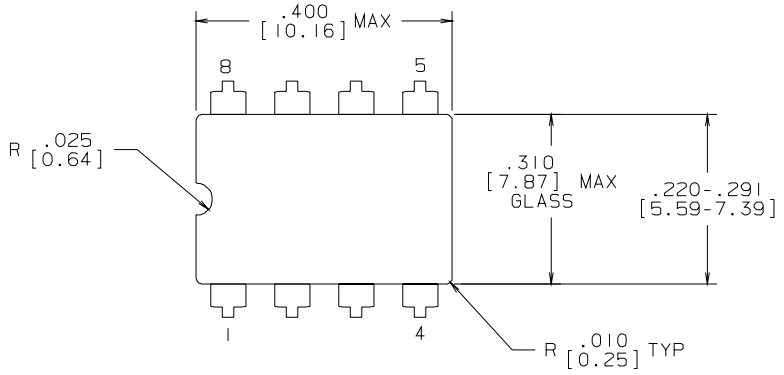
Note 1: The algebraic convention, whereby the most negative value is a minimum and most positive is a maximum, is used in this table. Negative current shall be defined as convential current flow out of a device terminal.

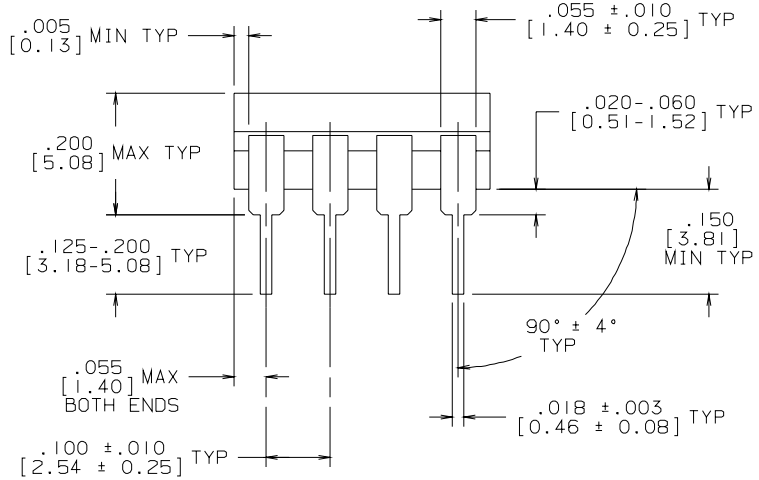
Graphics and Diagrams

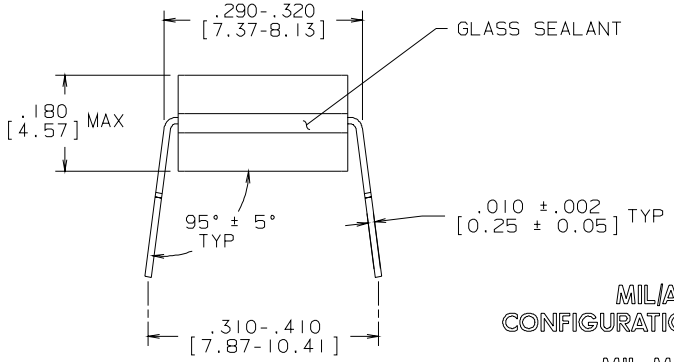
GRAPHICS#	DESCRIPTION
06409HRA3	CERAMIC SOIC (WG), 10 LEAD (B/I CKT)
07077HRA5	CERDIP (J), 8 LEAD (B/I CKT)
J08ARL	CERDIP (J), 8 LEAD (P/P DWG)
P000481A	CERDIP (J), 8 LEAD (PIN OUT)
P000485A	CERAMIC SOIC (WG), 10 LEAD (PIN OUT)
WG10ARC	CERAMIC SOIC (WG), 10 LEAD (P/P DWG)

See attached graphics following this page.

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
L	REVISE PER CURRENT STD; REDRAW	10002	09/21/93	TL/







MIL/AERO
CONFIGURATION CONTROL

MIL-M-38510
CONFIGURATION CONTROL

NOTES: UNLESS OTHERWISE SPECIFIED

1. LEAD FINISH TO BE 200 MICROINCHES / 5.08 MICROMETERS MINIMUM SOLDER MEASURED AT THE CREST OF THE MAJOR FLATS.
2. JEDEC REGISTRATION MO-036, VARIATION AA, DATED 04/1981.

CONTROLLING DIMENSION: INCH

APPROVALS	DATE
DRAWN T. LEQUANG	09/21/93
DFTG. CHK.	
ENGR. CHK.	
APPROVAL	

PROJECTION

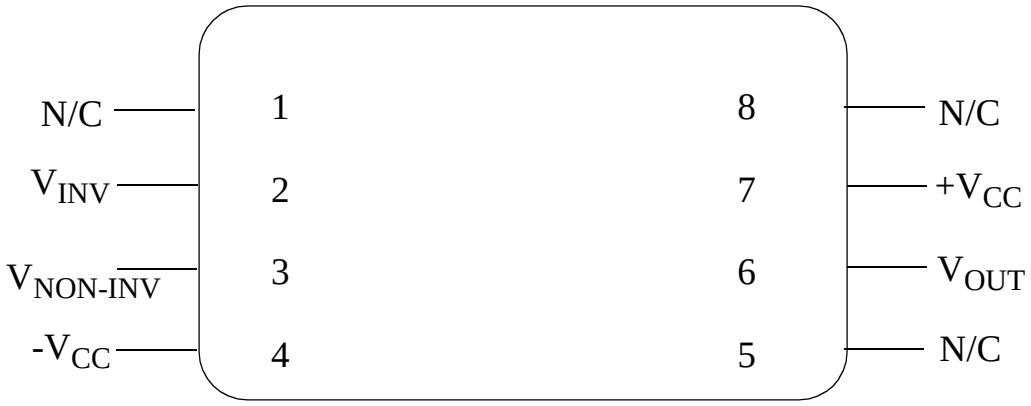
INCH
[MM]

NATIONAL SEMICONDUCTOR CORPORATION
2900 Semiconductor Drive, Santa Clara, CA 95052-8090

CERDIP (J), 8 LEAD

SCALE	SIZE	DRAWING NUMBER	REV
N/A	B	MKT-J08A	L

DO NOT SCALE DRAWING | SHEET 1 OF 1



LMH6702J

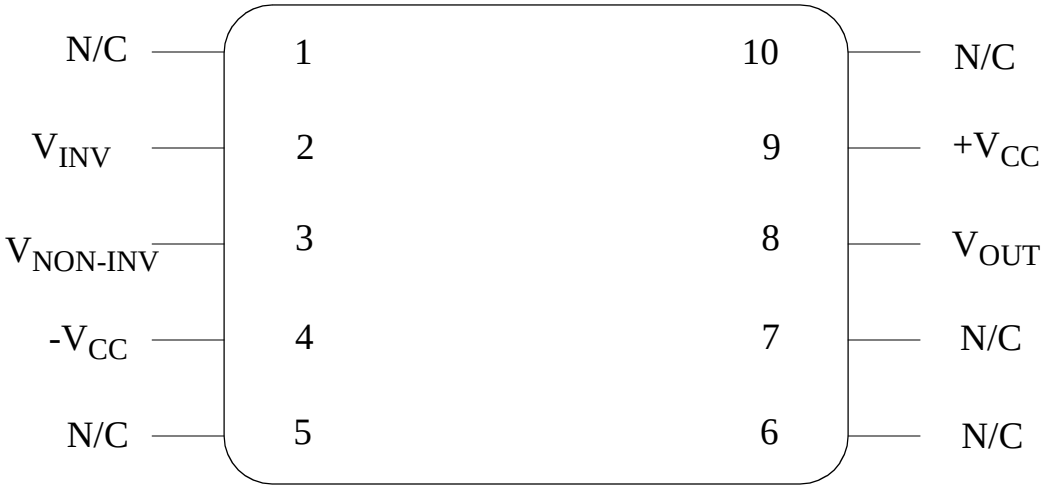
8 - LEAD DIP

CONNECTION DIAGRAM

TOP VIEW

P000481A

National Semiconductor™
MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050



LMH6702WG

10 - LEAD CERAMIC SOIC

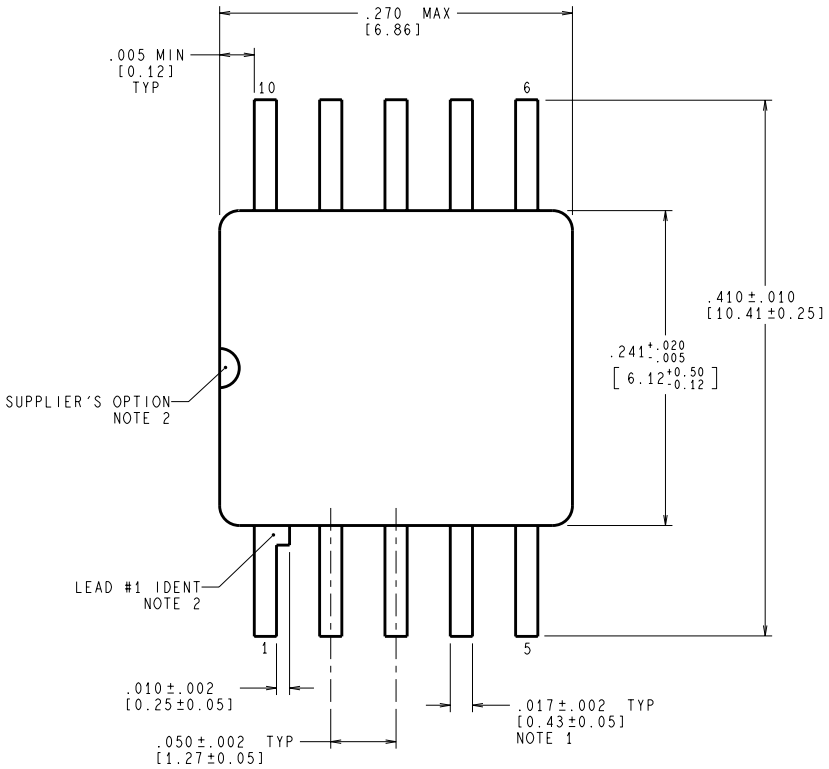
CONNECTION DIAGRAM

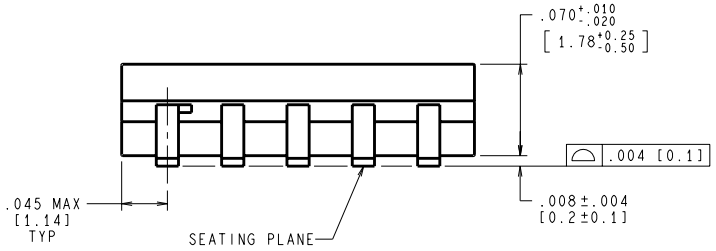
TOP VIEW

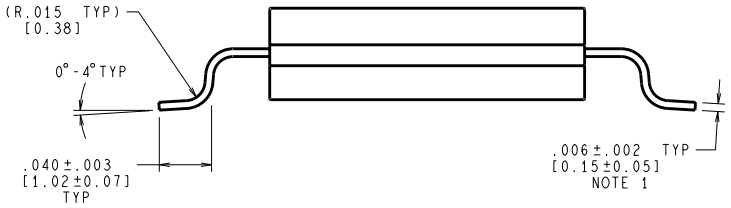
P000485A

National Semiconductor™
MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
A	RELEASE TO DOCUMENT CONTROL	11374	02/29/1996	MS/KH
B	LD PITCH TOL WAS ±.005; CHANGE LD RADIUS TO REF DIM; REMOVE THE OTHER R.006±.002 DIM .040±.003 WAS .037±.003	11441	04/19/1996	MS/KH
C	R .015[0.38] WAS R .006[0.15]	11838	10/08/1997	TL/







NOTES: UNLESS OTHERWISE SPECIFIED

1. LEAD FINISH: SOLDER DIPPED WITH Sn60 OR Sn63 SOLDER CONFORMING TO MIL-PRF-38535 TO A MINIMUM THICKNESS OF 200 MICROINCHES/ 5.08 MICROMETERS. SOLDER MAY BE APPLIED OVER LEAD BASIS METAL OR Sn PLATE. MAXIMUM LIMIT MAY BE INCREASED BY .003 IN/ 0.08mm AFTER LEAD FINISH APPLIED.
2. LEAD 1 IDENTIFICATION SHALL BE:
   a) A NOTCH OR OTHER MARK WITHIN THIS AREA
   b) A TAB ON LEAD 1, EITHER SIDE
3. NO JEDEC REGISTRATION AS OF FEBRUARY 1996.

CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS

MIL-PRF-38535
CONFIGURATION CONTROL

APPROVALS	DATE
DRAWN: MARTA SUCHY	02/29/96
DFTG. CHK.	
ENGR. CHK.	

National Semiconductor
2900 Semiconductor dr, Santa Clara, CA 95052-8090

CERPACK, 10 LEAD, GULL WING

PROJECTION
INCH [MM]

SCALE	SIZE	DRAWING NUMBER	REV
N/A	C	(SC)MKT-WG10A	C

DO NOT SCALE DRAWING | SHEET 1 of 1

Revision History

Rev	ECN #	Rel Date	Originator	Changes
0A0	M0004358	03/08/04	Rose Malone	Initial MDS Release: MNLMH6702-X, Rev. 0A0
1A0	M0004360	03/08/04	Rose Malone	Update MDS: MNLMH6702-X, Rev. 0A0 to MNLMH6702-X, Rev. 1A0. Added reference to Controlling Documents in Features Section. Changed the following Parameter limits on: Ibn, Ibi, Vio, Icc, HD3, GFPH and GFRH.