National Semiconductor

MICROCIRCUIT DATA SHEET

MNLMH6714-X REV 0A0

Original Creation Date: 06/22/04
Last Update Date: 06/25/04
Last Major Revision Date:

SINGLE WIDEBAND VIDEO OP AMP

General Description

The LMH6714 is built on National's VIP10 (TM) high speed complementary bipolar process combined with National's current feedback topology to produce a very high speed op amp. This amplifier provides a 400MHz small signal bandwidth at a gain of +2V/V and a 1800V/uS slew rate while consuming only 5.6mA from ±5V supplies.

The LMH6714 offers exceptional video performance with its 0.01% and 0.01 degree differential gain and phase errors for NTSC and PAL video signals while driving a back terminated 75 Ohms load. It also offers a flat gain response of 0.1dB to 120MHz. Additionally, it can deliver 70mA continuous output current. This level of performance makes it an ideal op amp for broadcast quality video systems.

The LMH6714 low power requirement, low noise and distortion allows the LMH6714 to serve portable RF applications.

Industry Part Number

LMH6714A

NS Part Numbers

LMH6714J-QML
LMH6714WG-QML

Prime Die

LMH6714A

Controlling Document

SEE FEATURES SECTION

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883, Method 5005

Subgrp	Description	Temp (°C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

Features

- 400MHz (Av = +2V/V, Vout = 500mVpp) -3dB Bw
- 250MHz (Av = +2V/V, Vout = 2Vpp) -3dB Bw
- 0.1dB gain flatness to 120MHz
- Low power: 5.6mA
- Very Low Diff. Gain, Phase: 0.01%, 0.01 deg.
- -58 HD2/ -70 HD3 at 20MHz
- Fast slew rate: 1800V/uS
- Unity gain stable
- Improved replacement for CLC400, 401, 402, 404, 406 and 446

CONTROLLING DOCUMENTS:

LMH6714J-QML	5962-0420201QPA
LMH6714WG-QML	5962-0420201QZA

Applications

- NTSC & PAL video systems
- Wideband active filters
- Cable drivers
- High speed multiplexer
- Programmable gain amplifier

(Absolute Maximum Ratings)
(Note 1)

Vcc	±6.75Vdc
Iout (Note 3)	See Note 3
Common Mode Input Voltage	±Vcc
Differential Input Voltage	2.2V
Maximum Junction Temperature (Note 2)	+150 C
Lead temperature (soldering, 10 seconds)	+300 C
Storage Temperature Range	-65 C ≤ Ta ≤ +150 C
Thermal Resistance	
ThetaJA Junction-to-ambient	
Ceramic SOIC	
(Still Air)	220 C/W
(500LF/Min Air Flow)	160 C/W
Ceramic Dip	
(Still Air)	165 C/W
(500LF/Min Air Flow)	105 C/W
ThetaJC Junction-to-case	
Ceramic SOIC	38 C/W
Ceramic Dip	30 C/W
Package Weight (typical)	
Ceramic SOIC	220mg
Ceramic Dip	953mg
ESD Tolerance (Note 4)	4000V

Note 1: Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: The maximum power dissipation must be derated at elevated temperatures and is dictated by Tjmax (maximum junction temperature), ThetaJA (package junction to ambient thermal resistance), and TA (ambient temperature). The maximum allowable power dissipation at any temperature is Pdmax = (Tjmax - TA) / ThetaJA or the number given in the Absolute Maximum Ratings, whichever is lower.

Note 3: The maximum output current (Iout) is determined by device power dissipation limitations.

Note 4: Human body model, 100pF discharged through 1.5K Ohms.

Recommended Operating Conditions

Operating Temperature Range (Ta)	-55 C to +125 C
Nominal Supply voltage (Vs)	±5V to ±6V

Electrical Characteristics

AC/DC PARAMETERS:

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Av = +6, Rf = 500 Ohm, Vcc = ±5V, Rl = 100 Ohms, Rg (Gain resistor) = 100 Ohms, -55 C ≤ Ta ≤ +125 C (NOTE 1)

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Ibn	Input bias current noninverting				-10	10	uA	1
					-15	15	uA	2, 3
Ibi	Input Bias Current Inverting				-12	12	uA	1
					-20	20	uA	2, 3
Vio	Input offset voltage				-6	6	mV	1
					-10	10	mV	2, 3
Icc	Supply Current					7.5	mA	1
						8	mA	2, 3
PSRR	Power supply rejection ratio	-Vcc = - 4.5V to -5.0V, +Vcc = +4.5V to +5.0V			48		dB	1, 2, 3
+Vo	Output Voltage Range				2.7		V	1, 2, 3
-Vo	Output Voltage range					-2.7	V	1, 2, 3
SSBW	Small signal bandwidth	-3 dB bandwidth, Vout <2 Vpp			105		MHz	4
GFPL	Gain flatness peaking	0.1MHz to 25MHz, Vout <2 Vpp				0.2	dB	4
GFPH	Gain flatness peaking	>25MHz, Vout <2 Vpp				0.5	dB	4
GFR	Gain flatness rolloff	0.1MHz to 50MHz, Vout <2 Vpp				1	dB	4
HD2	2nd harmonic distortion	2 Vpp at 20 MHz				-46	dBc	4
HD3	3rd harmonic distortion	2 Vpp at 20 MHz				-50	dBc	4

Note 1: The algebraic convention whereby the most negative value is a minimum, and the most positive a maximum, is used in this table. Negative current shall be defined as conventional current flow out of a device terminal.

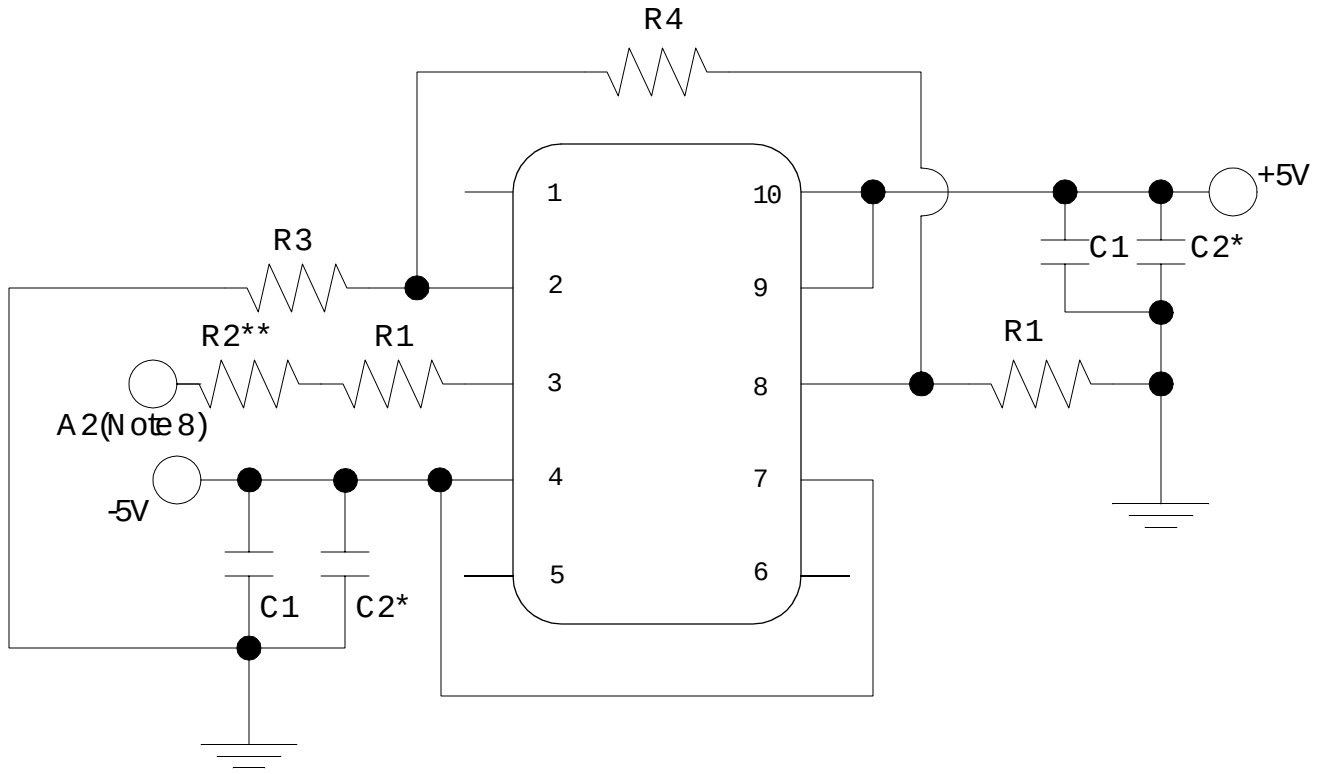
Graphics and Diagrams

GRAPHICS#	DESCRIPTION
06409HRA3	CERAMIC SOIC (WG), 10 LEAD (B/I CKT)
07077HRA5	CERDIP (J), 8 LEAD (B/I CKT)
J08ARL	CERDIP (J), 8 LEAD (P/P DWG)
P000492A	CERDIP (J), 8 LEAD (PIN OUT)
P000493A	CERPACK (WG), 10 LEAD (PIN OUT)
WG10ARC	CERPACK (WG), 10 LEAD (P/P DWG)

See attached graphics following this page.

GENERAL NOTES:
1. GENERIC - INDUSTRY TYPE DEVICES THAT MAY BE USED WITH THIS CIRCUIT SHALL BE AS SPECIFIED IN NSC BURN-IN CIRCUIT LIST R512B-04.
2. ALL 1/4 AND 1/2 WATT RESISTORS SHALL BE METAL FILM. ALL 1, 2, AND 3 WATT RESISTORS SHALL BE WIREWOUND. TOLERANCE SHALL BE +/-5% UNLESS OTHERWISE SPECIFIED.
3. ALL VOLTAGES SPECIFIED SHALL BE MEASURED AT THE "DEVICE UNDER TEST" PIN AND SHALL BE MINIMUM VALUES UNLESS OTHERWISE SPECIFIED.
4. WHEN APPLICABLE, CLOCK PULSES SPECIFIED SHALL HAVE 50% DUTY CYCLE.
5. THIS DRAWING COMPLIES WITH MIL-PRF-38535, WHEN APPLICABLE.

ECN	REV	APPROVALS	DATE
001467	A1	TTrinh	06/23/03
001548	A2	TTrinh	09/09/03
001560	A3	TTrinh	09/18/03



DUT CONDITIONS

	LIMITS MIN.	LIMITS MAX.	UNITS	SYMBOL	LIMITS MIN.	LIMITS MAX.	UNITS
+5V	+4.75	+5.25	VOLTS	A2	50	100	KHz
-5V	-5.25	-4.75	VOLTS	VIL	-0.6	-0.5	VOLTS
				VIH	+0.5	+0.6	VOLTS

NOTES:
6. DFC PIN 8.
7. *One pc per column for each supply.
8. A2 may be called as Vin
9. ** One PC per Row.
10. LMH6702/6714/6720

COMPONENT REQUIREMENTS PER POSITION

DESIG.	QTY	DESCRIPTION
R1	2	100 OHMS, 1/4 Watt, 1%
R2	1**	50 OHMS, 1/2 Watt, 1%
R3	1	500 OHMS, 1/4 Watt, 1%
R4	1	2K OHMS, 1/4 Watt, 1%
C1	2	0.1uF, X7R, 50V
C2	2*	10uF, 50V (Note 7)

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MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050

BURN-IN CIRCUIT

SH 1 OF 1

CUSTOMER	PACKAGE TYPE	MIL	NSC	TEST CONDITION
	W/WG010		Note 10	D

ORIGINATOR	DATE	CHECKED BY	DATE	DRAWING NUMBER	REV
T.Trinh	9/18/03			06409HR	A3

GENERAL NOTES:
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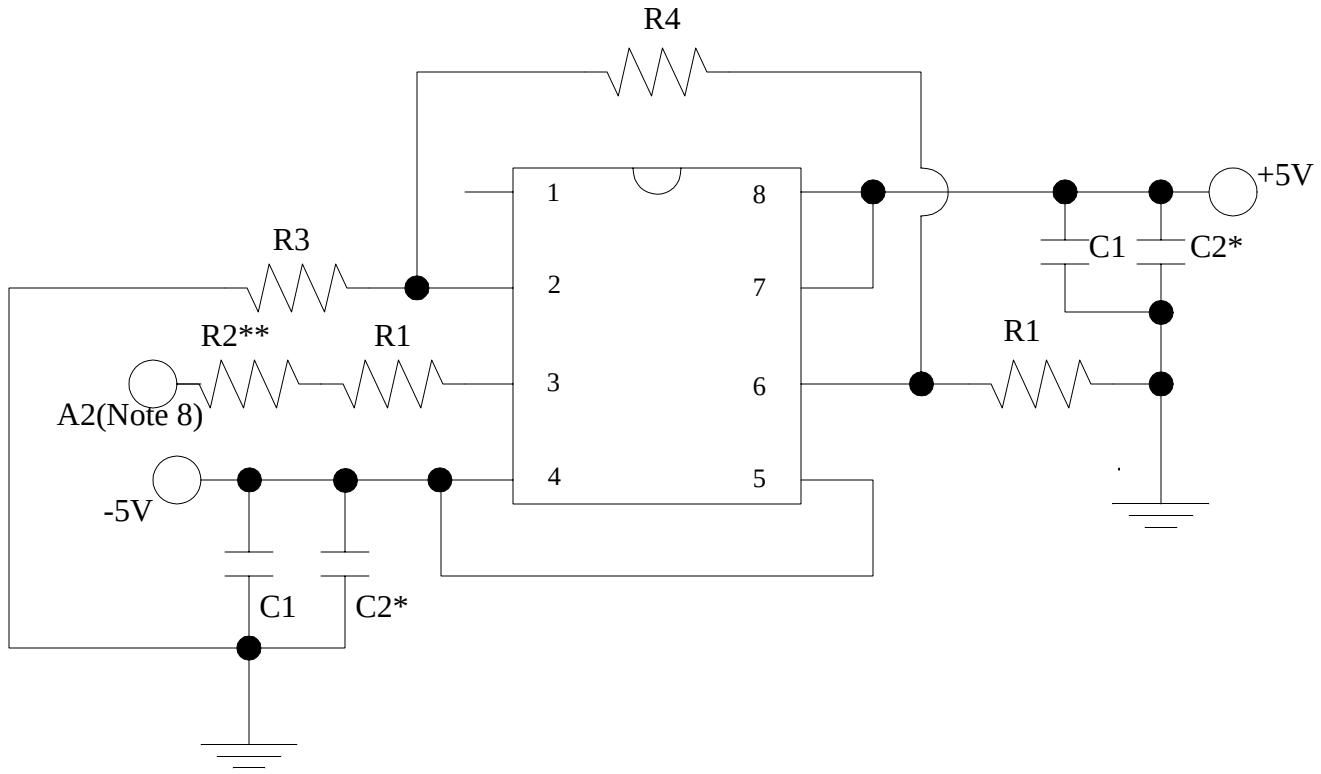
2. ALL 1/4 AND 1/2 WATT RESISTORS SHALL BE METAL FILM. ALL 1, 2, AND 3 WATT RESISTORS SHALL BE WIRE WOUND. TOLERANCE SHALL BE +/-5% UNLESS OTHERWISE SPECIFIED.
3. ALL VOLTAGES SPECIFIED SHALL BE MEASURED AT THE "DEVICE UNDER TEST" PIN AND SHALL BE MINIMUM VALUES UNLESS OTHERWISE SPECIFIED.
4. WHEN APPLICABLE, CLOCK PULSES SPECIFIED SHALL HAVE 50% DUTY CYCLE.
5. THIS DRAWING COMPLIES WITH MIL-PRF-38535, WHEN APPLICABLE.

ECN	REV	APPROVALS	DATE
07394	A1	LH Chong	12/16/97
07666	A2	J.Gomez	08/07/98
001121	A3	T. TRINH	06/21/02
001547	A4	T. TRINH	09/09/03
001561	A5	T. TRINH	09/18/03



DUT CONDITIONS

SYMBOL	LIMITS MIN.	LIMITS MAX.	UNITS	SYMBOL	LIMITS MIN.	LIMITS MAX.	UNITS
+5V	+4.75	+5.25	VOLTS	A2	50	100	KHz
-5V	-5.25	-4.75	VOLTS	V_{IL}	-0.6	-0.5	VOLTS
				V_{IH}	+0.5	+0.6	VOLTS

NOTES:
6. DFC PIN 6.
7. *One pc per column for each supply.
8. A2 may be called as Vin
9. T_{JMAX} @ 125°C is 155°C.
10. NSPNs are CLC409/ LMH6702 LMH6714/MH6720
11. ** One PC per Row

COMPONENT REQUIREMENTS PER POSITION

REF	QTY	DESCRIPTION
R1	2	100 Ω, 1/4 Watt, 1%
R2	1**	50 Ω, 1/2 Watt, 1%
R3	1	500 Ω, 1/4 Watt, 1%
R4	1	2 KΩ, 1/4 Watt, 1%
C1	2	0.1 uF, X7R, 50V
C2	2*	10 uF, 50V (Note 7)

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2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050

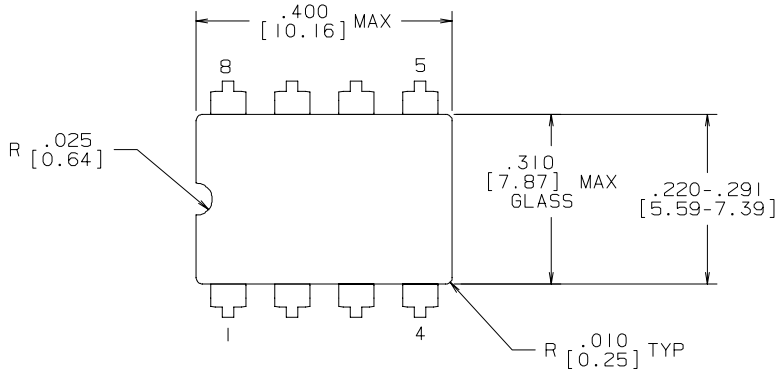
BURN-IN CIRCUIT

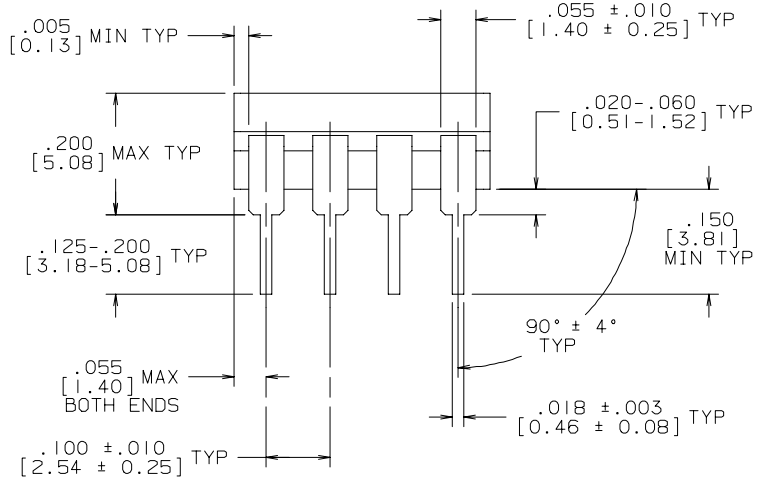
SH	OF
1	1

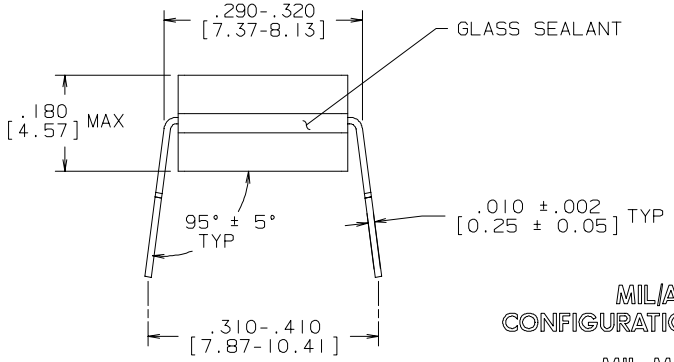
CUSTOMER	PACKAGE TYPE	MIL	NSC	TEST CONDITION
	J008		Note 10	D

ORIGINATOR	DATE	CHECKED BY	DATE	DRAWING NUMBER	REV
T.Trinh	9/18/03			07077HR	A5

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
L	REVISE PER CURRENT STD; REDRAW	I0002	09/21/93	TL/







MIL/AERO
CONFIGURATION CONTROL

MIL-M-38510
CONFIGURATION CONTROL

NOTES: UNLESS OTHERWISE SPECIFIED

1. LEAD FINISH TO BE 200 MICROINCHES / 5.08 MICROMETERS MINIMUM SOLDER MEASURED AT THE CREST OF THE MAJOR FLATS.
2. JEDEC REGISTRATION MO-036, VARIATION AA, DATED 04/1981.

CONTROLLING DIMENSION: INCH

APPROVALS	DATE
DRAWN T. LEQUANG	09/21/93
DFTG. CHK.	
ENGR. CHK.	
APPROVAL	

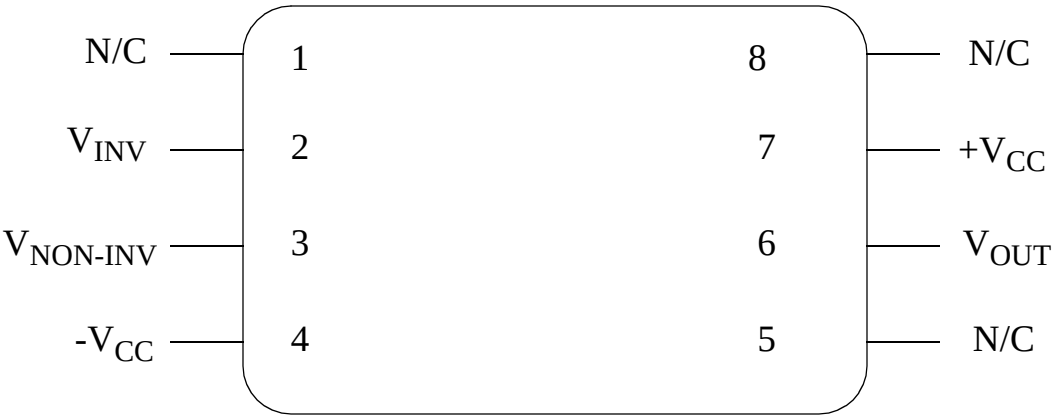
PROJECTION
INCH
[MM]

NATIONAL SEMICONDUCTOR CORPORATION
2900 Semiconductor Drive, Santa Clara, CA 95052-8090

CERDIP (J), 8 LEAD

SCALE	SIZE	DRAWING NUMBER	REV
N/A	B	MKT-J08A	L

DO NOT SCALE DRAWING | SHEET 1 OF 1



LMH6714J

8 - LEAD CER DIP

CONNECTION DIAGRAM

TOP VIEW

P000492A

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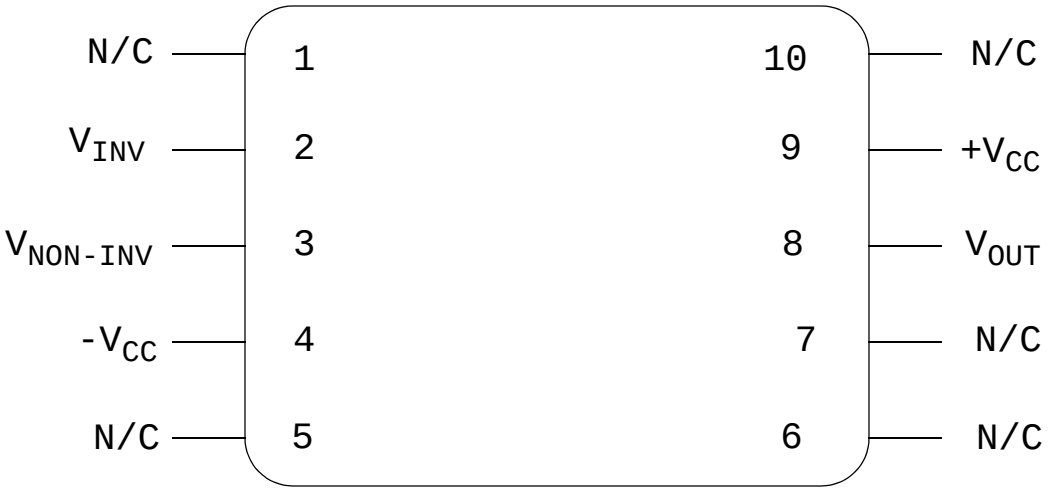
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050



LMH6714W/WG

10 - LEAD FLAT PACK/SOIC

CONNECTION DIAGRAM

TOP VIEW

P000493A

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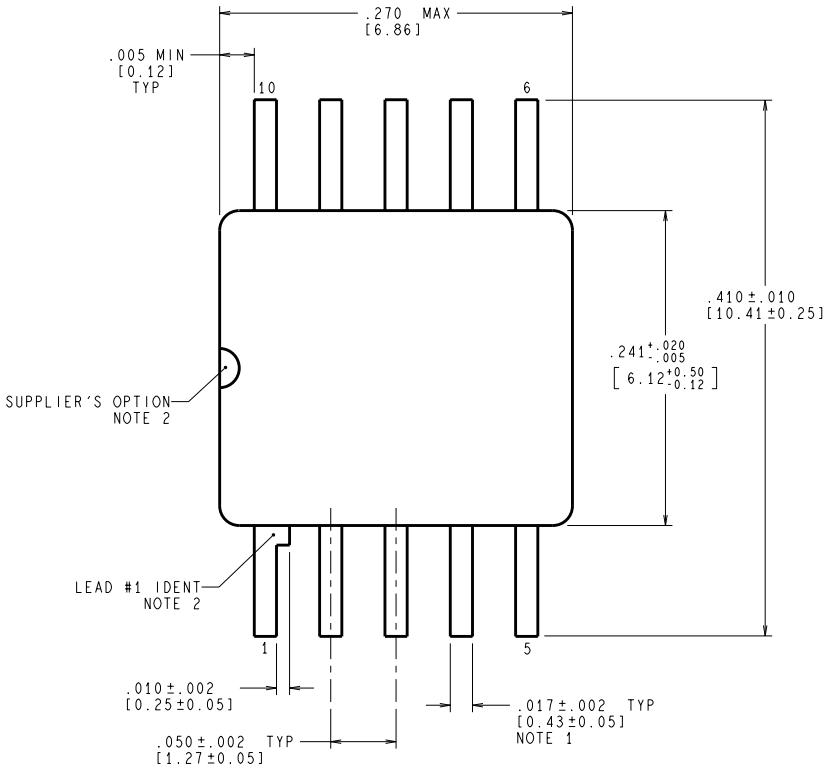
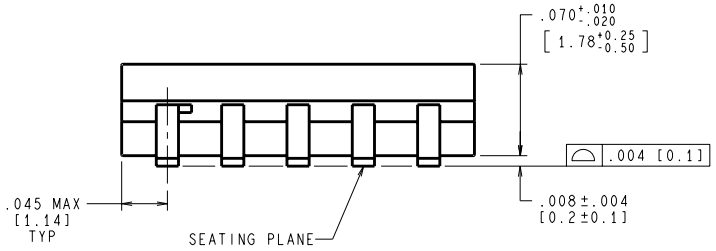
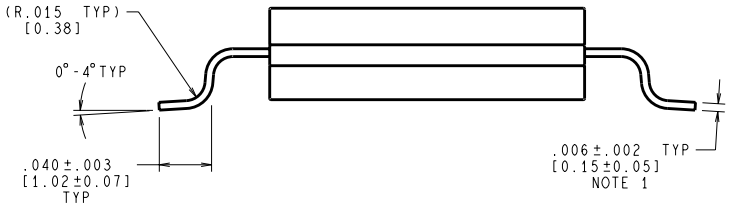
MIL/AEROSPACE OPERATIONS
SEMICONDUCTOR
SANTA CLARA, CA

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
A	RELEASE TO DOCUMENT CONTROL	11374	02/29/1996	MS/KH
B	LD PITCH TOL WAS ±.005; CHANGE LD RADIUS TO REF DIM; REMOVE THE OTHER R.006±.002 DIM .040±.003 WAS .037±.003	11441	04/19/1996	MS/KH
C	R .015[0.38] WAS R .006[0.15]	11838	10/08/1997	TL/







NOTES: UNLESS OTHERWISE SPECIFIED

1. LEAD FINISH: SOLDER DIPPED WITH Sn60 OR Sn63 SOLDER CONFORMING TO MIL-PRF-38535 TO A MINIMUM THICKNESS OF 200 MICROINCHES/ 5.08 MICROMETERS. SOLDER MAY BE APPLIED OVER LEAD BASIS METAL OR Sn PLATE. MAXIMUM LIMIT MAY BE INCREASED BY .003 IN/ 0.08mm AFTER LEAD FINISH APPLIED.
2. LEAD 1 IDENTIFICATION SHALL BE:
   a) A NOTCH OR OTHER MARK WITHIN THIS AREA
   b) A TAB ON LEAD 1, EITHER SIDE
3. NO JEDEC REGISTRATION AS OF FEBRUARY 1996.

CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS

MIL-PRF-38535
CONFIGURATION CONTROL

APPROVALS	DATE
DRAWN: MARTA SUCHY	02/29/96
DFTG. CHK.	
ENGR. CHK.	

National Semiconductor
2900 Semiconductor dr, Santa Clara, CA 95052-8090

CERPACK, 10 LEAD, GULL WING

PROJECTION
INCH [MM]

SCALE	SIZE	DRAWING NUMBER	REV
N/A	C	(SC)MKT-WG10A	C

DO NOT SCALE DRAWING | SHEET 1 of 1

Revision History

Rev	ECN #	Rel Date	Originator	Changes
0A0	M0004395	06/25/04	Rose Malone	Initial MDS Release: MNLMH6714-X, Rev. 0A0