National Semiconductor

MICROCIRCUIT DATA SHEET

MNLMH6720-X REV 0A0

Original Creation Date: 03/17/04
Last Update Date: 03/24/04
Last Major Revision Date:

LMH6720 WIDEBAND VIDEO OP AMP; SINGLE WITH SHUT DOWN

General Description

The LMH6720 series combine National's VIP10 (TM) high speed complementary bipolar process with National's current feedback topology to produce a very high speed op amp. These amplifiers provide a 400MHz small signal bandwidth at a gain of +2V/V and a 1800V/uS slew rate while consuming only 5.6mA from ±5V supplies.

The LMH6720 offers exceptional video performance with its 0.01% and 0.01 differential gain and phase errors for NTSC and PAL video signals while driving a back terminated 75 Ohms load. They also offer a flat gain respose of 0.1dB to 120MHz. Additionally, they can deliver 70mA continuous output current. This level of performance makes them an ideal op amp for broadcast quality video systems.

The LMH6720 low power requirement, low noise and distortion allow the LMH6720 to serve portable RF applications. The high impedance state during shutdown makes the LMH6720 suitable for use in multiplexing multiple high speed signals onto a shared transmission line. The LMH6720 is also ideal for portable applications where current draw can be reduced with the shutdown function.

Industry Part Number

LMH6720

NS Part Numbers

LMH6720J-QML
LMH6720WG-QML

Prime Die

LMH6720

Controlling Document

SEE FEATURES SECTION

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883, Method 5005

Subgrp	Description	Temp (^{O}C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

Features

- 400MHz (Av = +2V/V, Vout = 500mVpp) -3dB Bw
- 250MHz (Av = +2V/V, Vout = 2Vpp) -3dB Bw
- 0.1dB gain flatness to 120MHz
- Low power: 5.6mA
- TTL compatible shutdown pin
- -58 HD2/ -70 HD3 at 10MHz
- Fast slew rate: 1800V/uS
- Low shutdown current: 500uA
- 11nS turn on time
- 7nS shutdown time
- Unity gain stable
- Improved replacement for CLC405

CONTROLLING DOCUMENTS:

LMH6720J-QML	5962-0420301QPA
LMH6720WG-QML	5962-0420301QZA

Applications

- HDTV, NTSC & PAL video systems
- Wideband active filters
- Cable drivers
- High speed multiplexer
- Programmable gain amplifier

(Absolute Maximum Ratings)
(Note 1)

Vcc	±6.75Vdc
Iout (Note 3)	See Note 3
Common Mode Input Voltage	±Vcc
Differential Input Voltage	2.2V
Maximum Junction Temperature (Note 2)	+150 C
Lead temperature (soldering, 10 seconds)	+300 C
Storage Temperature Range	-65 C ≤ Ta ≤ +150 C
Shutdown Pin Voltage (Note 4)	+Vcc to Vcc/2-1V
Thermal Resistance	
ThetaJA (Junction to Ambient)	
CERAMIC DIP (Still Air)	170 C/W
(500LF/Min Air Flow)	105 C/W
CERAMIC SOIC (Still Air)	230 C/W
(500LF/Min Air Flow)	170 C/W
ThetaJC	
CERAMIC DIP	30 C/W
CERAMIC SOIC	40 C/W
Package Weight (typical)	
CERAMIC DIP	1090mg
CERAMIC SOIC	220mg
ESD Tolerance (Note 5)	4000V

Note 1: Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: The maximum power dissipation must be derated at elevated temperatures and is dictated by Tjmax (maximum junction temperature), ThetaJA (package junction to ambient thermal resistance), and TA (ambient temperature). The maximum allowable power dissipation at any temperature is Pdmax = (Tjmax - TA) / ThetaJA or the number given in the Absolute Maximum Ratings, whichever is lower.

Note 3: The maximum output current (Iout) is determined by device power dissipation limitations.

Note 4: The shutdown pin is designed to work between 0 and Vcc with split supplies (Vcc = -Vee). With single supplies (Vee = ground) the shutdown pin should not be taken below Vcc/2.

Note 5: Human body model, 100pF discharged through 1.5K Ohms.

Recommended Operating Conditions

Operating Temperature Range (Ta)	-55 C ≤ Ta ≤ +125 C
Nominal Supply voltage (Vs)	±5V to ±6V

Electrical Characteristics

DC PARAMETERS:

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Av = +2, Rf = 348 Ohm, Vcc = ±5V, R load = 100 Ohms, -55 C < = Ta <= +125 C (NOTE 1)

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Vio	Input Offset Voltage				-6	+6	mV	1
					-10	+10	mV	2, 3
Ibn	Input Bias Current	Non-Inverting			-10	+10	uA	1
					-15	+15	uA	2, 3
Ibi	Input Bias Current	Inverting			-12	+12	uA	1
					-20	+20	uA	2, 3
PSRR	Power Supply Rejection Ratio	DC			48		dB	1
					47		dB	2, 3
Icc Pos	Supply Current	R load = infinity			3.0	7.5	mA	1
					3.0	8.0	mA	2, 3
Icc Neg	Supply Current	R load = infinity			-7.5	-3	mA	1
					-8	-3	mA	2, 3
IccD	Supply Current During Shutdown					0.67	mA	1
						1	mA	2, 3

AC PARAMETERS: Frequency Domain Response

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: Av = +2, Rf = 348 Ohm, Vcc = ±5V, R load = 100 Ohms, -55 C < = Ta <= +125 C (NOTE 1)

SSBW	Small Signal Bandwith	-3dB bandwidth, Vout < 1. 0 Vpp			345		MHz	4
GFRH	Gain Flatness Rolloff	0.1 MHz to 30 MHz				0.3	dB	4

AC PARAMETERS: Distortion and Noise Test

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: Av = +2, Rf = 348 Ohm, Vcc = ±5V, R load = 100 Ohms, -55 C < = Ta <= +125 C (NOTE 1)

HD2	2nd Harmonic Distortion	2Vpp at 10 MHz, Vout = 2Vpp			46		dB	4
HD3	3rd Harmonic Distortion	2Vpp at 10 MHz, Vout = 2Vpp			50		dB	4

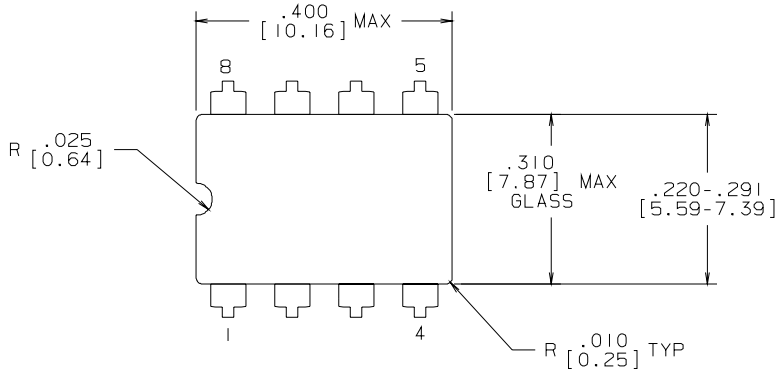
Note 1: The algebraic convention, whereby the most negative value is a minimum and the most positive is a maximum, is used in this table. Negative current shall be defined as conventional current flow out of a device terminal.

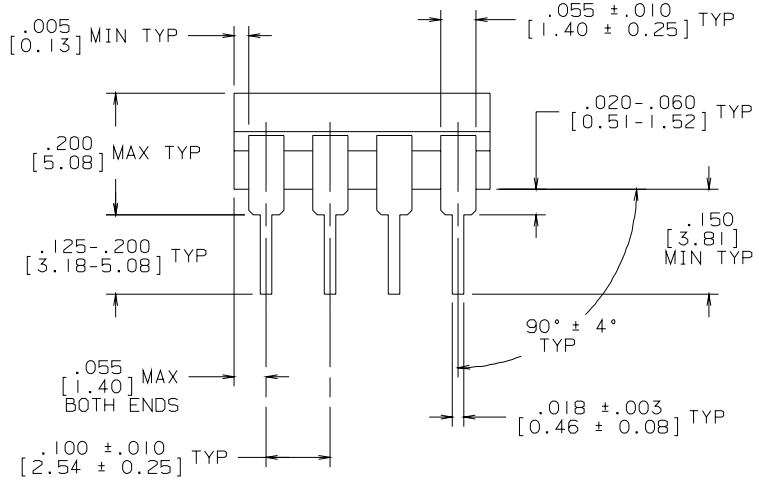
Graphics and Diagrams

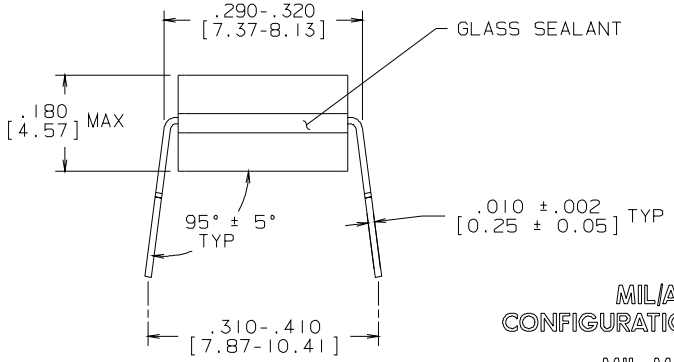
GRAPHICS#	DESCRIPTION
06409HRA3	CERAMIC SOIC (WG), 10 LEAD (B/I CKT)
07077HRA6	CERDIP (J), 8 LEAD (B/I CKT)
J08ARL	CERDIP (J), 8 LEAD (P/P DWG)
P000490A	CERDIP (J), 8 LEAD (PIN OUT)
P000491A	CERAMIC SOIC (WG), 10 LEAD (PIN OUT)
WG10ARC	CERPACK (WG), 10 LEAD (P/P DWG)

See attached graphics following this page.

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
L	REVISE PER CURRENT STD; REDRAW	10002	09/21/93	TL/







MIL/AERO
CONFIGURATION CONTROL

MIL-M-38510
CONFIGURATION CONTROL

NOTES: UNLESS OTHERWISE SPECIFIED

1. LEAD FINISH TO BE 200 MICROINCHES / 5.08 MICROMETERS MINIMUM SOLDER MEASURED AT THE CREST OF THE MAJOR FLATS.
2. JEDEC REGISTRATION MO-036, VARIATION AA, DATED 04/1981.

CONTROLLING DIMENSION: INCH

APPROVALS	DATE
DRAWN T. LEQUANG	09/21/93
DFTG. CHK.	
ENGR. CHK.	
APPROVAL	

PROJECTION

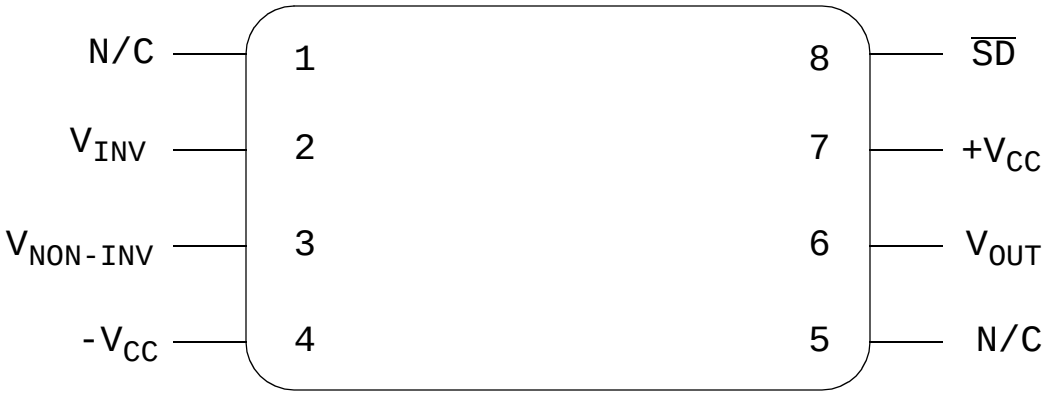
INCH
[MM]

NATIONAL SEMICONDUCTOR CORPORATION
2900 Semiconductor Drive, Santa Clara, CA 95052-8090

CERDIP (J), 8 LEAD

SCALE	SIZE	DRAWING NUMBER	REV
N/A	B	MKT-J08A	L

DO NOT SCALE DRAWING | SHEET 1 OF 1



LMH6720J

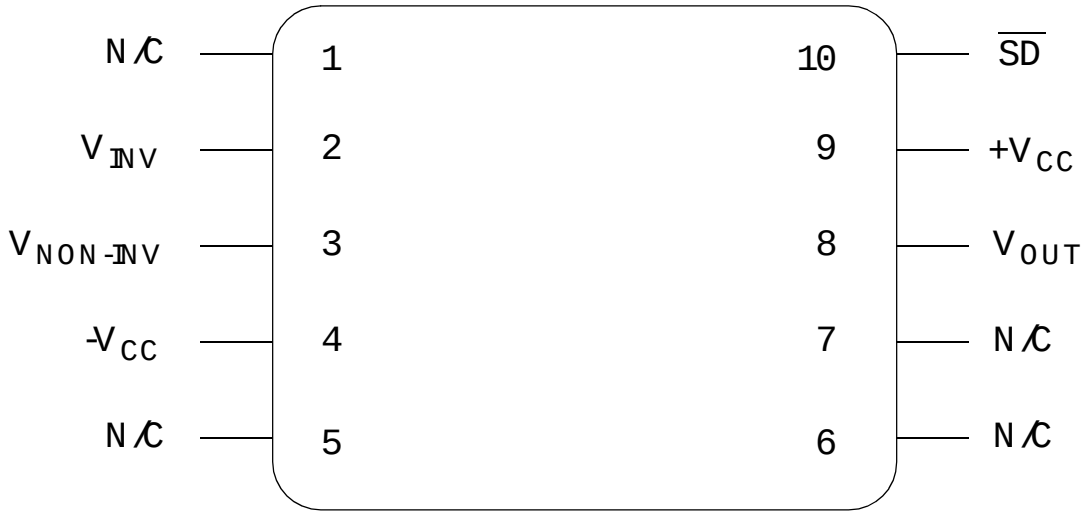
8 - LEAD CER-DIP

CONNECTION DIAGRAM

TOP VIEW

P000490A

National Semiconductor
MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050



LMH6720W/WG

10 - LEAD FLAT PACK/SOIC

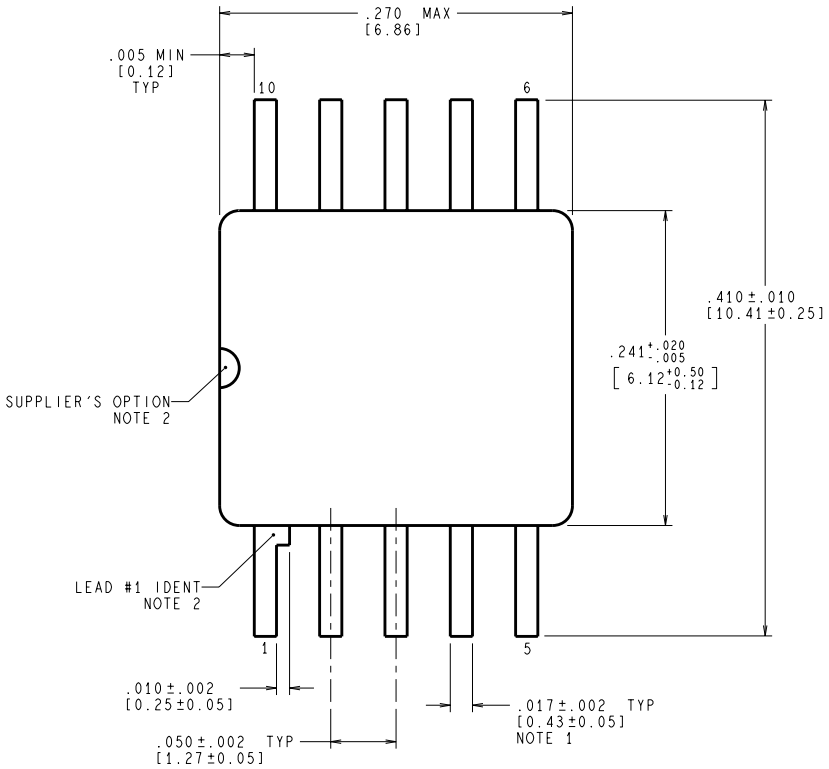
CONNECTION DIAGRAM

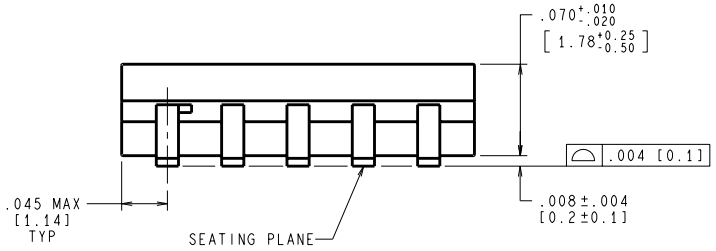
TOP VIEW

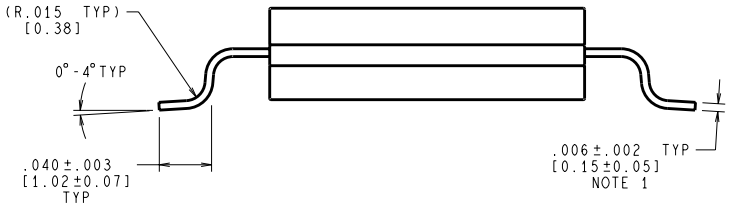
P000491A

National Semiconductor
MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
A	RELEASE TO DOCUMENT CONTROL	11374	02/29/1996	MS/KH
B	LD PITCH TOL WAS ±.005; CHANGE LD RADIUS TO REF DIM; REMOVE THE OTHER R.006±.002 DIM .040±.003 WAS .037±.003	11441	04/19/1996	MS/KH
C	R .015[0.38] WAS R .006[0.15]	11838	10/08/1997	TL/







NOTES: UNLESS OTHERWISE SPECIFIED

1. LEAD FINISH: SOLDER DIPPED WITH Sn60 OR Sn63 SOLDER CONFORMING TO MIL-PRF-38535 TO A MINIMUM THICKNESS OF 200 MICROINCHES/ 5.08 MICROMETERS. SOLDER MAY BE APPLIED OVER LEAD BASIS METAL OR Sn PLATE. MAXIMUM LIMIT MAY BE INCREASED BY .003 IN/ 0.08mm AFTER LEAD FINISH APPLIED.
2. LEAD 1 IDENTIFICATION SHALL BE:
   a) A NOTCH OR OTHER MARK WITHIN THIS AREA
   b) A TAB ON LEAD 1, EITHER SIDE
3. NO JEDEC REGISTRATION AS OF FEBRUARY 1996.

CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS

MIL-PRF-38535
CONFIGURATION CONTROL

APPROVALS	DATE
DRAWN: MARTA SUCHY	02/29/96
DFTG. CHK.	
ENGR. CHK.	

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CERPACK, 10 LEAD, GULL WING

PROJECTION
INCH [MM]

SCALE	SIZE	DRAWING NUMBER	REV
N/A	C	(SC)MKT-WG10A	C

DO NOT SCALE DRAWING | SHEET 1 of 1