MICROCIRCUIT DATA SHEET

MNLMH6722-X REV 1A0

Original Creation Date: 01/08/04
Last Update Date: 02/24/04
Last Major Revision Date: 02/20/04

Quad, Current Feedback, Wideband Video OP AMP

General Description

The LMH6722 series combine National's VIP10 (TM) high speed complementary bipolar process with National's current feedback topology to produce a very high speed op amp. These amplifiers provide a 400MHz small signal bandwidth at a gain of +2V/V and a 1800V/uS slew rate while consuming only 5.6mA from ±5V supplies.

The LMH6722 series offer exceptional video performance with its 0.01% and 0.01deg differential gain and phase errors for NTSC and PAL video signals while driving a back terminated 75 Ohm load. They also offer a flat gain response of 0.1dB to 120MHz. Additionally, they can deliver 70mA continuous output current. This level of performance makes them an ideal op amp for broadcast quality video systems.

Industry Part Number

LMH6722

NS Part Numbers

LMH6722J-QML
LMH6722WG-QML

Prime Die

LMH6722

Controlling Document

SEE FEATURES SECTION

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883, Method 5005

Subgrp	Description	Temp (°C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

Features

- 400MHz (Av = +2V/V, Vout = 500mVpp) -3dB Bw
- 250MHz (Av = +2V/V, Vout = 2Vpp) -3dB Bw
- 0.1dB gain flatness to 120MHz
- Low power: 5.6mA per Op Amp
- -58dbc HD2/ -70dbc HD3 at 20MHz
- Fast slew rate: 1800V/uS
- Unity gain stable
- Improved replacement for CLC415 (LMH6722)

CONTROLLING DOCUMENTS:

LMH6722J-QML	5962-0324901QCA
LMH6722WG-QML	5962-0324901QZA

Applications

- HDTV, NTSC & PAL video systems
- Wideband active filters
- Cable drivers

(Absolute Maximum Ratings)
(Note 1)

Supply voltage (Vs)	±6.75Vdc
Common mode input voltage (Vcm)	V- to V+
Differential input voltage (Vid)	2.2V
Maximum Power dissipation (Pd) (Note 2)	1W
Lead temperature (soldering, 10 seconds)	+300 C
Junction temperature (Tj)	+175 C
Storage temperature range	-65 C ≤ Ta ≤ +150 C
Thermal Resistance	
(ThetaJA) Junction -to-ambient	
CERAMIC DIP (Still Air)	130 C/W
(500LF/Min Air Flow)	83 C/W
CERAMIC SOIC (Still Air)	165 C/W
(500LF/Min Air Flow)	110 C/W
(ThetaJC) Junction-to-case	
CERAMIC DIP	24 C/W
CERAMIC SOIC	26 C/W
Package Weight (typical)	
CERAMIC DIP	2190 mg
CERAMIC SOIC	410 mg
ESD Tolerance (Note 3)	4000V

Note 1: Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: The maximum power dissipation must be derated at elevated temperatures and is dictated by Tjmax (maximum junction temperature), ThetaJA (package junction to ambient thermal resistance), and TA (ambient temperature). The maximum allowable power dissipation at any temperature is Pdmax = (Tjmax - TA) / ThetaJA or the number given in the Absolute Maximum Ratings, whichever is lower.

Note 3: Human body model, 100pF discharged through 1.5K Ohms.

Recommended Operating Conditions

Supply voltage (Vs)	±5 Vdc
Ambient Operating Temperature Range (Ta)	-55C to +125C

Electrical Characteristics

DC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Rl = 100 Ohms, Vs = ±5 V dc, Av = +6, and Rf = 500 Ohms. -55 C ≤ Ta ≤ +125C . (NOTE 1)

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
+Iin	Input bias current (noninverting)				-10	+10	uA	1
					-15	+15	uA	2, 3
-Iin	Input bias current (inverting)				-12	+12	uA	1
					-20	+20	uA	2, 3
Vio	Input offset voltage	Rs = 50 Ohms			-6.0	+6.0	mV	1
					-10.0	+10.0	mV	2, 3
Is	Supply current (all channels)	No load				27	mA	1, 3
						28	mA	2
PSRR	Power supply rejection ratio	+Vs = +4.5V to +5.0V, -Vs = -4.5V to -5.0V			53		dB	1
					50		dB	2
					55		dB	3

AC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: Rl = 100 Ohms, Vs = ±5 V dc, Av = +6, and Rf = 500 Ohms. -55 C ≤ Ta ≤ +125C . (NOTE 1)

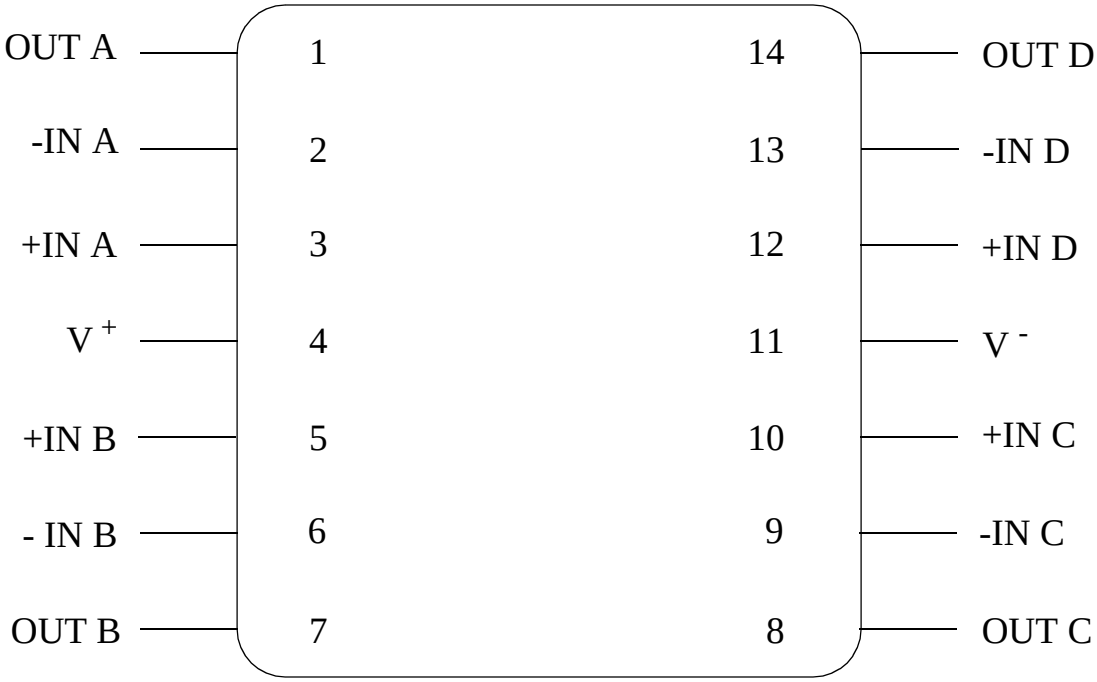
SSBW	Small signal bandwidth	-3dB bandwidth, Vout <2.0Vpp			80		MHz	4
GFPL	Gain flatness peaking low	0.1MHz to 25MHz, Vout <2.0Vpp				0.2	dB	4
GFPH	Gain flatness peaking high	>25MHz, Vout <2.0Vpp				0.2	dB	4
HD2	Second harmonic distortion	2Vpp at 20MHz				-38	dBc	4
HD3	Third harmonic distortion	2Vpp at 20MHz				-46	dBc	4

Note 1: The algebraic convention, whereby the most negative value is a minimum and the most positive is a maximum, is used in this table. Negative current shall be defined as conventional current flow out of a device terminal.

Graphics and Diagrams

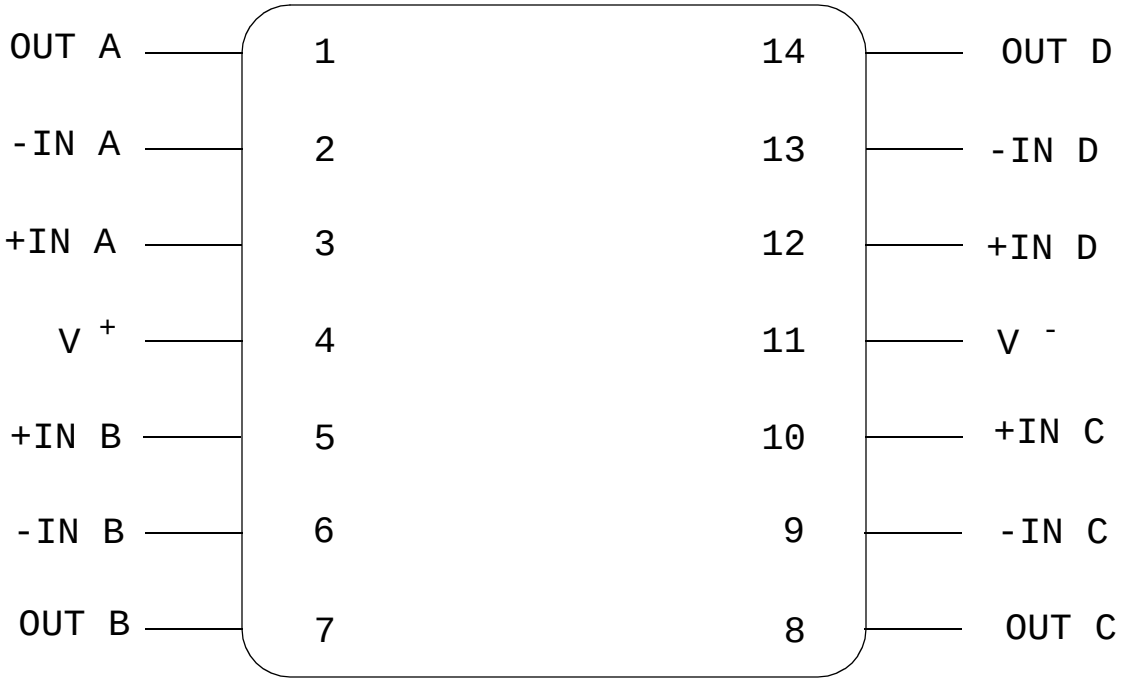
GRAPHICS#	DESCRIPTION
07066HRA2	CERDIP (J), 14 LEAD (B/I CKT)
07071HRA2	CERAMIC SOIC (WG), 14LD (B/I CKT)
J14ARJ	CERDIP (J), 14 LEAD (P/P DWG)
P000488A	CERDIP (J), 14 LEAD (PIN OUT)
P000489A	CERAMIC SOIF (WG), 14LD (PIN OUT)
WG14ARC	CERAMIC SOIC (WG), 14LD (P/P DWG)

See attached graphics following this page.



LMH6722J
14 - LEAD DIP
CONNECTION DIAGRAM
TOP VIEW
P000488A

National Semiconductor™
MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050

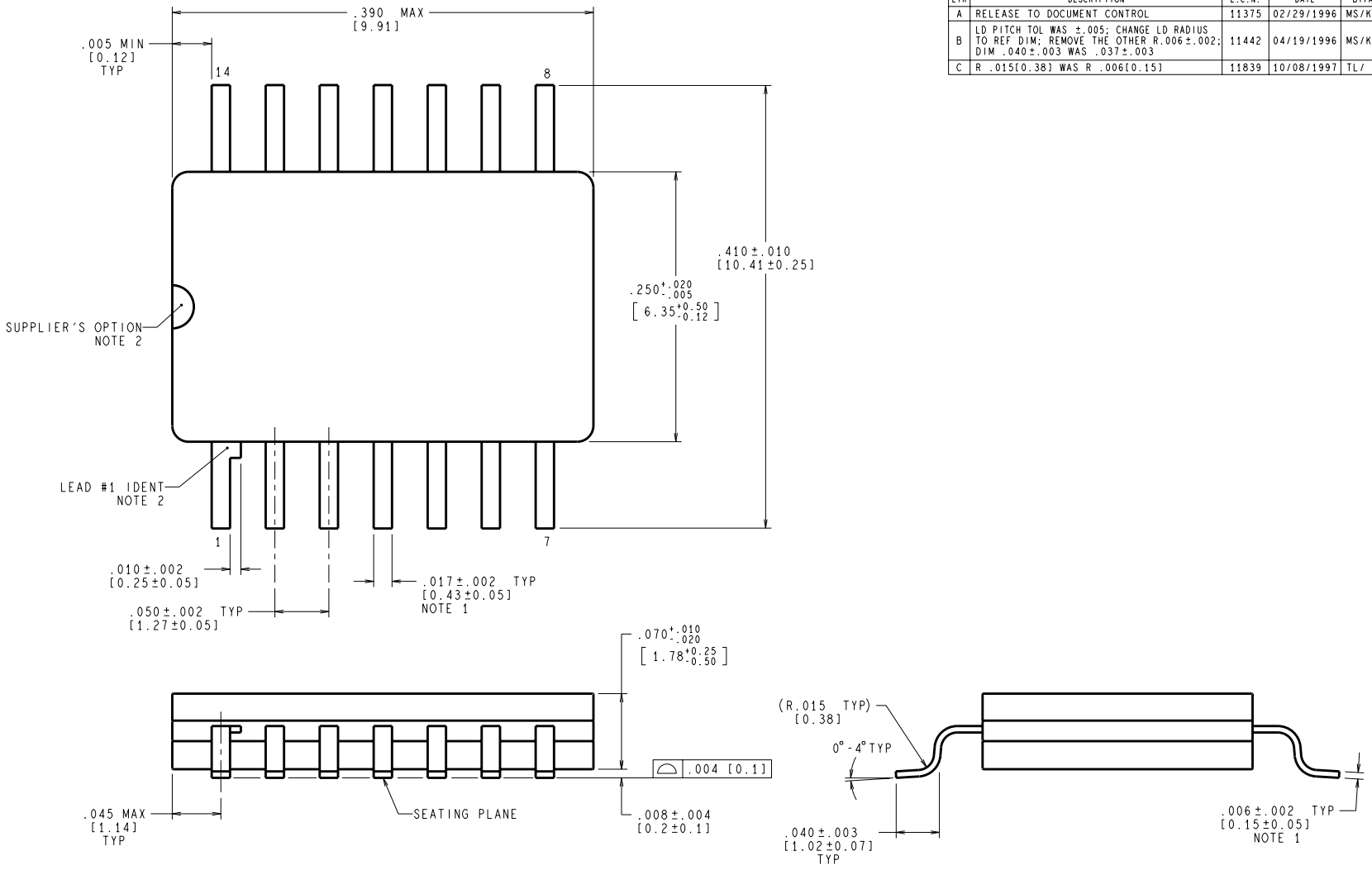


LMH6722W/WG
14 - LEAD FLAT PACK/SOIC
CONNECTION DIAGRAM
TOP VIEW
P000489A

National Semiconductor

MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
A	RELEASE TO DOCUMENT CONTROL	11375	02/29/1996	MS/KH
B	LD PITCH TOL WAS ±.005; CHANGE LD RADIUS TO REF DIM; REMOVE THE OTHER R.006±.002; DIM .040±.003 WAS .037±.003	11442	04/19/1996	MS/KH
C	R .015[0.38] WAS R .006[0.15]	11839	10/08/1997	TL/



NOTES: UNLESS OTHERWISE SPECIFIED

1. LEAD FINISH: SOLDER DIPPED WITH Sn60 OR Sn63 SOLDER CONFORMING TO MIL-PRF-38535 TO A MINIMUM THICKNESS OF 200 MICROINCHES/ 5.08 MICROMETERS. SOLDER MAY BE APPLIED OVER LEAD BASIS METAL OR Sn PLATE. MAXIMUM LIMIT MAY BE INCREASED BY .003 IN/ 0.08mm AFTER LEAD FINISH APPLIED.
2. LEAD 1 IDENTIFICATION SHALL BE:
   a) A NOTCH OR OTHER MARK WITHIN THIS AREA
   b) A TAB ON LEAD 1, EITHER SIDE
3. NO JEDEC REGISTRATION AS OF FEBRUARY 1996.

CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS

MIL-PRF-38535
CONFIGURATION CONTROL

APPROVALS	DATE
DRAWN: MARTA SUCHY	02/29/96
DFTG. CHK.	
ENGR. CHK.	

National Semiconductor
2900 Semiconductor dr, Santa Clara, CA 95052-8090

CERPACK, 14 LEAD, GULL WING

PROJECTION — INCH [MM]

SCALE	SIZE	DRAWING NUMBER	REV
N/A	C	(SC)MKT-WG14A	C

DO NOT SCALE DRAWING — SHEET 1 of 1