

LMS75LBC176

Differential Bus Transceivers

General Description

The LMS75LBC176 is a differential bus/line transceiver designed for bidirectional data communication on multipoint bus transmission lines. It is designed for balanced transmission lines. It meets TIA/EIA RS485 and ISO 8482:1987(E). The LMS75LBC176 combines a TRI-STATE™ differential line driver and differential input receiver, both of which operate from a single 5.0V power supply. The driver and receiver have an active high and active low enable, respectively, that can be externally connected to function as a direction control. The driver and receiver differential inputs are internally connected to form differential input/output (I/O) bus ports that are designed to offer minimum loading to bus whenever the driver is disabled or when $V_{CC} = 0V$. These ports feature wide positive and negative common mode voltage ranges, making the device suitable for multipoint applications in noisy environments. The LMS75LBC176 is available in a 8-Pin SOIC package. It is a drop-in socket replacement to TI's SN75LBC176.

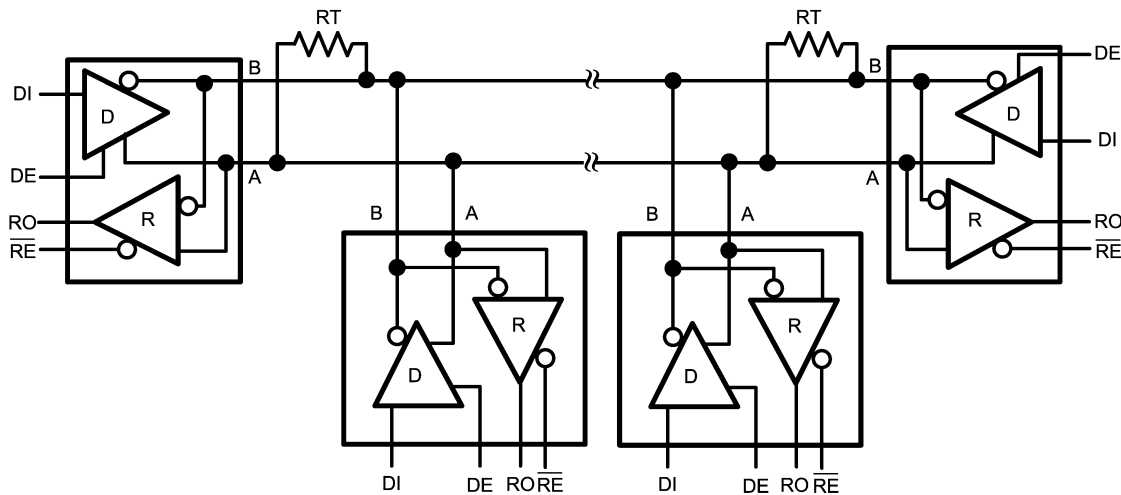
Features

- Bidirectional transceiver
- Meet ANSI standard RS-485
- Low skew, 6ns
- Low supply current, 8mA (max)
- Wide input and output voltage range
- High output drive capacity $\pm 60mA$
- Thermal shutdown protection
- Open circuit fail-safe for receiver
- Receiver input sensitivity $\pm 200mV$
- Receiver input hysteresis 10mV (min.)
- Single supply voltage operation, 5V
- Glitch free power-up and power-down operation
- Pin and functional compatible with TI's SN75LBC176
- 8-Pin SOIC

Applications

- Network hubs, bridges, and routers
- Point of sales equipment (ATM, barcode readers,...)
- Industrial programmable logic controllers
- High speed parallel and serial applications
- Multipoint applications with noisy environment

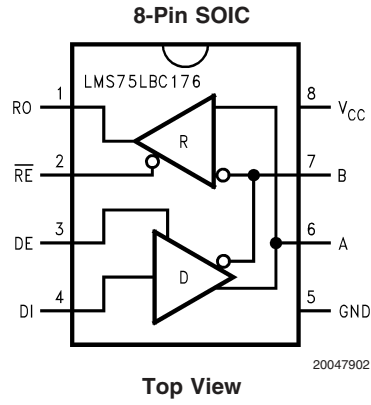
Typical Application



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A typical multipoint application is shown in the above figure. Terminating resistors, R_T , are typically required but only located at the two ends of the cable. Pull up and pull down resistors may be required at the end of the bus to provide failsafe biasing. The biasing resistors provide a bias to the cable when all drivers are in TRI-STATE, See National Application Note, AN-847 for further information.

Connection Diagram



Ordering Information

Package	Part Number	Package Marking	Transport Media	NSC Drawing
8-Pin SOIC	LMS75LBC176M	LMS75LBC176	Rail	M08A
	LMS75LBC176MX		2.5k Units Tape and Reel	

Truth Table

DRIVER SECTION				
RE	DE	DI	A	B
X	H	H	H	L
X	H	L	L	H
X	L	X	Z	Z
RECEIVER SECTION				
RE	DE	A-B		RO
L	L	$\geq +0.2V$		H
L	L	$\leq -0.2V$		L
H	X	X		Z
L	L	OPEN *		H

Note: * = Non Terminated, Open Input only

X = Irrelevant

Z = TRI-STATE

H = High level

L = Low level

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage, V_{CC} (Note 2)	7V
Voltage Range at Any Bus Terminal	-7V to 12V
Input Voltage, V_{IN} (DI, DE, or \overline{RE})	-0.3V to $V_{CC} + 0.3V$
Package Thermal Impedance, θ_{JA}	125C/W
Junction Temperature (Note 3)	150°C
Operating Free-Air Temperature Range, T_A	0°C to 70°C
Storage Temperature Range	-65°C to 150°C
Soldering Information	
Infrared or Convection (20 sec.)	235°C
ESD Rating (Note 4)	2KV

Operating Ratings

	Min	Nom	Max	
Supply Voltage, V_{CC}	4.75	5.0	5.25	V
Voltage at any Bus Terminal (Separately or Common Mode)			12	V
			-7	
V_{IN} or V_{IC}				
High-Level Input Voltage, V_{IH} (Note 5)	2			V
Low-Level Input Voltage, V_{IL} (Note 5)			0.8	V
Differential Input Voltage, V_{ID} (Note 6)			±12	V
High-Level Output				
Driver, I_{OH}			-60	mA
Receiver, I_{OH}			-400	µA
Low-Level Output				
Driver, I_{OL}			60	mA
Receiver, I_{OL}			8	mA

Electrical Characteristics

$V_{CC} = 5V$, $T_A = 0^\circ C$ to $70^\circ C$

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Driver Section						
V_{CL}	Input Clamp Voltage	$I_I = -18mA$			-1.5	V
V_O	Output Voltage	$I_O = 0$	0		6	V
$ V_{OD1} $	Differential Output Voltage	$I_O = 0$	1.5		6	V
$ V_{OD2} $	Differential Output Voltage	$R_L = 54\Omega$	1.5		5	V
V_{OD3}	Differential Output Voltage	$V_{TEST} = -7V$ to 12V	1.5		5	V
ΔV_{OD}	Change in Magnitude of Differential Output Voltage (Note 8)	$R_L = 54\Omega$ or 100Ω			±0.2	V
V_{OC}	Common-Mode Output Voltage	$R_L = 54\Omega$ or 100Ω			3 -1	V
ΔV_{OC}	Change in Magnitude of Differential Output Voltage (Note 8)	$R_L = 54\Omega$ or 100Ω			±0.2	V
I_O	Output Current	Output Disabled (Note 8)			1 -0.8	mA
		$V_O = 12V$				
		$V_O = -7V$				
I_{IH}	High-Level Input Current	$V_{IN} = 2.4V$			-100	µA
I_{IL}	Low-Level Input Current	$V_{IN} = 0.4V$			-100	µA
I_{OSD}	Short-Circuit Output Current	$V_O = -7V$			-250	mA
		$V_O = 0$			-150	
		$V_O = V_{CC}$			250	
		$V_O = 12V$			250	
I_{CC}	Supply Current	$V_{IN} = 0$ or V_{CC} , No Load			8	mA
		Receiver Disabled and Driver Enabled				
		Receiver and Driver Disabled			8	

Electrical Characteristics (Continued) $V_{CC} = 5V, T_A = 0^{\circ}C \text{ to } 70^{\circ}C$

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Switching Characteristics						
t_d (OD)	Differential Output Delay Time	$R_L = 54\Omega, C_L = 50pF$	3		25	ns
t_t (OD)	Differential Output Transition Time	$R_L = 54\Omega, C_L = 50pF$		8		ns
$t_{sk(p)}$	Pulse Skew, ($ t_{d(ODH)} - t_{d(ODL)} $)	$R_L = 54\Omega, C_L = 50pF$		0	6	ns
t_{PZH}	Output Enable Time to High Level	$R_L = 110\Omega, C_L = 50pF$			35	ns
t_{PZL}	Output Enable Time to Low Level	$R_L = 110\Omega, C_L = 50pF$			35	ns
t_{PHZ}	Output Disable Time from High Level	$R_L = 110\Omega, C_L = 50pF$			60	ns
t_{PLZ}	Output Disable Time from Low Level	$R_L = 110\Omega, C_L = 50pF$			35	ns
Receiver Section						
V_{TH+}	Positive-Going Input Threshold Voltage	$V_O = 2.7V, I_O = -0.4mA$			0.2	V
V_{TH-}	Negative-Going Input Threshold Voltage	$V_O = 0.5V, I_O = 8mA$	-0.2			V
ΔV_{TH}	Hysteresis Voltage ($V_{TH+} - V_{TH-}$)		10			mV
V_{CL}	Enable-Input Clamp Voltage	$I_I = -18mA$			-1.5	V
V_{OH}	High-Level Output Voltage	$V_{ID} = 200mV, I_{OH} = -400\mu A$	2.7			V
V_{OL}	Low-Level Output Voltage	$V_{ID} = -200mV, I_{OL} = 8mA$			0.45	V
I_{OZ}	High-Impedance-State Output Current	$V_O = 0.4V \text{ to } 2.4V$			± 20	μA
I_{IN}	Line Input Current	Other Input = 0V, See (Note 8)	$V_{IN} = 12V$		1	mA
			$V_{IN} = -7V$		-0.8	
I_{IH}	High-Level Enable-Input Current	$V_{IH} = 2.7V$			-100	μA
I_{IL}	Low-Level Enable-Input Current	$V_{IL} = 0.4V$			-100	μA
R_{IN}	Input Resistance		12			k Ω
I_{CC}	Supply Current	$V_{IN} = 0 \text{ or } V_{CC},$ No Load	Receiver Enabled and Driver Disabled		8	mA
			Receiver and Driver Disabled		8	
Switching Characteristics						
T_{PLH}	Propagation Delay Time, Low-to High-Level Single-Ended Output	$V_{ID} = -1.5V \text{ to } 1.5V$	8		33	ns
T_{PHL}	Propagation Delay Time, High-to Low-Level Single-Ended Output	$V_{ID} = -1.5V \text{ to } 1.5V$	8		33	ns
$t_{sk(p)}$	Pulse Skew ($ t_{PLH} - t_{PHL} $)	$V_{ID} = -1.5V \text{ to } 1.5V$		2		ns

Electrical Characteristics (Continued) $V_{CC} = 5V$, $T_A = 0^{\circ}C$ to $70^{\circ}C$

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PZH}	Output Enable Time to High Level				35	ns
t_{PZL}	Output Enable Time to Low Level				30	ns
t_{PHZ}	Output Disable Time from High Level				35	ns
t_{PLZ}	Output Disable Time from Low Level				30	ns

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics

Note 2: All voltage values, except differential I/O bus voltage, are with respect to network ground terminal.

Note 3: The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA} , and T_A . The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly into a PC board.

Note 4: ESD rating based upon human body model, 100pF discharged through 1.5k Ω .

Note 5: Voltage limits apply to DI, DE, \overline{RE} pins.

Note 6: Differential input/output bus voltage is measured at the non-inverting terminal A with respect to the inverting terminal B

Note 7: ΔV_{OD} and $|\Delta V_{OC}|$ are changes in magnitude of V_{OD} and V_{OC} , respectively when the input changes from high to low levels.

Note 8: Applies to both power on and off (ANSI Standard RS-485 conditions).

Parameter Measuring Information

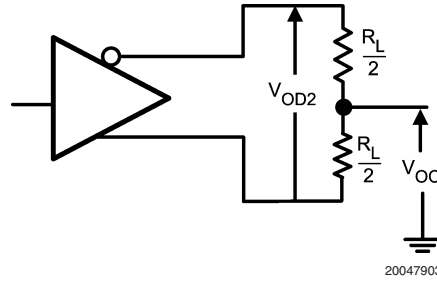


FIGURE 1. Test Circuit for V_{OD2} and V_{OC}

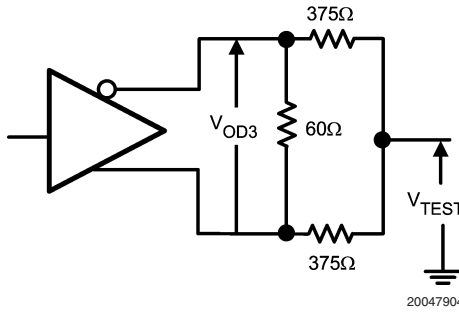


FIGURE 2. Test Circuit for V_{OD2}

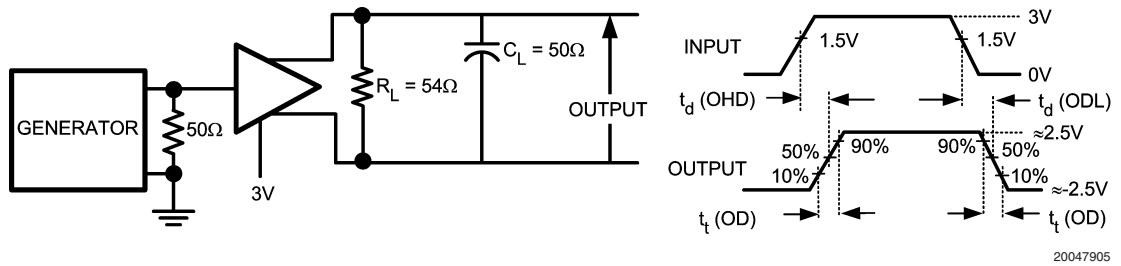


FIGURE 3. Test Circuit for Driver Differential Output Delay and Transition Times

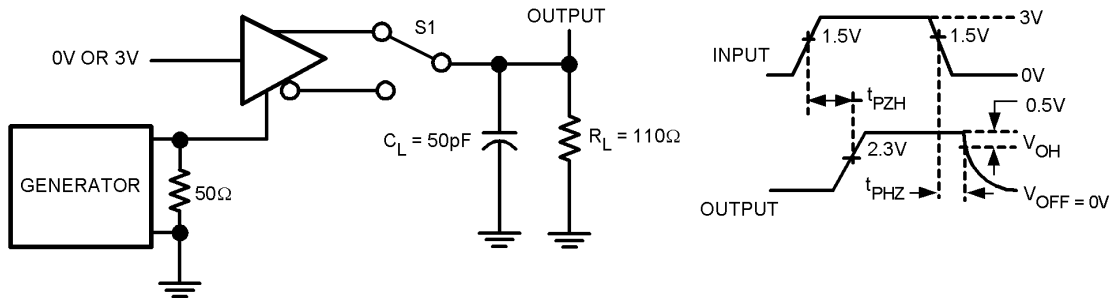
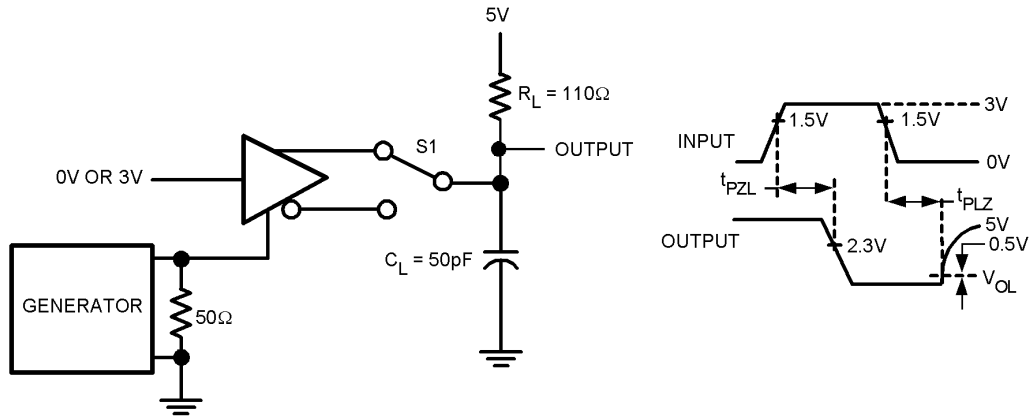


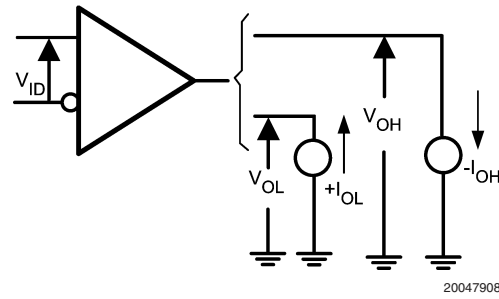
FIGURE 4. Test Circuit for Driver T_{PZH} and T_{PHZ}

Parameter Measuring Information (Continued)



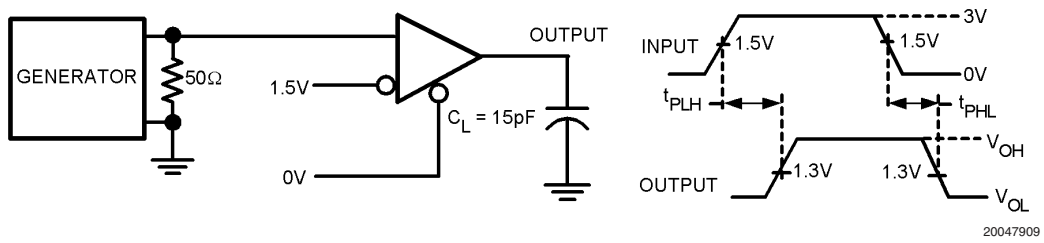
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FIGURE 5. Test Circuit for Driver T_{PZL} and T_{PLZ}



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FIGURE 6. Test Circuit for Receiver V_{OH} and V_{OL}

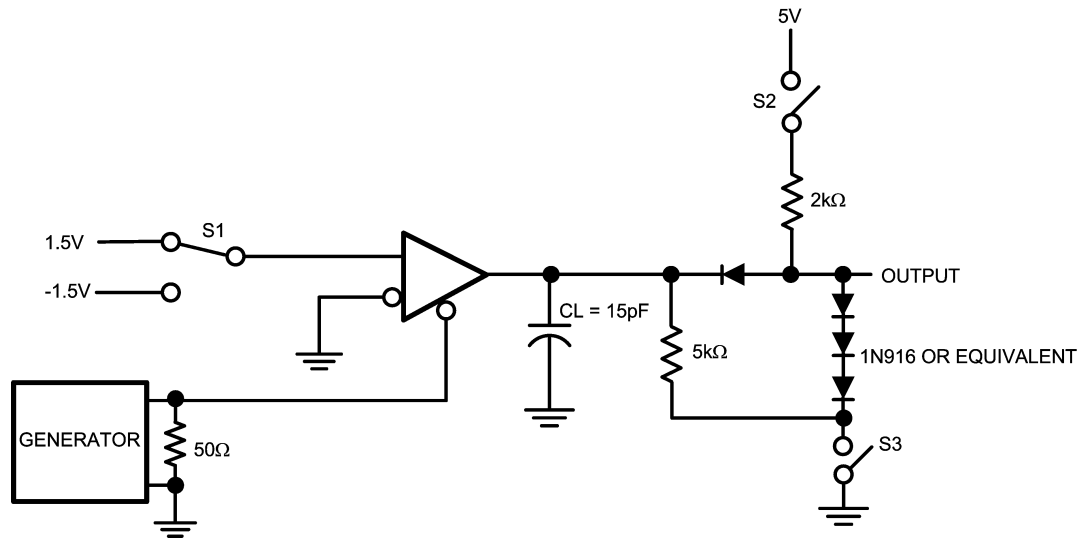


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FIGURE 7. Test Circuit for Receiver T_{PLH} and T_{PHL}

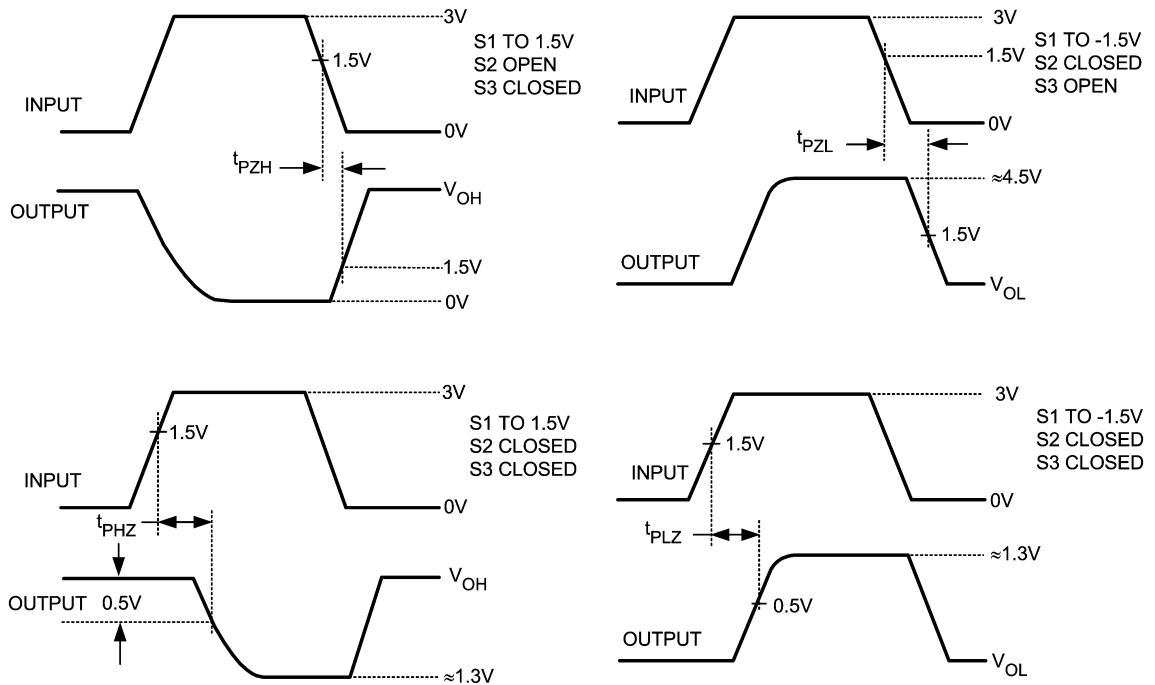
Parameter Measuring Information (Continued)

Test Circuit



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Voltage Waveforms



VOLTAGE WAVEFORMS

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FIGURE 8. Test Circuit for Receiver T_{PZH}/T_{PZL} and T_{PHZ}/T_{PLZ}

Application Information

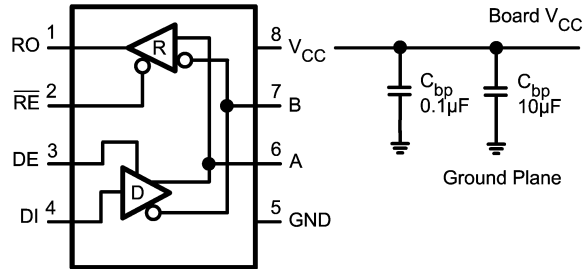
POWER LINE NOISE FILTERING

A factor to consider in designing power and ground is noise filtering. A noise filtering circuit is designed to prevent noise generated by the integrated circuit (IC) as well as noise entering the IC from other devices. A common filtering method is to place by-pass capacitors (C_{bp}) between the power and ground lines.

Placing a by-pass capacitor (C_{bp}) with the correct value at the proper location solves many power supply noise problems. Choosing the correct capacitor value is based upon the desired noise filtering range. Since capacitors are not

ideal, they may act more like inductors or resistors over a specific frequency range. Thus, many times two by-pass capacitors may be used to filter a wider bandwidth of noise. It is highly recommended to place a larger capacitor, such as $10\mu\text{F}$, between power supply pin and ground to filter out low frequencies and a $0.1\mu\text{F}$ to filter out higher frequencies.

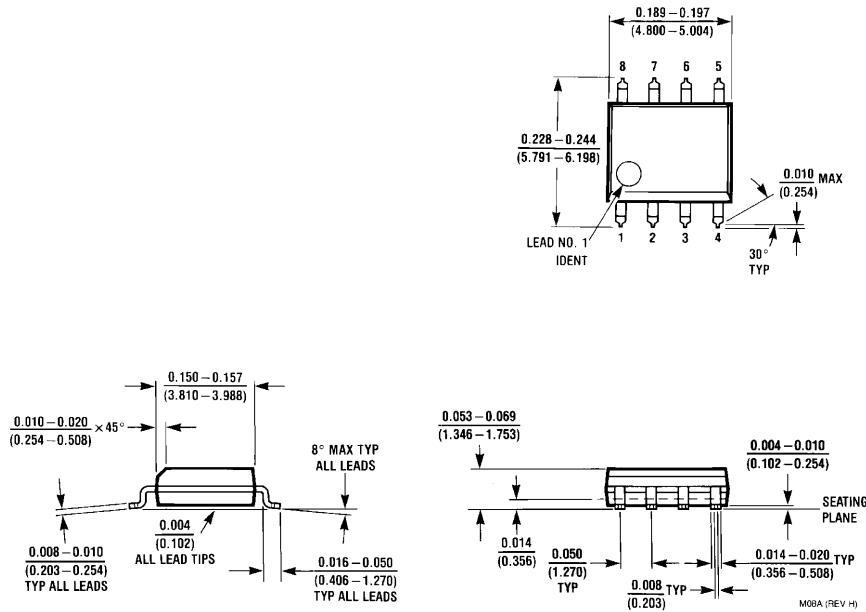
By-pass capacitors must be mounted as close as possible to the IC to be effective. Long leads produce higher impedance at higher frequencies due to stray inductance. Thus, this will reduce the by-pass capacitor's effectiveness. Surface mounting chip capacitors are the best solution because they have lower inductance.



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FIGURE 9. Placement of by-pass Capacitors, C_{bp}

Physical Dimensions inches (millimeters) unless otherwise noted



**8-Pin SOIC
NS Package Number M08A**

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