National Semiconductor

June 2004

LMV331 Single / LMV393 Dual / LMV339 Quad General Purpose, Low Voltage, Tiny Pack Comparators

General Description

The LMV393 and LMV339 are low voltage (2.7-5V) versions of the dual and quad comparators, LM393/339, which are specified at 5-30V. The LMV331 is the single version, which is available in space saving SC70-5 and SOT23-5 packages. SC70-5 is approximately half the size of SOT23-5.

The LMV393 is available in 8-pin SOIC and 8-pin MSOP. The LMV339 is available in 14-pin SOIC and 14-pin TSSOP.

The LMV331/393/339 is the most cost-effective solution where space, low voltage, low power and price are the primary specification in circuit design for portable consumer products. They offer specifications that meet or exceed the familiar LM393/339 at a fraction of the supply current.

The chips are built with National's advanced Submicron Silicon-Gate BiCMOS process. The LMV331/393/339 have bipolar input and output stages for improved noise performance.

Features

(For 5V Supply, Typical Unless Otherwise Noted)

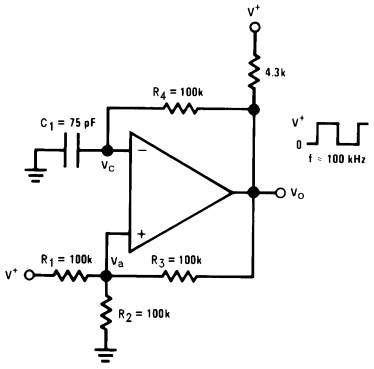
- Space Saving SC70-5 Package (2.0 x 2.1 x 1.0 mm)
- Space Saving SOT23-5 Package (3.00 x 3.01 x1.43 mm)
- Guaranteed 2.7V and 5V Performance
- Industrial Temperature Range –40˚C to +85˚C
- Low Supply Current 60µA/Channel
- Input Common Mode Voltage Range Includes Ground
- Low Output Saturation Voltage 200 mV

Applications

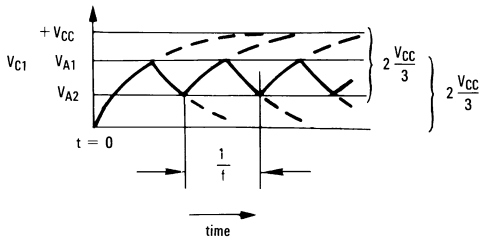
- Mobile Communications
- Notebooks and PDA's
- Battery Powered Electronics
- General Purpose Portable Device
- General Purpose Low Voltage Applications

Typical Applications

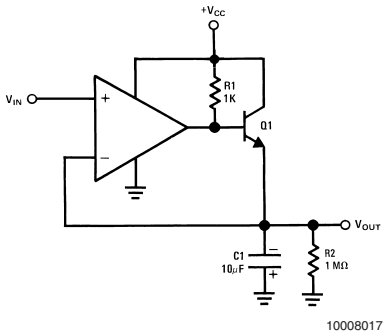
Squarewave Oscillator



10008008



10008024



10008017

Positive Peak Detector

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

ESD Tolerance (Note 2)	
Human Body Model	
LMV331/ 393/ 339	800V
Machine Model LMV331/339/393	120V
Differential Input Voltage	± Supply Voltage
Voltage on any pin (referred to V^- pin)	5.5V
Soldering Information	
Infrared or Convection (20 sec)	235˚C
Storage Temp. Range	−65˚C to +150˚C
Junction Temperature (Note 3)	150˚C

Operating Ratings (Note 1)

Supply Voltage	2.7V to 5.0V
Temperature Range	
LMV393, LMV339, LMV331	$-40˚C \le T_J \le +85˚C$
Thermal Resistance (θ_{JA})	
M Package, 8-pin Surface Mount	190˚C/W
M Package, 14-pin Surface Mount	145˚C/W
MTC Package, 14-pin TSSOP	155˚C/W
MAA05 Package, 5-pin SC70-5	478˚C/W
M05A Package 5 -pin SOT23-5	265˚C/W
MM Package, 8-pin Mini Surface Mount	235˚C/W

2.7V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25˚C, V+ = 2.7V, V− = 0V. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 4)	LMV331/ 393/339 Limit (Note 5)	Units
V_{OS}	Input Offset Voltage		1.7	7	mV max
TCV_{OS}	Input Offset Voltage Average Drift		**5**		µV/˚C
I_B	Input Bias Current		10	250 **400**	nA max
I_{OS}	Input Offset Current		5	50 **150**	nA max
V_{CM}	Input Voltage Range		−0.1		V
			2.0		V
V_{SAT}	Saturation Voltage	$I_{sink} \le$ 1mA	200		mV
I_O	Output Sink Current	$V_O \le$ 1.5V	23	5	mA min
I_S	Supply Current	LMV331	40	100	µA max
		LMV393 Both Comparators	70	140	µA max
		LMV339 All four Comparators	140	200	µA max
	Output Leakage Current		.003	**1**	µA max

2.7V AC Electrical Characteristics

T_J = 25˚C, V+ = 2.7V, R_L = 5.1 kΩ, V− = 0V.

Symbol	Parameter	Conditions	Typ (Note 4)	Units
t_{PHL}	Propagation Delay (High to Low)	Input Overdrive =10 mV	1000	ns
		Input Overdrive =100 mV	350	ns
t_{PLH}	Propagation Delay (Low to High)	Input Overdrive =10 mV	500	ns
		Input Overdrive =100 mV	400	ns

5V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25˚C, V+ = 5V, V− = 0V. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 4)	LMV331/ 393/339 Limit (Note 5)	Units
V_{OS}	Input Offset Voltage		1.7	7 **9**	mV max
TCV_{OS}	Input Offset Voltage Average Drift		5		µV/˚C
I_B	Input Bias Current		25	250 **400**	nA max
I_{OS}	Input Offset Current		2	50 **150**	nA max
V_{CM}	Input Voltage Range		−0.1		V
			4.2		V
A_V	Voltage Gain		50	20	V/mV min
V_{sat}	Saturation Voltage	$I_{sink} \leq 4$ mA	200	400 **700**	mV max
I_O	Output Sink Current	$V_O \leq 1.5V$	84	10	mA
I_S	Supply Current	LMV331	60	120 **150**	µA max
		LMV393 Both Comparators	100	200 **250**	µA max
		LMV339 All four Comparators	170	300 **350**	µA max
	Output Leakage Current		.003	**1**	µA max

5V AC Electrical Characteristics

T_J = 25˚C, V+ = 5V, R_L = 5.1 kΩ, V− = 0V.

Symbol	Parameter	Conditions	Typ (Note 4)	Units
t_{PHL}	Propagation Delay (High to Low)	Input Overdrive =10 mV	600	ns
		Input Overdrive =100 mV	200	ns
t_{PLH}	Propagation Delay (Low to High)	Input Overdrive =10 mV	450	ns
		Input Overdrive =100 mV	300	ns

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical characteristics.

Note 2: : Human body model, 1.5kΩ in series with 100 pF. Machine model, 200Ω in series with 100 pF.

Note 3: The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly into a PC board.

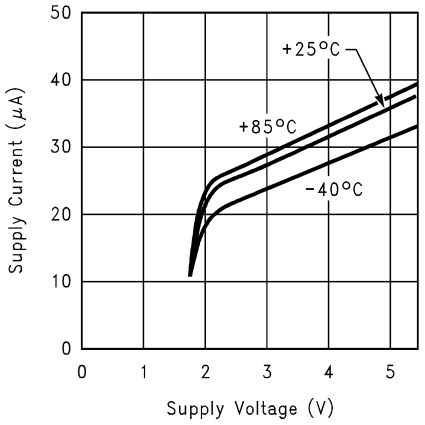
Note 4: Typical Values represent the most likely parametric norm.

Note 5: All limits are guaranteed by testing or statistical analysis.

Typical Performance Characteristics

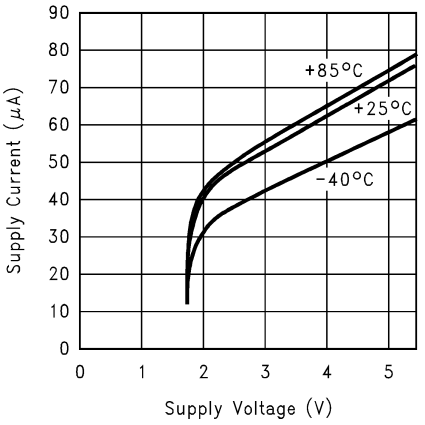
Unless otherwise specified, V_S = +5V, single supply, T_A = 25˚C

Supply Current vs. Supply Voltage Output High (LMV331)



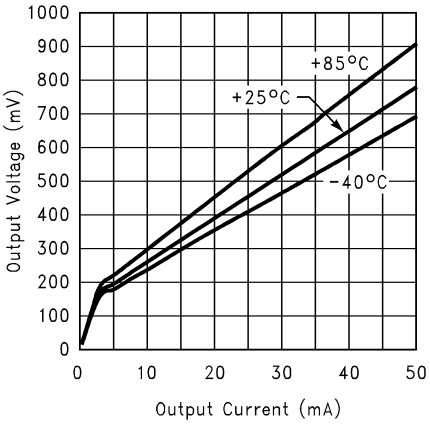
10008034

Supply Current vs. Supply Voltage Output Low (LMV331)



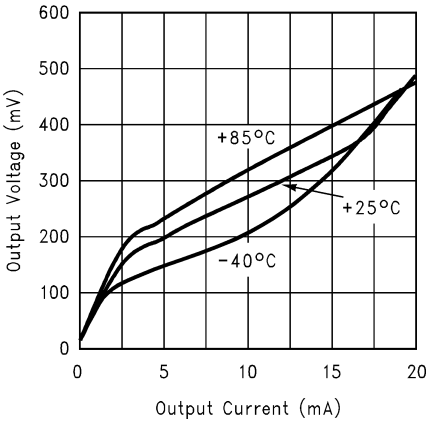
10008033

Output Voltage vs. Output Current at 5V Supply



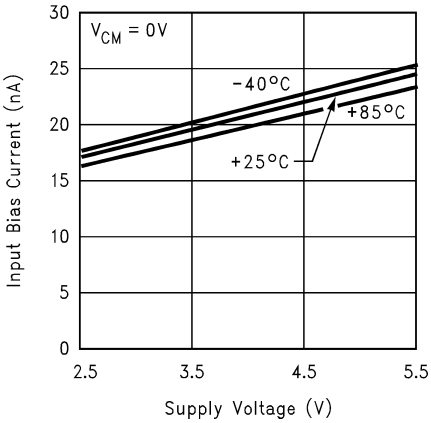
10008037

Output Voltage vs. Output Current at 2.7 Supply



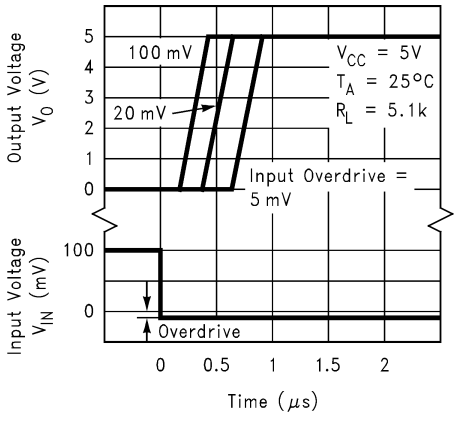
10008038

Input Bias Current vs. Supply Voltage



10008036

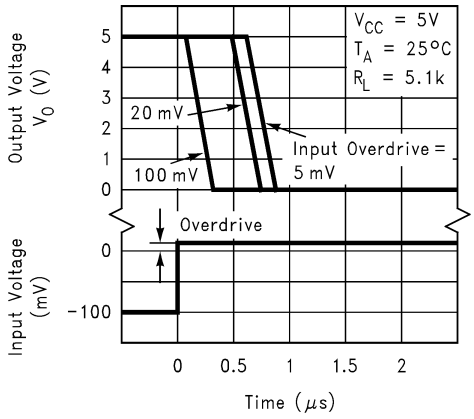
Response Time vs. Input Overdrives Negative Transition



10008042

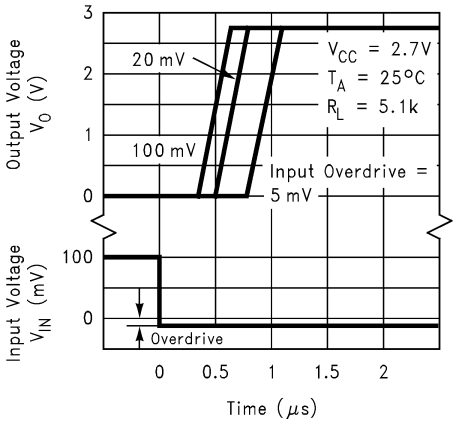
Typical Performance Characteristics Unless otherwise specified, V_S = +5V, single supply, T_A = 25˚C (Continued)

Response Time for Input Overdrive Positive Transition



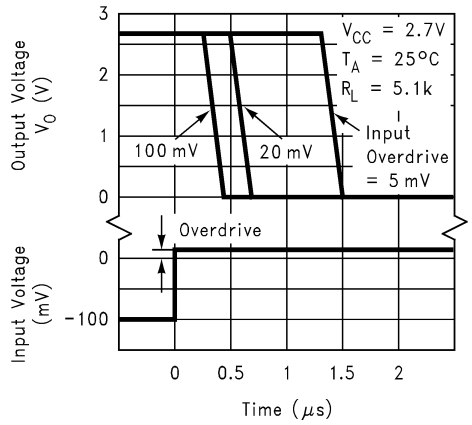
10008043

Response Time vs. Input Overdrives Negative Transition



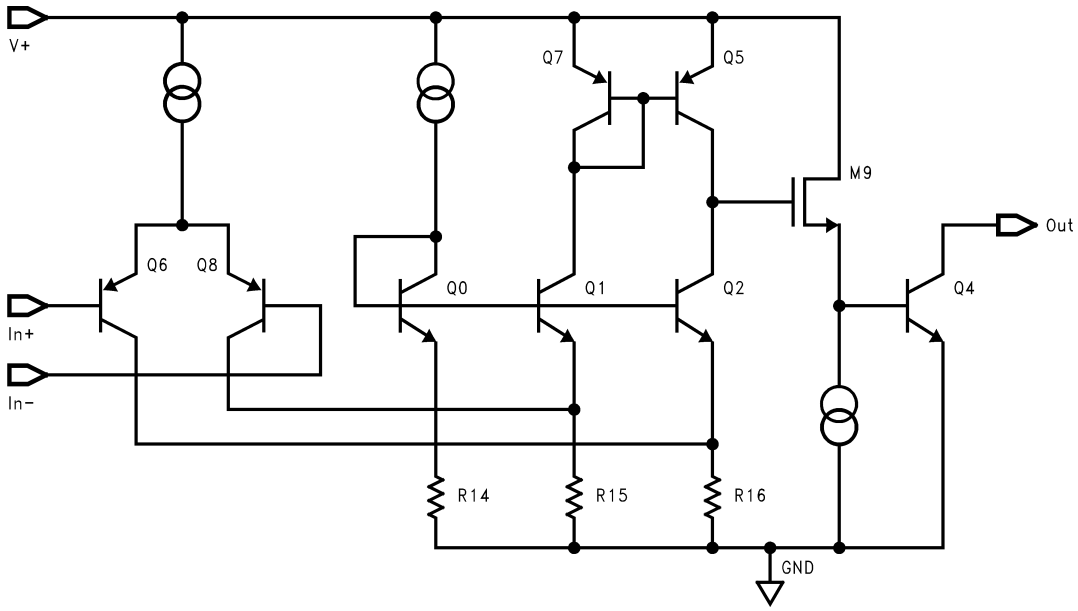
10008041

Response Time for Input Overdrive Positive Transition



10008040

Simplified Schematic



10008047

Application Circuits

BASIC COMPARATOR

A basic comparator circuit is used for converting analog signals to a digital output. The LMV331/393/339 have an open-collector output stage, which requires a pull-up resistor to a positive supply voltage for the output to switch properly. When the internal output transistor is off, the output voltage will be pulled up to the external positive voltage.

The output pull-up resistor should be chosen high enough so as to avoid excessive power dissipation yet low enough to supply enough drive to switch whatever load circuitry is used on the comparator output. On the LMV331/393/339 the pull-up resistor should range between 1k to 10kΩ.

The comparator compares the input voltage (V_{IN}) at the non-inverting pin to the reference voltage (V_{REF}) at the inverting pin. If V_{IN} is less than V_{REF}, the output voltage (V_O) is at the saturation voltage. On the other hand, if V_{IN} is greater than V_{REF}, the output voltage (V_O) is at V_{CC}.

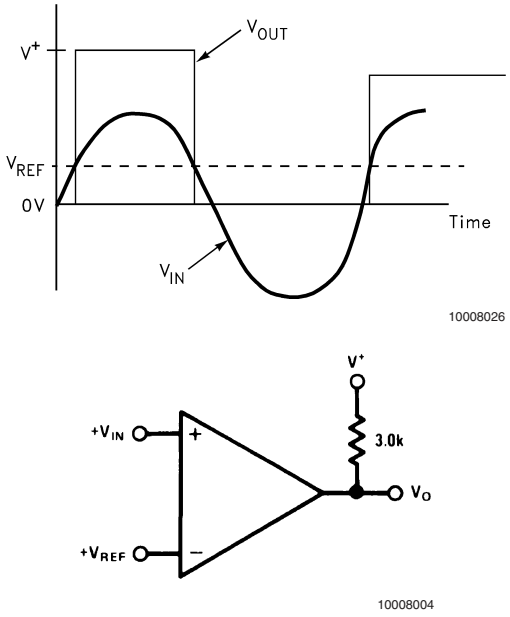


FIGURE 1. Basic Comparator

COMPARATOR WITH HYSTERESIS

The basic comparator configuration may oscillate or produce a noisy output if the applied differential input voltage is near the comparator's offset voltage. This usually happens when the input signal is moving very slowly across the comparator's switching threshold. This problem can be prevented by the addition of hysteresis or positive feedback.

INVERTING COMPARATOR WITH HYSTERESIS

The inverting comparator with hysteresis requires a three resistor network that are referenced to the supply voltage V_{CC} of the comparator. When V_{in} at the inverting input is less than V_a, the voltage at the non-inverting node of the comparator ($V_{in} < V_a$), the output voltage is high (for simplicity assume V_O switches as high as V_{CC}). The three network resistors can be represented as R_1//R_3 in series with R_2. The lower input trip voltage V_{a1} is defined as

$$V_{a_1} = \frac{V_{CC}\ R_2}{(R_1 \,||\, R_3) + R_2}$$

When V_{in} is greater than V_a ($V_{in} > V_a$), the output voltage is low very close to ground. In this case the three network resistors can be presented as R_2//R_3 in series with R_1. The upper trip voltage V_{a2} is defined as

$$V_{a2} = \frac{V_{CC}\,(R_2 \,//\, R_3)}{R_1 + (R_2 \,//\, R_3)}$$

The total hysteresis provided by the network is defined as

$$\Delta V_a = V_{a1} - V_{a2}$$

To assure that the comparator will always switch fully to V_{CC} and not be pulled down by the load the resistors values should be chosen as follow:

$$R_{PULL\text{-}UP} << R_{LOAD}$$

and $R_1 > R_{PULL\text{-}UP}$.

Application Circuits (Continued)

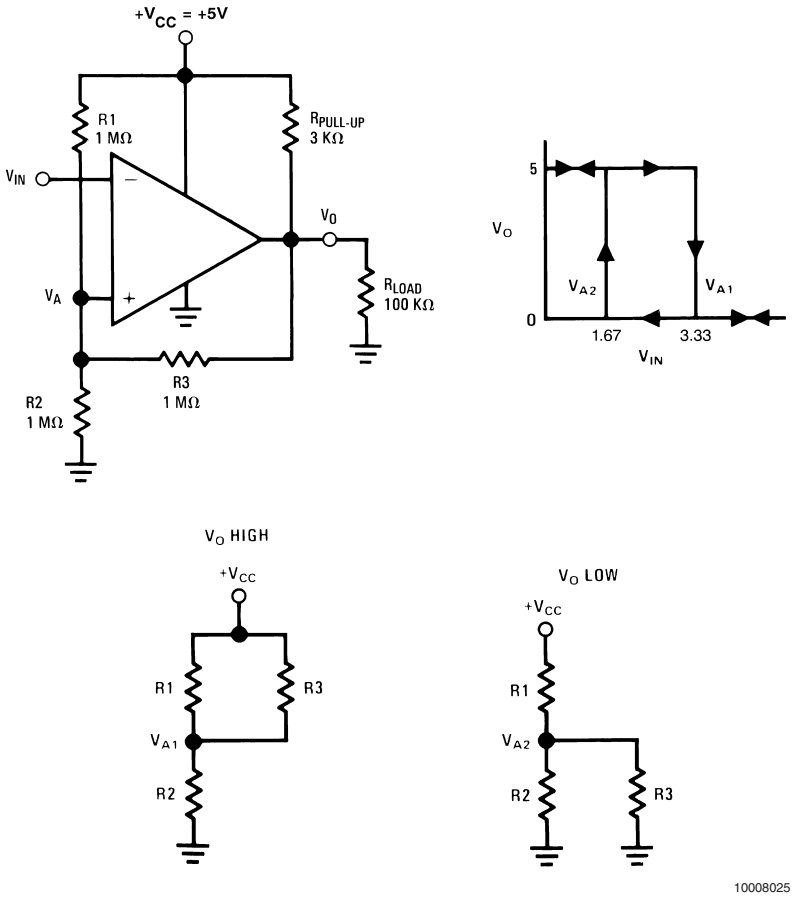


FIGURE 2. Inverting Comparator with Hysteresis

NON-INVERTING COMPARATOR WITH HYSTERESIS

Non inverting comparator with hysteresis requires a two resistor network, and a voltage reference (V_{ref}) at the inverting input. When V_{in} is low, the output is also low. For the output to switch from low to high, V_{in} must rise up to V_{in1} where V_{in1} is calculated by

$$V_{in1} = \frac{V_{ref}(R_1 + R_2)}{R_2}$$

When V_{in} is high, the output is also high, to make the comparator switch back to it's low state, V_{in} must equal V_{ref} before V_A will again equal V_{ref}. V_{in} can be calculated by:

$$V_{in2} = \frac{V_{ref}(R_1 + R_2) - V_{CC}R_1}{R_2}$$

The hysteresis of this circuit is the difference between V_{in1} and V_{in2}.

$$\Delta V_{in} = V_{CC}R_1/R_2$$

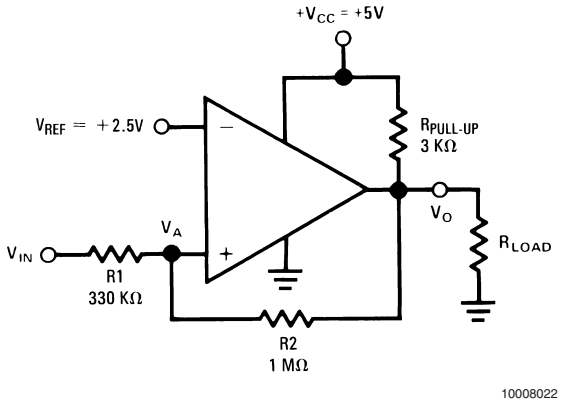


FIGURE 3.

Application Circuits (Continued)

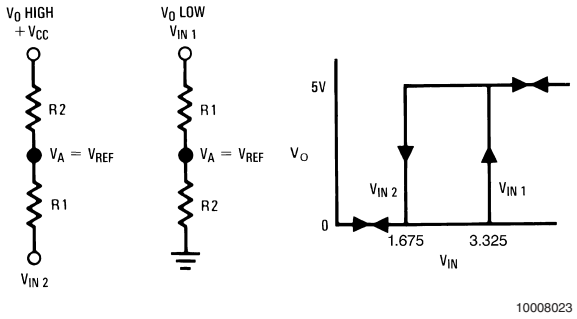
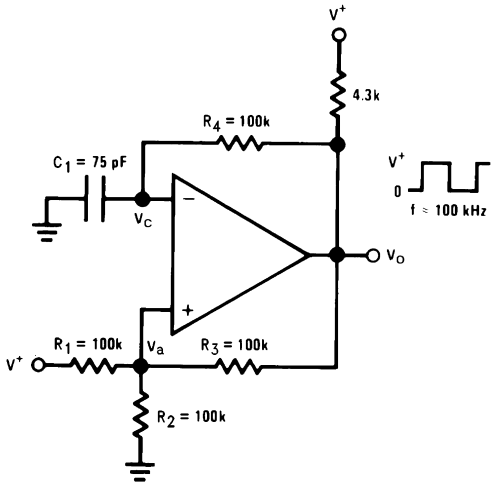


FIGURE 4.

SQUAREWAVE OSCILLATOR

Comparators are ideal for oscillator applications. This square wave generator uses the minimum number of components. The output frequency is set by the RC time constant of the capacitor C_1 and the resistor in the negative feedback R_4. The maximum frequency is limited only by the large signal propagation delay of the comparator in addition to any capacitive loading at the output, which would degrade the output slew rate.



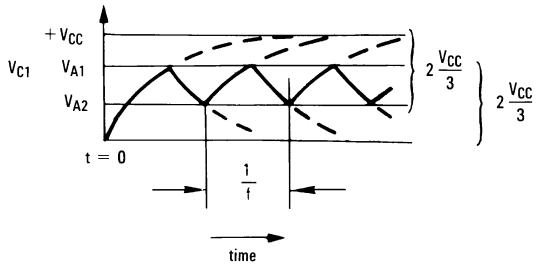


FIGURE 5. Squarewave Oscillator

To analyze the circuit, assume that the output is initially high. For this to be true, the voltage at the inverting input V_c has to be less than the voltage at the non-inverting input V_a. For V_c to be low, the capacitor C_1 has to be discharged and will charge up through the negative feedback resistor R_4. When it has charged up to value equal to the voltage at the positive input V_{a1}, the comparator output will switch.

V_{a1} will be given by:

$$V_{a1} = \frac{V_{CC}\, R_2}{R_2 + (R_1 \,//\, R_2)}$$

If:

$$R_1 = R_2 = R_3$$

Then:

$$V_{a1} = 2V_{CC}/3$$

When the output switches to ground, the value of V_a is reduced by the hysteresis network to a value given by:

$$V_{a2} = V_{CC}/3$$

Capacitor C_1 must now discharge through R_4 towards ground. The output will return to its high state when the voltage across the capacitor has discharged to a value equal to V_{a2}.

For the circuit shown, the period for one cycle of oscillation will be twice the time it takes for a single RC circuit to charge up to one half of its final value. The time to charge the capacitor can be calculated from

$$V_C = V_{max}\ e^{\frac{-t}{RC}}$$

Where V_{max} is the max applied potential across the capacitor = $(2V_{CC}/3)$

and V_C = Vmax/2 = $V_{CC}/3$

One period will be given by:

$$1/\text{freq} = 2t$$

or calculating the exponential gives:

$$1/\text{freq} = 2(0.694)\ R_4\ C_1$$

Resistors R_3 and R_4 must be at least two times larger than R_5 to insure that V_O will go all the way up to V_{CC} in the high state. The frequency stability of this circuit should strictly be a function of the external components.

FREE RUNNING MULTIVIBRATOR

A simple yet very stable oscillator that generates a clock for slower digital systems can be obtained by using a resonator as the feedback element. It is similar to the free running multivibrator, except that the positive feedback is obtained through a quartz crystal. The circuit oscillates when the transmission through the crystal is at a maximum, so the crystal in its series-resonant mode.

The value of R_1 and R_2 are equal so that the comparator will switch symmetrically about $+V_{CC}/2$. The RC constant of R_3 and C_1 is set to be several times greater than the period of the oscillating frequency, insuring a 50% duty cycle by maintaining a DC voltage at the inverting input equal to the absolute average of the output waveform.

When specifying the crystal, be sure to order series resonant with the desired temperature coefficient

Application Circuits (Continued)

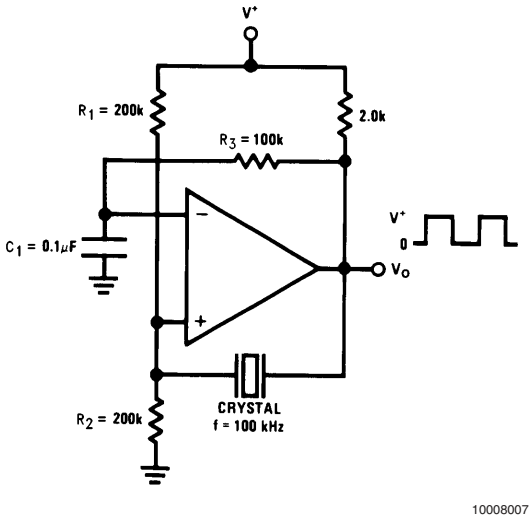


FIGURE 6. Crystal controlled Oscillator

PULSE GENERATOR WITH VARIABLE DUTY CYCLE

The pulse generator with variable duty cycle is just a minor modification of the basic square wave generator. Providing a separate charge and discharge path for capacitor C_1generates a variable duty cycle. One path, through R_2 and D_2 will charge the capacitor and set the pulse width (t_1). The other path, R_1 and D_1 will discharge the capacitor and set the time between pulses (t_2).

By varying resistor R_1, the time between pulses of the generator can be changed without changing the pulse width. Similarly, by varying R_2, the pulse width will be altered without affecting the time between pulses. Both controls will change the frequency of the generator. The pulse width and time between pulses can be found from:

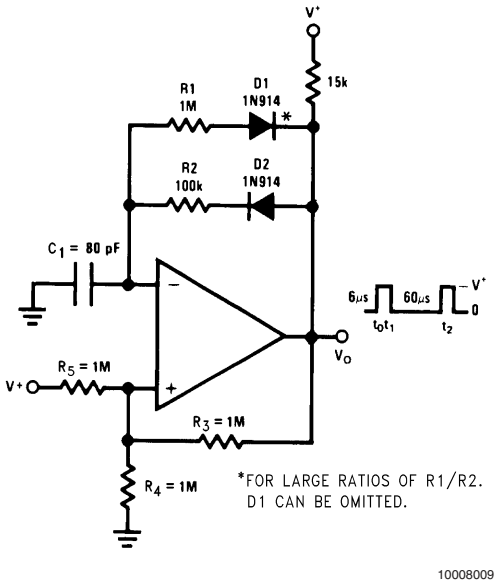


FIGURE 7. Pulse Generator

$$V_1 = V_{max}\left(1 - e^{-t_1/R_4C_1}\right) \quad \text{rise time}$$

$$V_1 = V_{max}\ e^{-t_2/R_5C_1} \quad \text{fall time}$$

Where

$$V_{max} = \frac{2\,V_{CC}}{3}$$

and

$$V_1 = \frac{V_{max}}{3} = \frac{V_{CC}}{3}$$

Which gives

$$\frac{1}{2} = e^{-t_1/R_4C_1}$$

t_2 is then given by:

$$\frac{1}{2} = e^{-t_2/R_5C_1}$$

Solving these equations for t_1 and t_2

$$t_1 = R_4C_1\ln 2$$

$$t_2 = R_5C_1\ln 2$$

These terms will have a slight error due to the fact that V_{max} is not exactly equal to 2/3 V_{CC} but is actually reduced by the diode drop to:

$$V_{max} = \frac{2}{3}\left(V_{CC} - V_{BE}\right)$$

$$\frac{1}{2\left(1 - V_{BE}\right)} = e^{-t_1/R_4C_1}$$

$$\frac{1}{2\left(1 - V_{BE}\right)} = e^{-t_2/R_5C_1}$$

POSITIVE PEAK DETECTOR

Positive peak detector is basically the comparator operated as a unit gain follower with a large holding capacitor from the output to ground. Additional transistor is added to the output to provide a low impedance current source. When the output of the comparator goes high, current is passed through the transistor to charge up the capacitor. The only discharge path will be the 1 MΩ resistor shunting C1 and any load that is connected to the output. The decay time can be altered simply by changing the 1 MΩ resistor. The output should be used through a high impedance follower to a avoid loading the output of the peak detector.

Application Circuits (Continued)

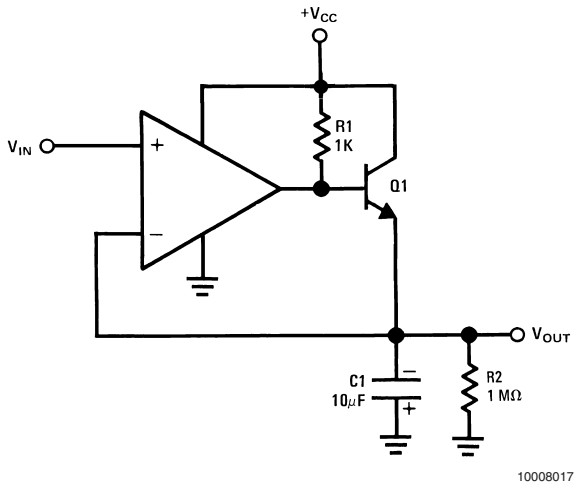


FIGURE 8. Positive Peak Detector

NEGATIVE PEAK DETECTOR

For the negative detector, the output transistor of the comparator acts as a low impedance current sink. The only discharge path will be the 1 MΩ resistor and any load impedance used. Decay time is changed by varying the 1 MΩ resistor

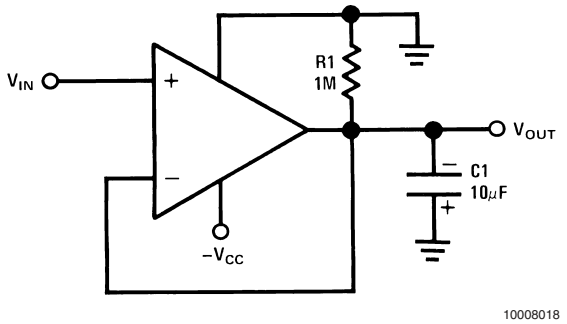


FIGURE 9. Negative Peak Detector

DRIVING CMOS AND TTL

The comparator's output is capable of driving CMOS and TTL Logic circuits.

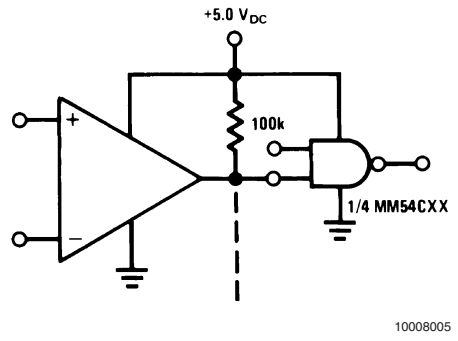


FIGURE 10. Driving CMOS

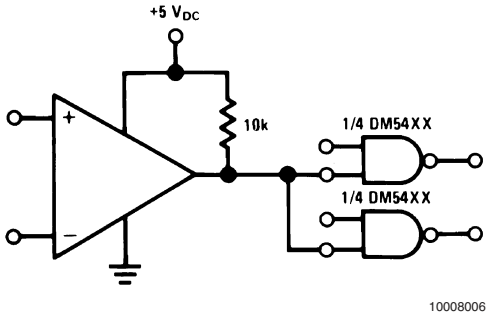


FIGURE 11. Driving TTL

AND GATES

The comparator can be used as three input AND gate. The operation of the gate is as follow:

The resistor divider at the inverting input establishes a reference voltage at that node. The non-inverting input is the sum of the voltages at the inputs divided by the voltage dividers. The output will go high only when all three inputs are high, casing the voltage at the non-inverting input to go above that at inverting input. The circuit values shown work for a "0" equal to ground and a "1" equal to 5V.

The resistor values can be altered if different logic levels are desired. If more inputs are required, diodes are recommended to improve the voltage margin when all but one of the inputs are high.

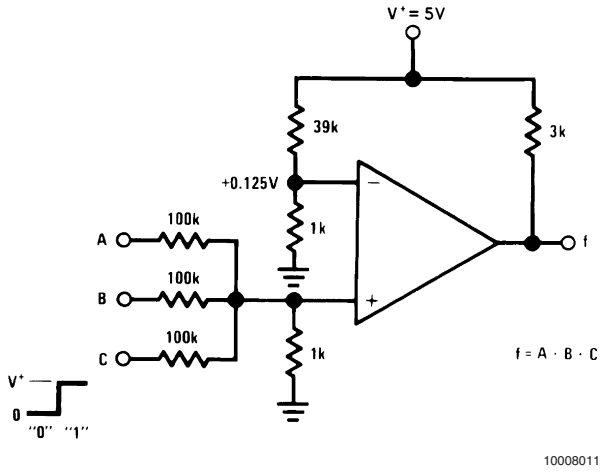


FIGURE 12. AND Gate

OR GATES

A three input OR gate is achieved from the basic AND gate simply by increasing the resistor value connected from the inverting input to V_{cc}, thereby reducing the reference voltage.

A logic "1" at any of the inputs will produce a logic "1" at the output.

Application Circuits (Continued)

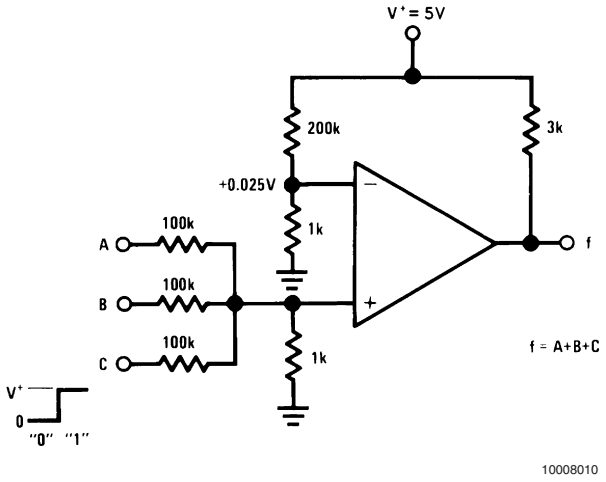


FIGURE 13. OR Gate

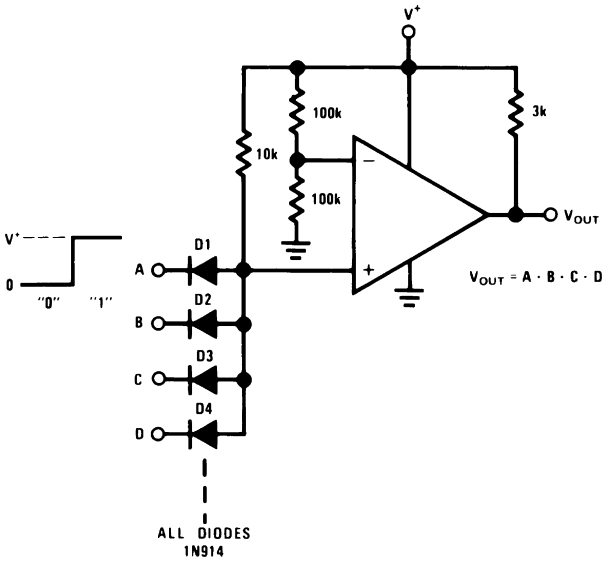


FIGURE 15. Large Fan-In AND Gate

ORing THE OUTPUT

By the inherit nature of an open collector comparator, the outputs of several comparators can be tied together with a pull up resistor to V_{CC}. If one or more of the comparators outputs goes low, the output V_O will go low.

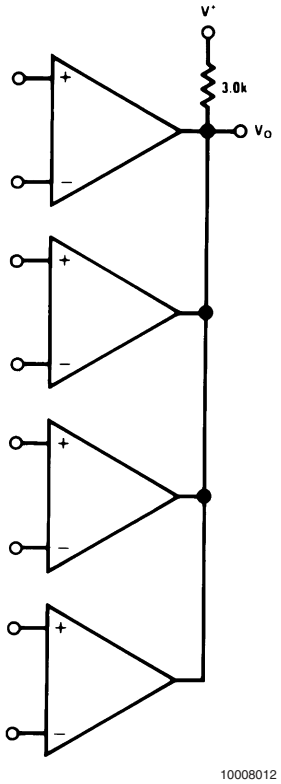
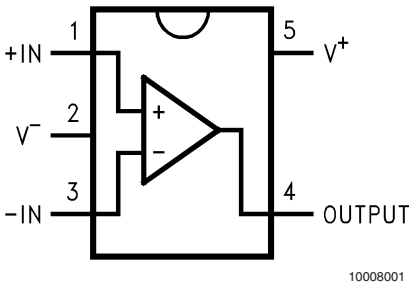


FIGURE 14. ORing the Outputs

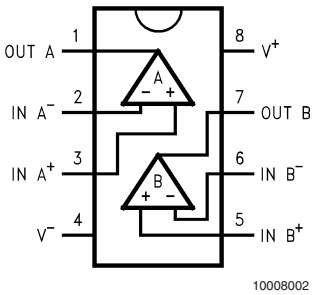
Connection Diagrams

5-Pin SC70-5/SOT23-5



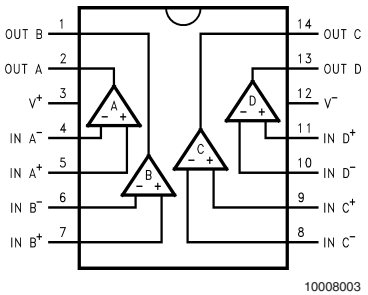
Top View

8-Pin SO/MSOP



Top View

14-Pin SO/TSSOP

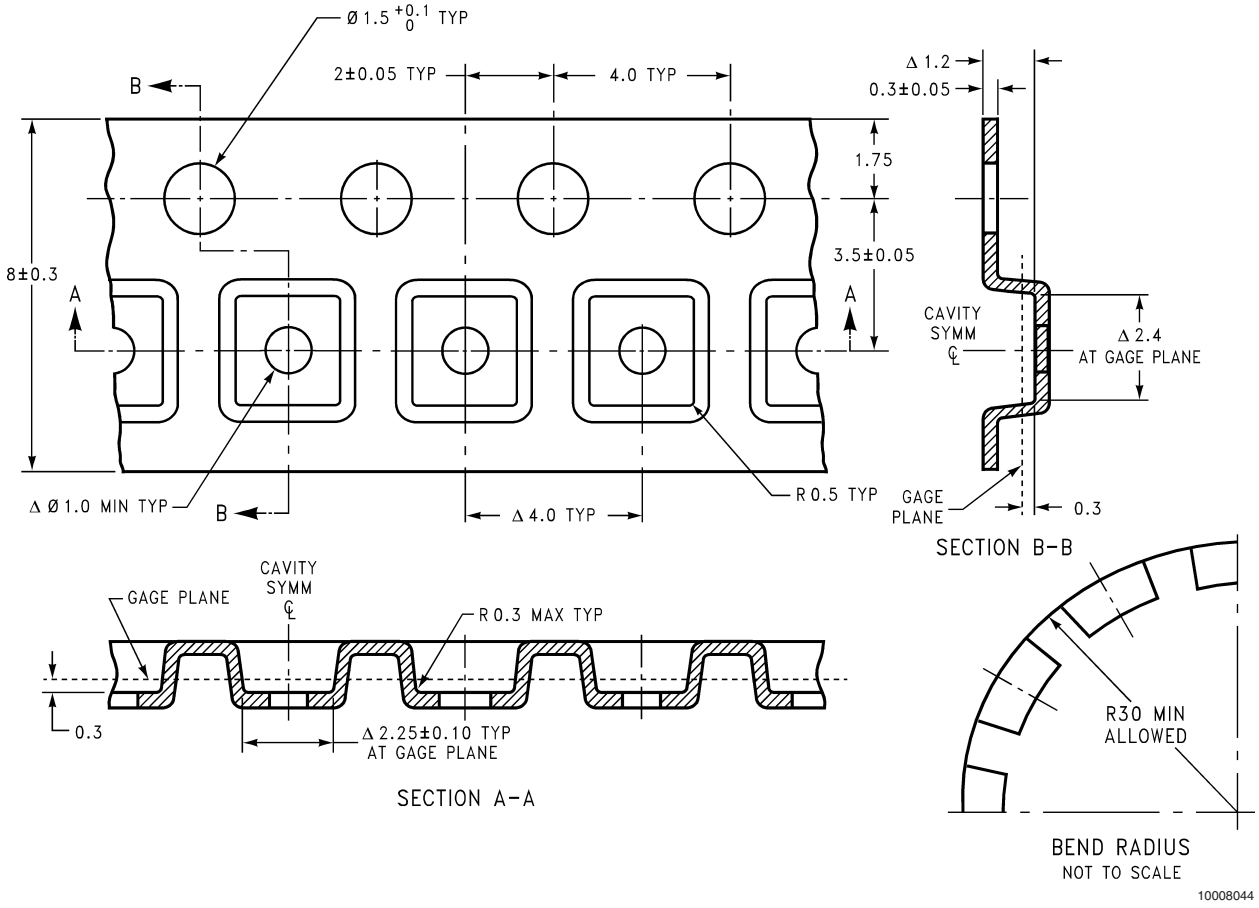


Top View

Ordering Information

Package	Temperature Range	Packaging Marking	Transport Media	NSC Drawing
	Industrial −40˚C to +85˚C			
5-pin SC70-5	LMV331M7	C13	1k Units Tape and Reel	MAA05
	LMV331M7X	C13	3k Units Tape and Reel	
5-pin SOT23-5	LMV331M5	C12	1k Units Tape and Reel	MA05B
	LMV331M5X	C12	3k Units Tape and Reel	
8-pin Small Outline	LMV393M	LMV393M	Rails	M08A
	LMV393MX	LMV393M	2.5k Units Tape and Reel	
8-pin MSOP	LMV393MM	V393	1k UnitsTape and Reel	MUA08A
	LMV393MMX	V393	3.5k Units Tape and Reel	
14-pin Small Outline	LMV339M	LMV339M	Rails	M14A
	LMV339MX	LMV339M	2.5k Units Tape and Reel	
14-pin TSSOP	LMV339MT	LMV339MT	Rails	MTC14
	LMV339MTX	LMV339MT	2.5k Units Tape and Reel	

SC70-5 Tape and Reel Specification



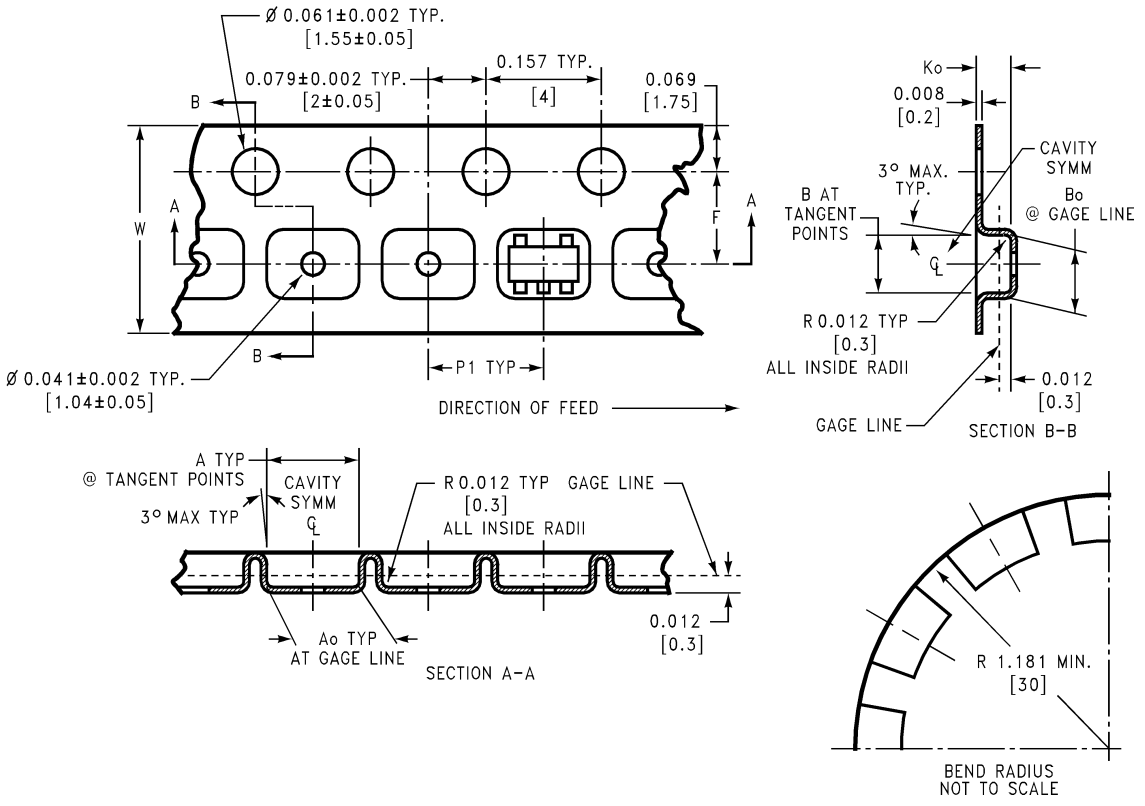
SOT-23-5 Tape and Reel Specification

TAPE FORMAT

Tape Section	# Cavities	Cavity Status	Cover Tape Status
Leader	0 (min)	Empty	Sealed
(Start End)	75 (min)	Empty	Sealed
Carrier	3000	Filled	Sealed
	250	Filled	Sealed
Trailer	125 (min)	Empty	Sealed
(Hub End)	0 (min)	Empty	Sealed

SOT-23-5 Tape and Reel Specification (Continued)

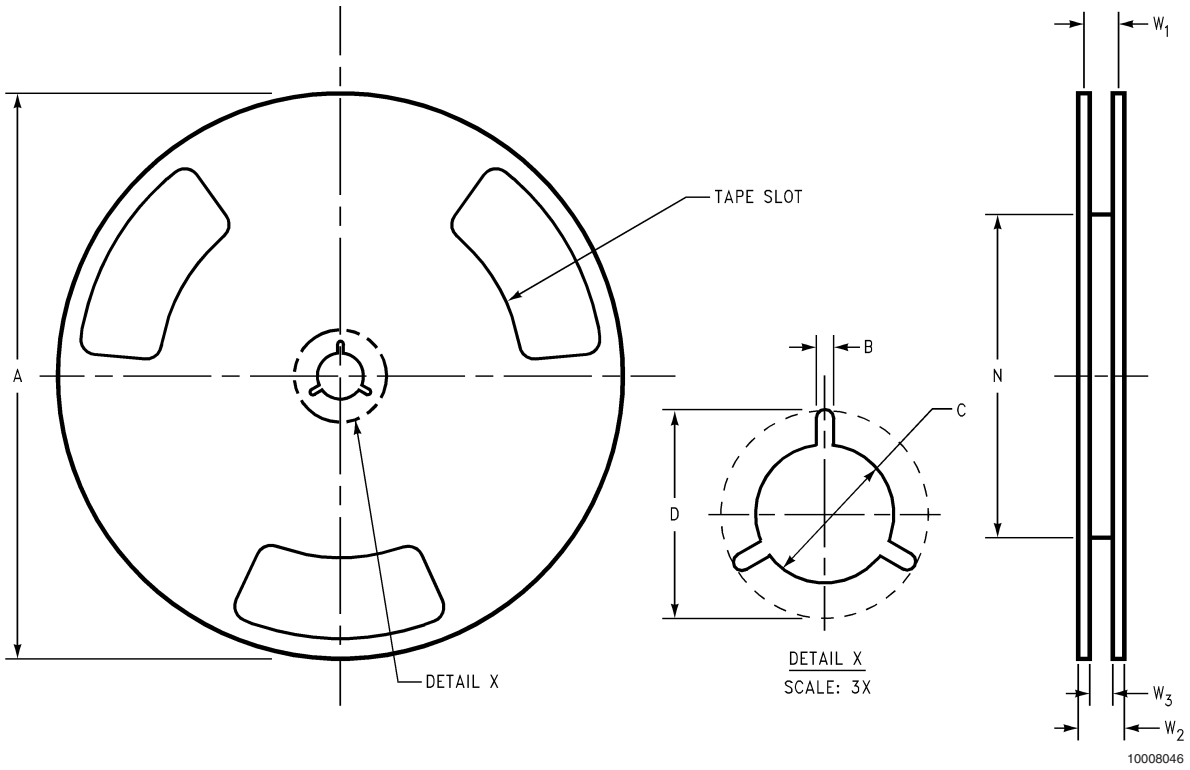
TAPE DIMENSIONS



8 mm	0.130 (3.3)	0.124 (3.15)	0.130 (3.3)	0.126 (3.2)	0.138 ±0.002 (3.5 ±0.05)	0.055 ±0.004 (1.4 ±0.11)	0.157 (4)	0.315 ±0.012 (8 ±0.3)
Tape Size	DIM A	DIM Ao	DIM B	DIM Bo	DIM F	DIM Ko	DIM P1	DIM W

SOT-23-5 Tape and Reel Specification (Continued)

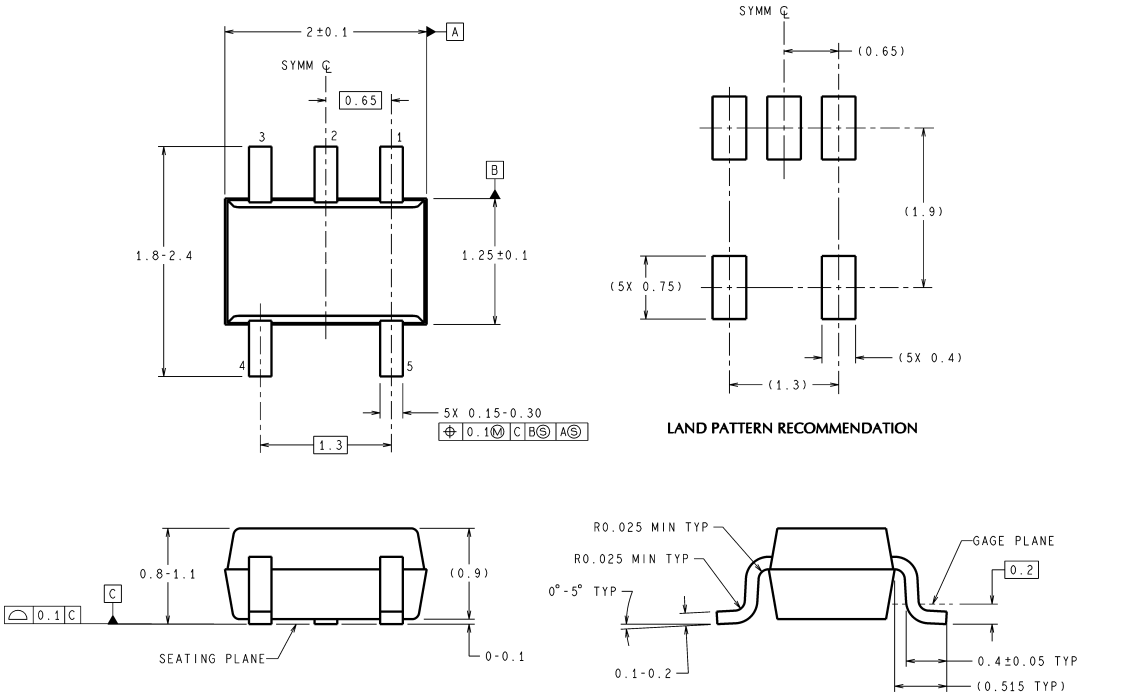
REEL DIMENSIONS



8 mm	7.00 330.00	0.059 1.50	0.512 13.00	0.795 20.20	2.165 55.00	0.331 + 0.059/–0.000 8.40 + 1.50/–0.00	0.567 14.40	W1+ 0.078/–0.039 W1 + 2.00/–1.00
Tape Size	A	B	C	D	N	W1	W2	W3

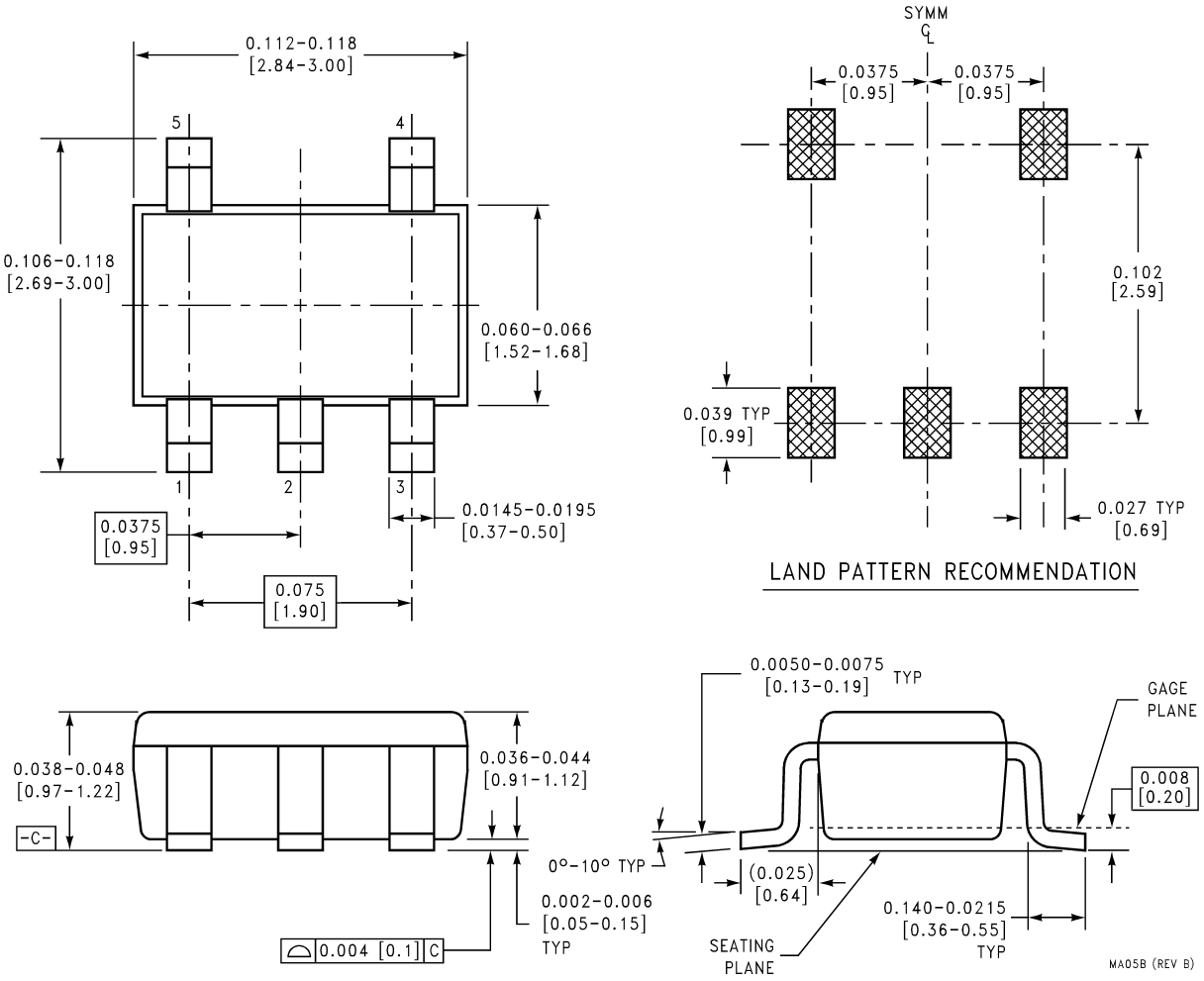
Physical Dimensions inches (millimeters)

unless otherwise noted



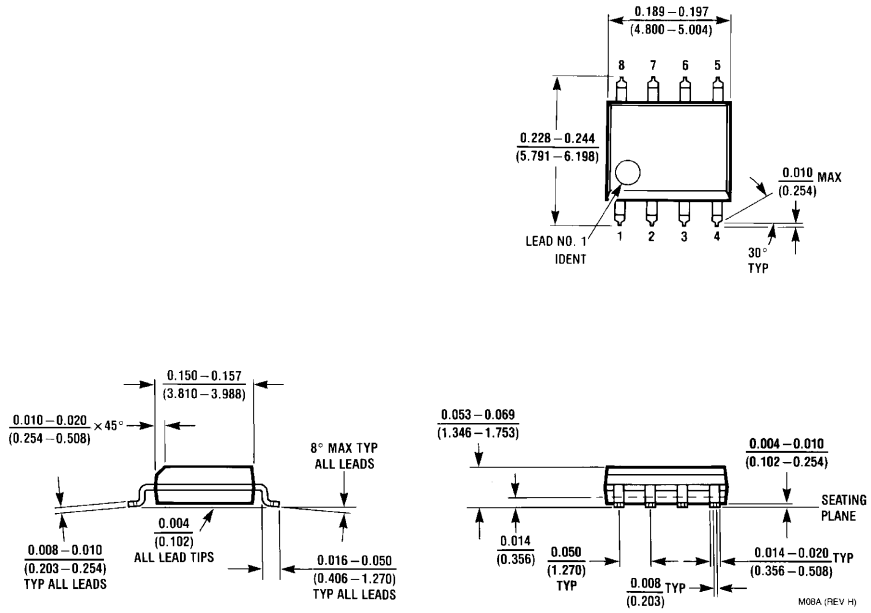
5-Pin SC70-5 Tape and Reel
NS Package Number MAA05A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

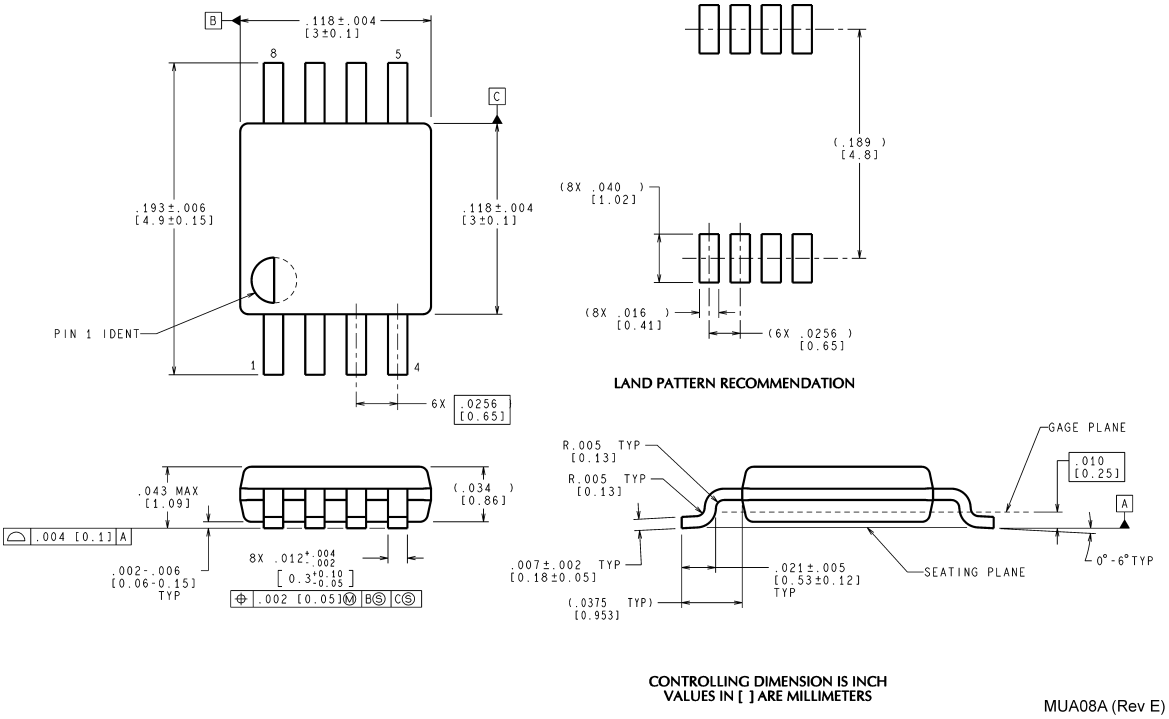


5-Pin SOT23-5 Tape and Reel
NS Package Number MA05B

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

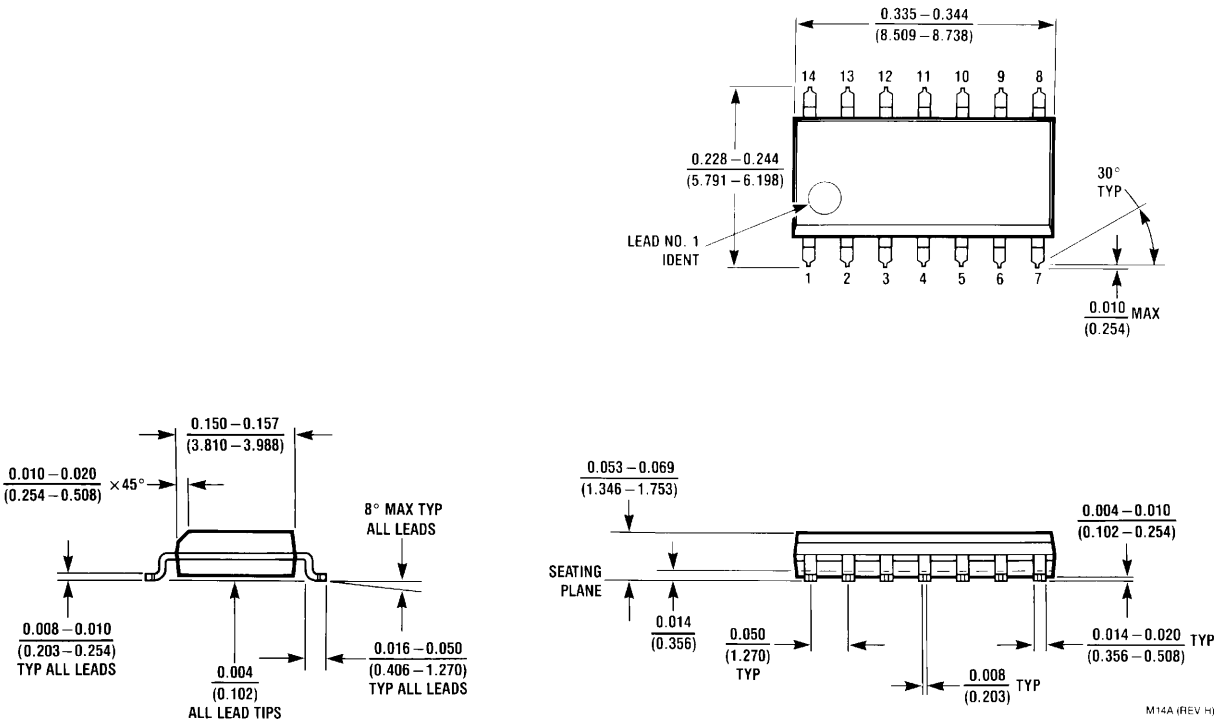


8-Pin Small Outline
NS Package Number M08A

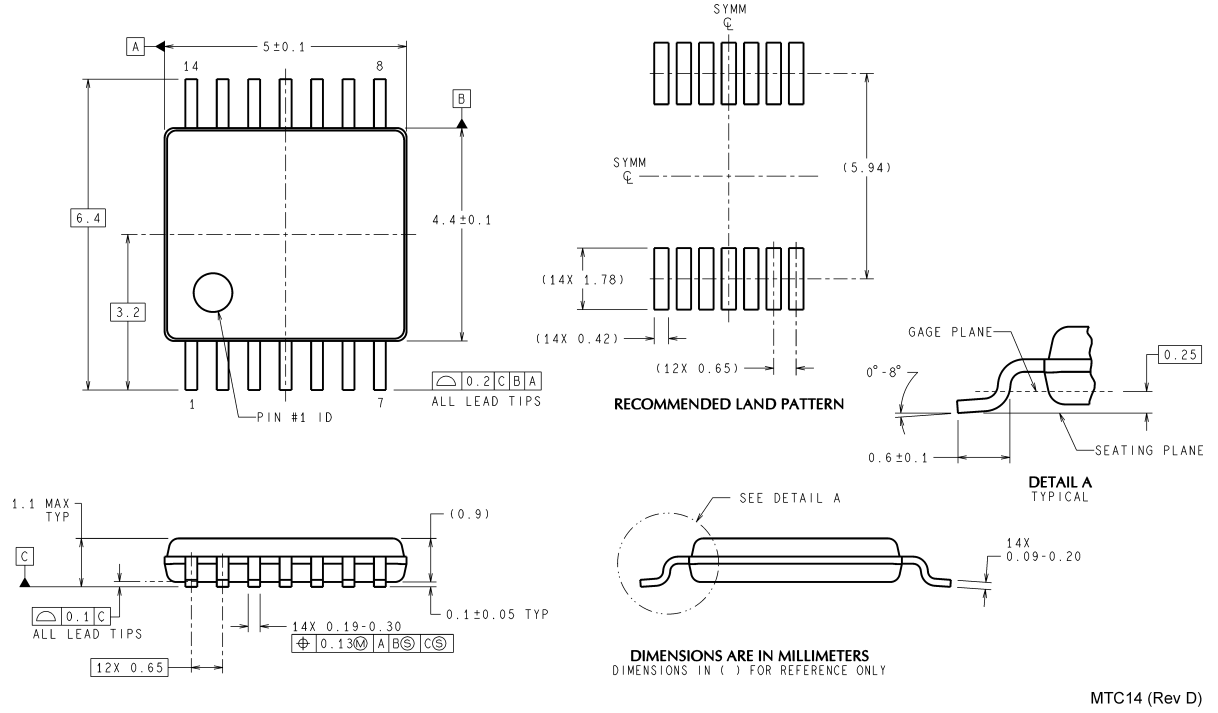


8-Pin MSOP
NS Package Number MUA08A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



14-Pin Small Outline
NS Package Number M14A



14-Pin TSSOP
NS Package Number MTC14

Notes

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT AND GENERAL COUNSEL OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

BANNED SUBSTANCE COMPLIANCE

National Semiconductor certifies that the products and packing materials meet the provisions of the Customer Products Stewardship Specification (CSP-9-111C2) and the Banned Substances and Materials of Interest Specification (CSP-9-111S2) and contain no ''Banned Substances'' as defined in CSP-9-111S2.

National Semiconductor
Americas Customer
Support Center
Email: new.feedback@nsc.com
Tel: 1-800-272-9959

www.national.com

National Semiconductor
Europe Customer Support Center
Fax: +49 (0) 180-530 85 86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 69 9508 6208
English Tel: +44 (0) 870 24 0 2171
Français Tel: +33 (0) 1 41 91 8790

National Semiconductor
Asia Pacific Customer
Support Center
Email: ap.support@nsc.com

National Semiconductor
Japan Customer Support Center
Fax: 81-3-5639-7507
Email: jpn.feedback@nsc.com
Tel: 81-3-5639-7560