

# LMV821 Single/ LMV822 Dual/ LMV824 Quad

## Low Voltage, Low Power, R-to-R Output, 5 MHz Op Amps

### General Description

The LMV821/LMV822/LMV824 bring performance and economy to low voltage / low power systems. With a 5 MHz unity-gain frequency and a guaranteed 1.4 V/ $\mu$ s slew rate, the quiescent current is only 220  $\mu$ A/amplifier (2.7 V). They provide rail-to-rail (R-to-R) output swing into heavy loads (600  $\Omega$  Guarantees). The input common-mode voltage range includes ground, and the maximum input offset voltage is 3.5mV (Guaranteed). They are also capable of comfortably driving large capacitive loads (refer to the application notes section).

The LMV821 (single) is available in the ultra tiny SC70-5 package, which is about half the size of the previous title holder, the SOT23-5.

Overall, the LMV821/LMV822/LMV824 (Single/Dual/Quad) are low voltage, low power, performance op amps, that can be designed into a wide range of applications, at an economical price.

### Features

(For Typical, 5 V Supply Values; Unless Otherwise Noted)

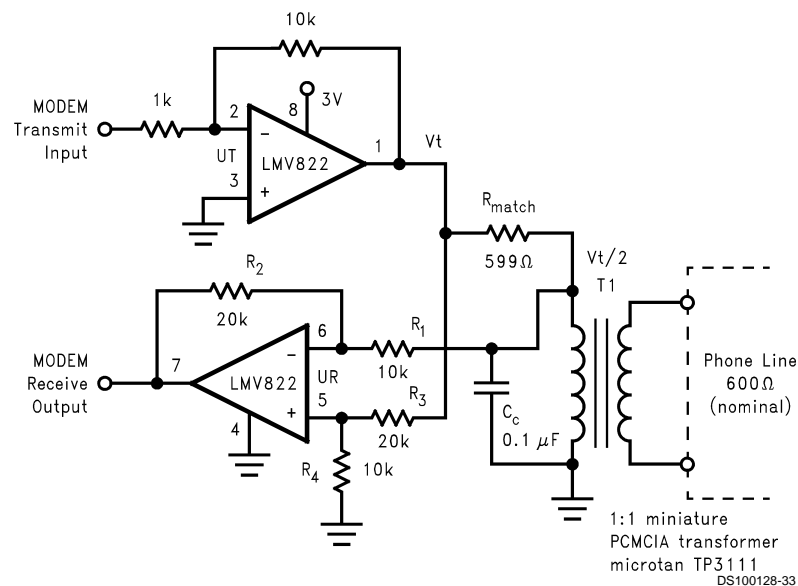
- Ultra Tiny, SC70-5 Package                      2.0 x 2.0 x 1.0 mm

- Guaranteed 2.5 V, 2.7 V and 5 V Performance
- Maximum VOS    3.5 mV (Guaranteed)
- VOS Temp. Drift    1  $\mu$ V/ $^{\circ}$  C
- GBW product @ 2.7 V    5 MHz
- $I_{\text{Supply}}$  @ 2.7 V    220  $\mu$ A/Amplifier
- Minimum SR    1.4 V/us (Guaranteed)
- CMRR    90 dB
- PSRR    85 dB
- Rail-to-Rail (R-to-R) Output Swing
  - @600  $\Omega$  Load    160 mV from rail
  - @10 k $\Omega$  Load    55 mV from rail
- $V_{\text{CM}}$  @ 5 V    -0.3 V to 4.3 V
- Stable with High Capacitive Loads (Refer to Application Section)

### Applications

- Cordless Phones
- Cellular Phones
- Laptops
- PDAs
- PCMCIA

### Telephone-line Transceiver for a PCMCIA Modem Card



## Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

ESD Tolerance (Note 2)	
Machine Model	100V
Human Body Model	
LMV822/824	2000V
LMV821	1500V
Differential Input Voltage	± Supply Voltage
Supply Voltage (V <sup>+</sup> -V <sup>-</sup> )	5.5V
Output Short Circuit to V <sup>+</sup> (Note 3)	
Output Short Circuit to V <sup>-</sup> (Note 3)	
Soldering Information	
Infrared or Convection (20 sec)	235°C
Storage Temperature Range	-65°C to 150°C
Junction Temperature (Note 4)	150°C

## Operating Ratings (Note 1)

Supply Voltage	2.5V to 5.5V
Temperature Range	
LMV821, LMV822, LMV824	-40°C ≤ T <sub>J</sub> ≤ 85°C
Thermal Resistance (θ <sub>JA</sub> )	
Ultra Tiny SC70-5 Package	440 °C/W
5-Pin Surface Mount	
Tiny SOT23-5 Package	265 °C/W
5-Pin Surface Mount	
SO Package, 8-Pin Surface Mount	190 °C/W
MSOP Package, 8-Pin Mini Surface Mount	235 °C/W
SO Package, 14-Pin Surface Mount	145 °C/W
TSSOP Package, 14-Pin	155 °C/W

## 2.7V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T<sub>J</sub> = 25°C. V<sup>+</sup> = 2.7V, V<sup>-</sup> = 0V, V<sub>CM</sub> = 1.0V, V<sub>O</sub> = 1.35V and R<sub>L</sub> > 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Typ (Note 5)	LMV821/822/824 Limit (Note 6)	Units
V <sub>OS</sub>	Input Offset Voltage		1	3.5 <b>4</b>	mV max
TCV <sub>OS</sub>	Input Offset Voltage Average Drift		1		µV/°C
I <sub>B</sub>	Input Bias Current		30	90 <b>140</b>	nA max
I <sub>OS</sub>	Input Offset Current		0.5	30 <b>50</b>	nA max
CMRR	Common Mode Rejection Ratio	0V ≤ V <sub>CM</sub> ≤ 1.7V	85	70 <b>68</b>	dB min
+PSRR	Positive Power Supply Rejection Ratio	1.7V ≤ V <sup>+</sup> ≤ 4V, V <sup>-</sup> = 1V, V <sub>O</sub> = 0V, V <sub>CM</sub> = 0V	85	75 <b>70</b>	dB min
-PSRR	Negative Power Supply Rejection Ratio	-1.0V ≤ V <sup>-</sup> ≤ -3.3V, V <sup>+</sup> = 1.7V, V <sub>O</sub> = 0V, V <sub>CM</sub> = 0V	85	73 <b>70</b>	dB min
V <sub>CM</sub>	Input Common-Mode Voltage Range	For CMRR ≥ 50dB	-0.3	-0.2	V max
			2.0	1.9	V min
A <sub>V</sub>	Large Signal Voltage Gain	Sourcing, R <sub>L</sub> = 600Ω to 1.35V, V <sub>O</sub> = 1.35V to 2.2V	100	90 <b>85</b>	dB min
			90	85 <b>80</b>	dB min
		Sinking, R <sub>L</sub> = 600Ω to 1.35V, V <sub>O</sub> = 1.35V to 0.5V	100	95 <b>90</b>	dB min
			95	90 <b>85</b>	dB min

## 2.7V DC Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for  $T_J = 25^\circ\text{C}$ .  $V^+ = 2.7\text{V}$ ,  $V^- = 0\text{V}$ ,  $V_{\text{CM}} = 1.0\text{V}$ ,  $V_O = 1.35\text{V}$  and  $R_L > 1\text{M}\Omega$ . **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Typ (Note 5)	LMV821/822/824 Limit (Note 6)	Units
$V_O$	Output Swing	$V^+ = 2.7\text{V}$ , $R_L = 600\Omega$ to $1.35\text{V}$	2.58	2.50 <b>2.40</b>	V min
			0.13	0.20 <b>0.30</b>	V max
		$V^+ = 2.7\text{V}$ , $R_L = 2\text{k}\Omega$ to $1.35\text{V}$	2.66	2.60 <b>2.50</b>	V min
			0.08	0.120 <b>0.200</b>	V max
$I_O$	Output Current	Sourcing, $V_O = 0\text{V}$	16	12	mA min
		Sinking, $V_O = 2.7\text{V}$	26	12	mA min
$I_S$	Supply Current	LMV821 (Single)	0.22	0.3 <b>0.5</b>	mA max
		LMV822 (Dual)	0.45	0.6 <b>0.8</b>	mA max
		LMV824 (Quad)	0.72	1.0 <b>1.2</b>	mA max

## 2.5V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for  $T_J = 25^\circ\text{C}$ .  $V^+ = 2.5\text{V}$ ,  $V^- = 0\text{V}$ ,  $V_{\text{CM}} = 1.0\text{V}$ ,  $V_O = 1.25\text{V}$  and  $R_L > 1\text{M}\Omega$ . **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Typ (Note 5)	LMV821/822/824 Limit (Note 6)	Units
$V_{\text{OS}}$	Input Offset Voltage		1	3.5 <b>4</b>	mV max
$V_O$	Output Swing	$V^+ = 2.5\text{V}$ , $R_L = 600\Omega$ to $1.25\text{V}$	2.37	2.30 <b>2.20</b>	V min
			0.13	0.20 <b>0.30</b>	V max
		$V^+ = 2.5\text{V}$ , $R_L = 2\text{k}\Omega$ to $1.25\text{V}$	2.46	2.40 <b>2.30</b>	V min
			0.08	0.12 <b>0.20</b>	V max

## 2.7V AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for  $T_J = 25^\circ\text{C}$ .  $V^+ = 2.7\text{V}$ ,  $V^- = 0\text{V}$ ,  $V_{\text{CM}} = 1.0\text{V}$ ,  $V_O = 1.35\text{V}$  and  $R_L > 1\text{M}\Omega$ . **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LMV821/822/824 Limit (Note 6)	Units
SR	Slew Rate	(Note 7)	1.5		V/ $\mu\text{s}$
GBW	Gain-Bandwidth Product		5		MHz
$\Phi_m$	Phase Margin		61		Deg.
$G_m$	Gain Margin		10		dB
	Amp-to-Amp Isolation	(Note 8)	135		dB
$e_n$	Input-Related Voltage Noise	$f = 1\text{kHz}$ , $V_{\text{CM}} = 1\text{V}$	28		$\frac{\text{nV}}{\sqrt{\text{Hz}}}$

## 2.7V AC Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for  $T_J = 25^\circ\text{C}$ .  $V^+ = 2.7\text{V}$ ,  $V^- = 0\text{V}$ ,  $V_{\text{CM}} = 1.0\text{V}$ ,  $V_O = 1.35\text{V}$  and  $R_L > 1\text{M}\Omega$ . **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LMV821/822/824 Limit (Note 6)	Units
$i_n$	Input-Referred Current Noise	$f = 1\text{ kHz}$	0.1		$\frac{\text{pA}}{\sqrt{\text{Hz}}}$
THD	Total Harmonic Distortion	$f = 1\text{ kHz}$ , $A_V = -2$ , $R_L = 10\text{ k}\Omega$ , $V_O = 4.1\text{ V}_{\text{PP}}$	0.01		%

## 5V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for  $T_J = 25^\circ\text{C}$ .  $V^+ = 5\text{V}$ ,  $V^- = 0\text{V}$ ,  $V_{\text{CM}} = 2.0\text{V}$ ,  $V_O = 2.5\text{V}$  and  $R_L > 1\text{M}\Omega$ . **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Typ (Note 5)	LMV821/822/824 Limit (Note 6)	Units
$V_{\text{OS}}$	Input Offset Voltage		1	3.5 <b>4.0</b>	mV max
$\text{TCV}_{\text{OS}}$	Input Offset Voltage Average Drift		1		$\mu\text{V}/^\circ\text{C}$
$I_B$	Input Bias Current		40	100 <b>150</b>	nA max
$I_{\text{OS}}$	Input Offset Current		0.5	30 <b>50</b>	nA max
CMRR	Common Mode Rejection Ratio	$0\text{V} \leq V_{\text{CM}} \leq 4.0\text{V}$	90	72 <b>70</b>	dB min
+PSRR	Positive Power Supply Rejection Ratio	$1.7\text{V} \leq V^+ \leq 4\text{V}$ , $V^- = 1\text{V}$ , $V_O = 0\text{V}$ , $V_{\text{CM}} = 0\text{V}$	85	75 <b>70</b>	dB min
-PSRR	Negative Power Supply Rejection Ratio	$-1.0\text{V} \leq V^- \leq -3.3\text{V}$ , $V^+ = 1.7\text{V}$ , $V_O = 0\text{V}$ , $V_{\text{CM}} = 0\text{V}$	85	73 <b>70</b>	dB min
$V_{\text{CM}}$	Input Common-Mode Voltage Range	For CMRR $\geq 50\text{dB}$	-0.3 4.3	-0.2 4.2	V max V min
$A_V$	Large Signal Voltage Gain	Sourcing, $R_L = 600\Omega$ to $2.5\text{V}$ , $V_O = 2.5$ to $4.5\text{V}$	105	95 <b>90</b>	dB min
		Sinking, $R_L = 600\Omega$ to $2.5\text{V}$ , $V_O = 2.5$ to $0.5\text{V}$	105	95 <b>90</b>	dB min
		Sourcing, $R_L = 2\text{k}\Omega$ to $2.5\text{V}$ , $V_O = 2.5$ to $4.5\text{V}$	105	95 <b>90</b>	dB min
		Sinking, $R_L = 2\text{k}\Omega$ to $2.5$ , $V_O = 2.5$ to $0.5\text{V}$	105	95 <b>90</b>	dB min
$V_O$	Output Swing	$V^+ = 5\text{V}$ , $R_L = 600\Omega$ to $2.5\text{V}$	4.84 0.17	4.75 0.250 <b>4.70</b> <b>.30</b>	V min V max
		$V^+ = 5\text{V}$ , $R_L = 2\text{k}\Omega$ to $2.5\text{V}$	4.90 0.10	4.85 0.15 <b>4.80</b> <b>0.20</b>	V min V max

## 5V DC Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for  $T_J = 25^\circ\text{C}$ .  $V^+ = 5\text{V}$ ,  $V^- = 0\text{V}$ ,  $V_{\text{CM}} = 2.0\text{V}$ ,  $V_O = 2.5\text{V}$  and  $R_L > 1\text{M}\Omega$ .

**Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Typ (Note 5)	LMV821/822/824 Limit (Note 6)	Units
$I_O$	Output Current	Sourcing, $V_O = 0\text{V}$	45	20 <b>15</b>	mA min
		Sinking, $V_O = 5\text{V}$	40	20 <b>15</b>	mA min
$I_S$	Supply Current	LMV821 (Single)	0.30	0.4 <b>0.6</b>	mA max
		LMV822 (Dual)	0.5	0.7 <b>0.9</b>	mA max
		LMV824 (Quad)	1.0	1.3 <b>1.5</b>	mA max

## 5V AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for  $T_J = 25^\circ\text{C}$ .  $V^+ = 5\text{V}$ ,  $V^- = 0\text{V}$ ,  $V_{\text{CM}} = 2\text{V}$ ,  $V_O = 2.5\text{V}$  and  $R_L > 1\text{M}\Omega$ .

**Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LMV821/822/824 Limit (Note 6)	Units
SR	Slew Rate	(Note 7)	2.0	1.4	V/ $\mu\text{s}$ min
GBW	Gain-Bandwidth Product		5.6		MHz
$\Phi_m$	Phase Margin		67		Deg.
$G_m$	Gain Margin		15		dB
	Amp-to-Amp Isolation	(Note 8)	135		dB
$e_n$	Input-Related Voltage Noise	$f = 1\text{kHz}$ , $V_{\text{CM}} = 1\text{V}$	24		$\frac{\text{nV}}{\sqrt{\text{Hz}}}$
$i_n$	Input-Referred Current Noise	$f = 1\text{kHz}$	0.25		$\frac{\text{pA}}{\sqrt{\text{Hz}}}$
THD	Total Harmonic Distortion	$f = 1\text{kHz}$ , $A_V = -2$ , $R_L = 10\text{k}\Omega$ , $V_O = 4.1\text{V}_{\text{PP}}$	0.01		%

**Note 1:** Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

**Note 2:** Human body model, 1.5 k $\Omega$  in series with 100 pF. Machine model, 200 $\Omega$  in series with 100 pF.

**Note 3:** Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150 $^\circ\text{C}$ . Output currents in excess of 45 mA over long term may adversely affect reliability.

**Note 4:** The maximum power dissipation is a function of  $T_{\text{J(max)}}$ ,  $\theta_{\text{JA}}$ , and  $T_A$ . The maximum allowable power dissipation at any ambient temperature is  $P_D = (T_{\text{J(max)}} - T_A) / \theta_{\text{JA}}$ . All numbers apply for packages soldered directly into a PC board.

**Note 5:** Typical Values represent the most likely parametric norm.

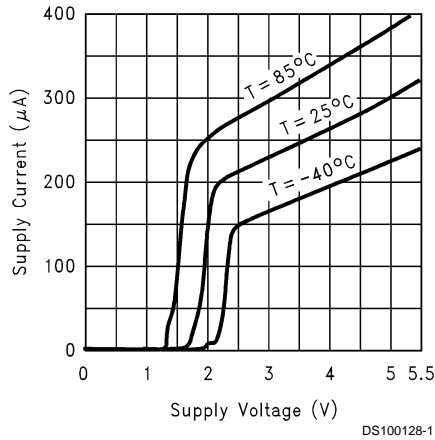
**Note 6:** All limits are guaranteed by testing or statistical analysis.

**Note 7:**  $V^+ = 5\text{V}$ . Connected as voltage follower with 3V step input. Number specified is the slower of the positive and negative slew rates.

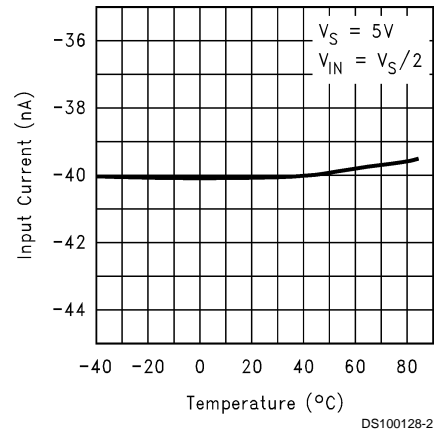
**Note 8:** Input referred,  $V^+ = 5\text{V}$  and  $R_L = 100\text{k}\Omega$  connected to 2.5V. Each amp excited in turn with 1 kHz to produce  $V_O = 3\text{V}_{\text{PP}}$ .

**Typical Performance Characteristics** Unless otherwise specified,  $V_S = +5V$ , single supply,  $T_A = 25^\circ C$ .

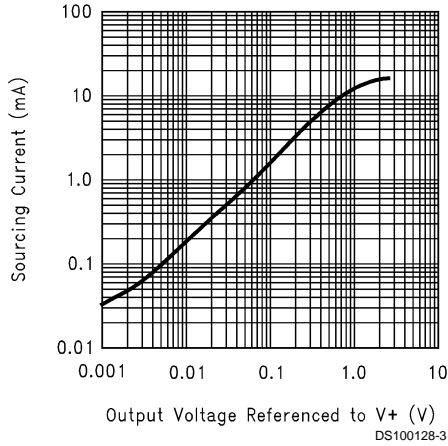
**Supply Current vs. Supply Voltage (LMV821)**



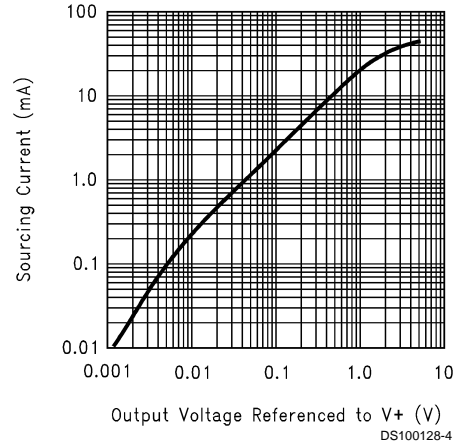
**Input Current vs. Temperature**



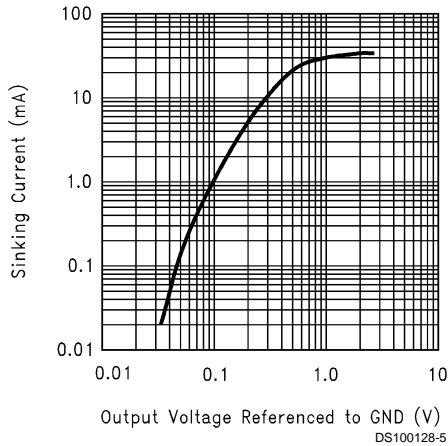
**Sourcing Current vs. Output Voltage ( $V_S = 2.7V$ )**



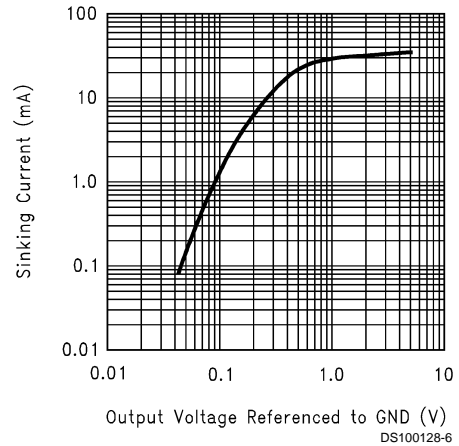
**Sourcing Current vs. Output Voltage ( $V_S = 5V$ )**



**Sinking Current vs. Output Voltage ( $V_S = 2.7V$ )**



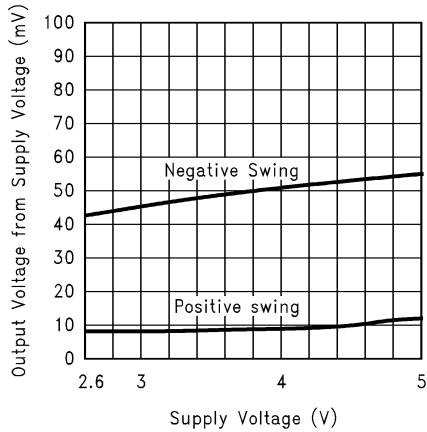
**Sinking Current vs. Output Voltage ( $V_S = 5V$ )**



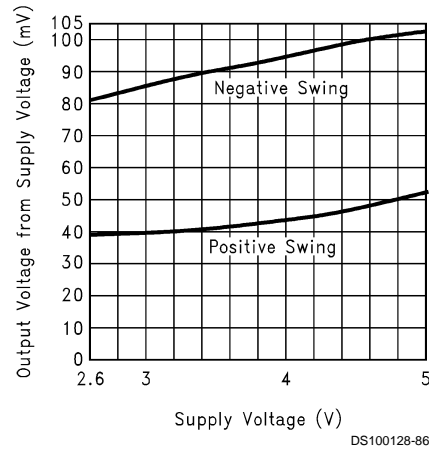
## Typical Performance Characteristics

Unless otherwise specified,  $V_S = +5V$ , single supply,  $T_A = 25^\circ C$ . (Continued)

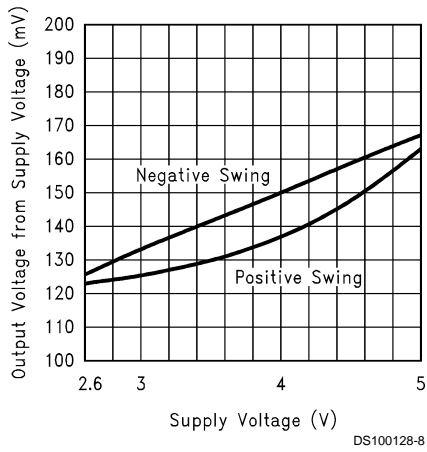
**Output Voltage Swing vs. Supply Voltage ( $R_L = 10k\Omega$ )**



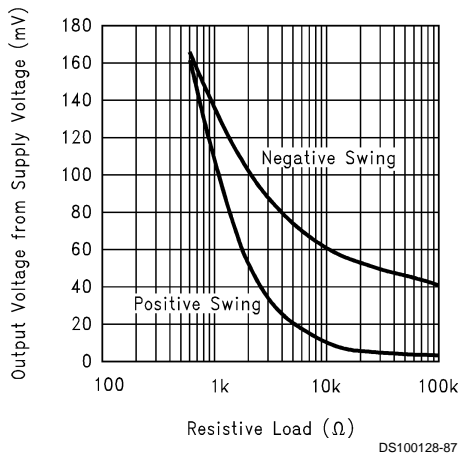
**Output Voltage Swing vs. Supply Voltage ( $R_L = 2k\Omega$ )**



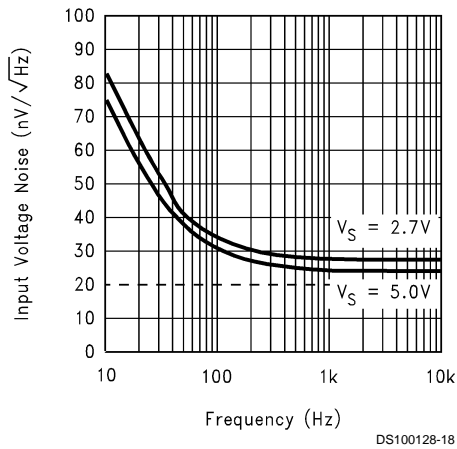
**Output Voltage Swing vs. Supply Voltage ( $R_L = 600\Omega$ )**



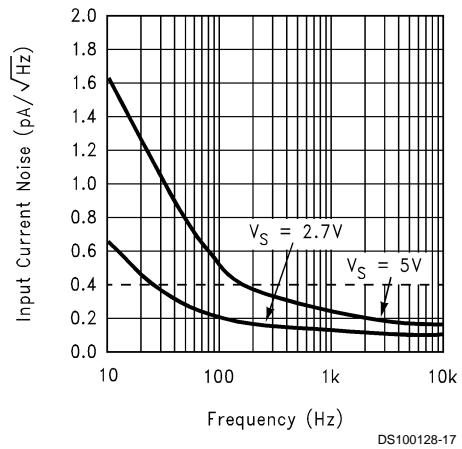
**Output Voltage Swing vs. Load Resistance**



**Input Voltage Noise vs. Frequency**

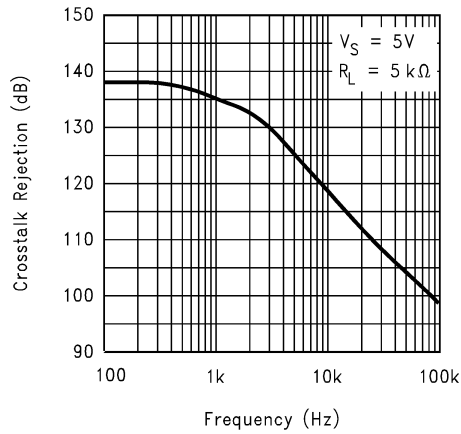


**Input Current Noise vs. Frequency**

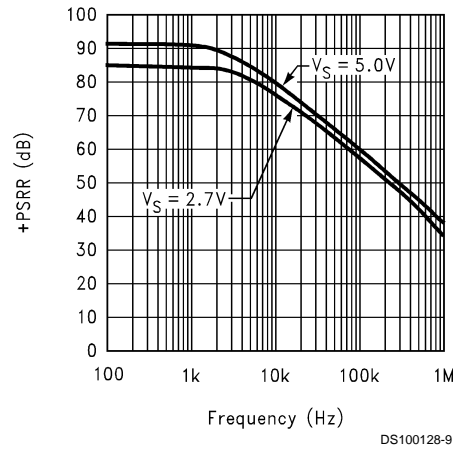


**Typical Performance Characteristics** Unless otherwise specified,  $V_S = +5V$ , single supply,  $T_A = 25^\circ C$ . (Continued)

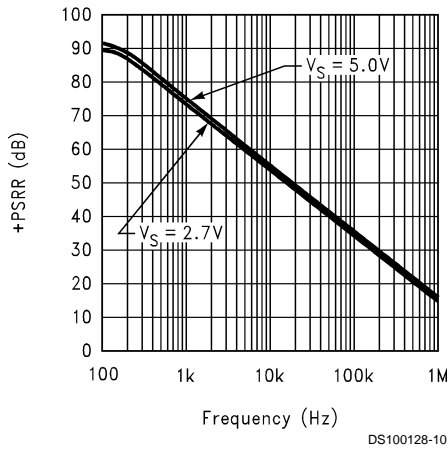
**Crosstalk Rejection vs. Frequency**



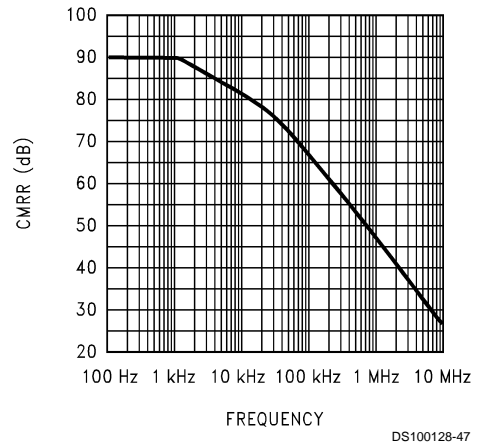
**+PSRR vs. Frequency**



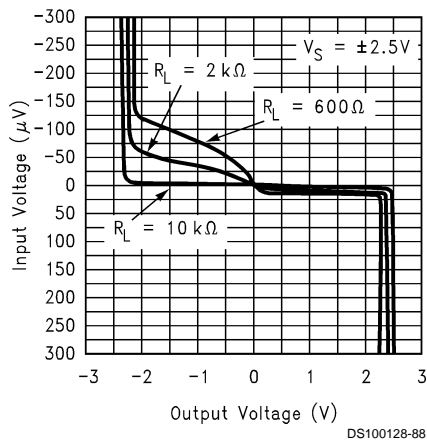
**-PSRR vs. Frequency**



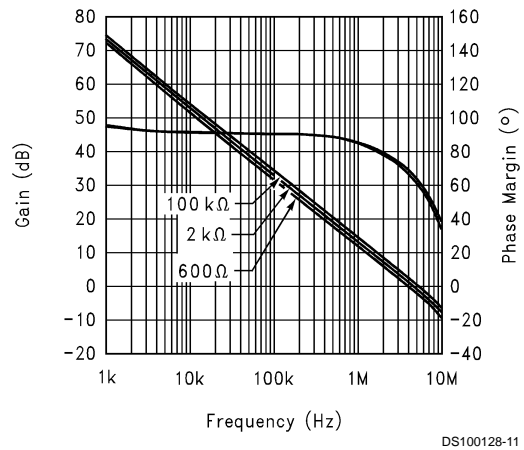
**CMRR vs. Frequency**



**Input Voltage vs. Output Voltage**



**Gain and Phase Margin vs. Frequency**  
( $R_L = 100k\Omega, 2k\Omega, 600\Omega$ ) 2.7V



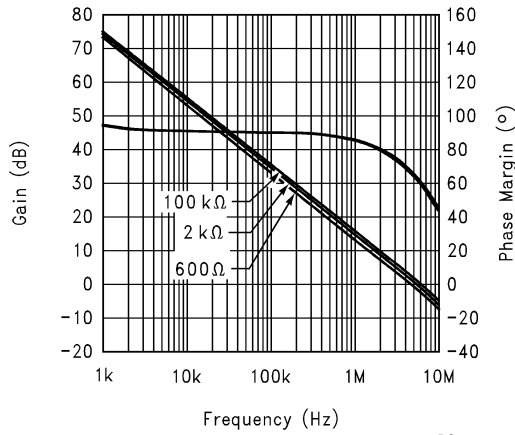


## Typical Performance Characteristics

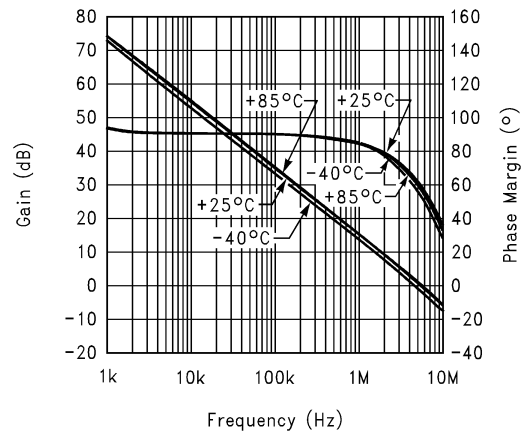
Unless otherwise specified,  $V_S = +5V$ , single supply,

$T_A = 25^\circ C$ . (Continued)

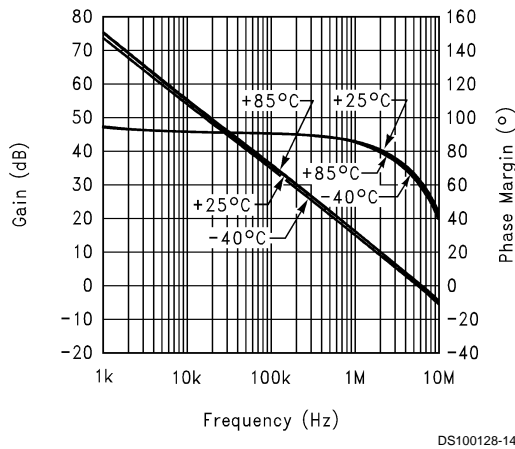
**Gain and Phase Margin vs. Frequency**  
( $R_L = 100k\Omega, 2k\Omega, 600\Omega$ ) 5V



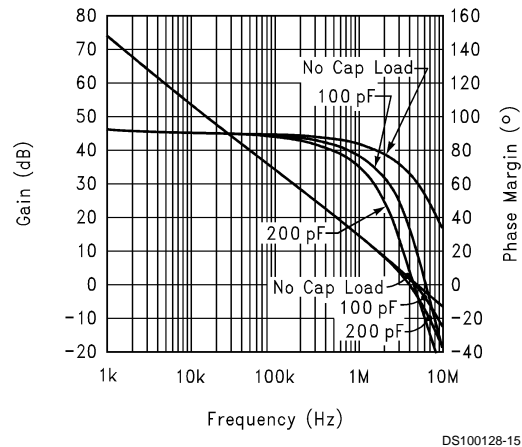
**Gain and Phase Margin vs. Frequency**  
(Temp.= 25, -40, 85°C,  $R_L = 10k\Omega$ ) 2.7V



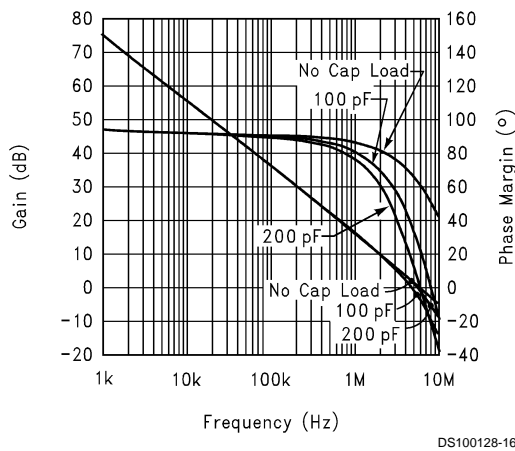
**Gain and Phase Margin vs. Frequency**  
(Temp.= 25, -40, 85°C,  $R_L = 10k\Omega$ ) 5V



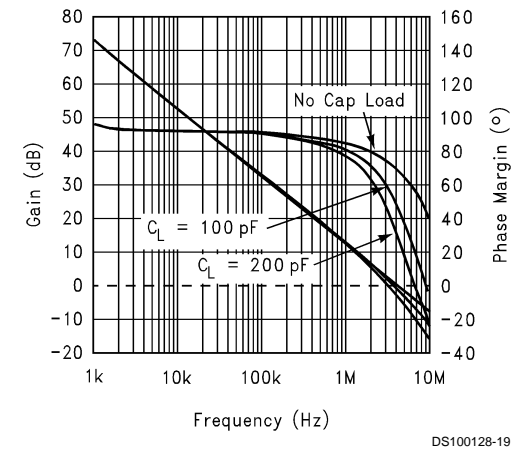
**Gain and Phase Margin vs. Frequency**  
( $C_L = 100pF, 200pF, 0pF, R_L = 10k\Omega$ ) 2.7V



**Gain and Phase Margin vs. Frequency**  
( $C_L = 100pF, 200pF, 0pF, R_L = 10k\Omega$ ) 5V

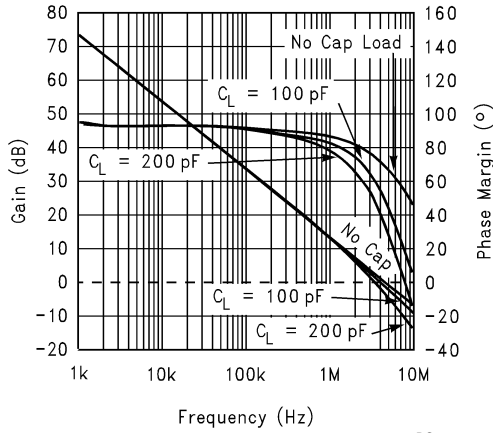


**Gain and Phase Margin vs. Frequency** ( $C_L = 100pF, 200pF, 0pF, R_L = 600\Omega$ ) 2.7V



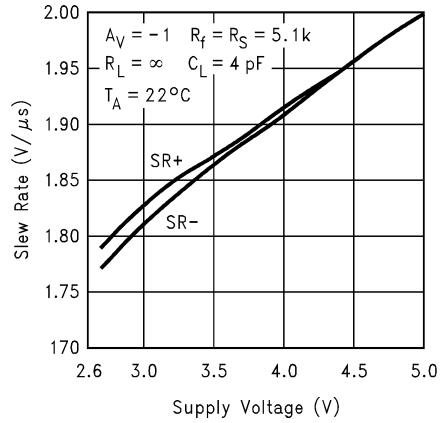
**Typical Performance Characteristics** Unless otherwise specified,  $V_S = +5V$ , single supply,  $T_A = 25^\circ C$ . (Continued)

**Gain and Phase Margin vs. Frequency**  
 $(C_L = 100pF, 200pF, 0pF, R_L = 600\Omega) 5V$



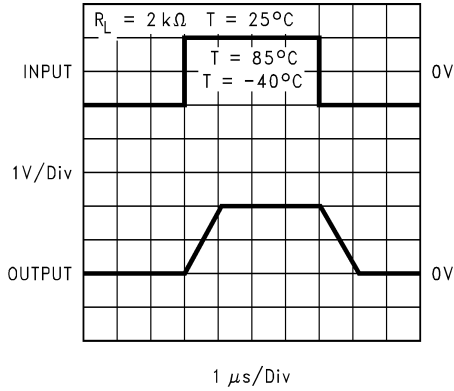
DS100128-20

**Slew Rate vs. Supply Voltage**



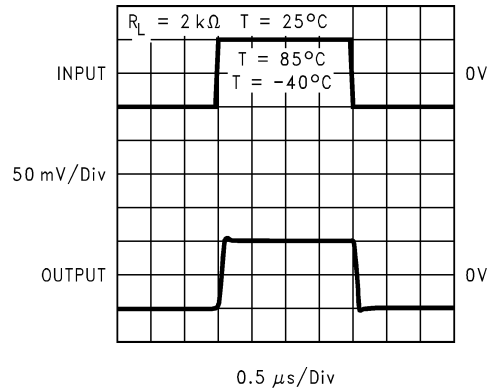
DS100128-62

**Non-Inverting Large Signal Pulse Response**



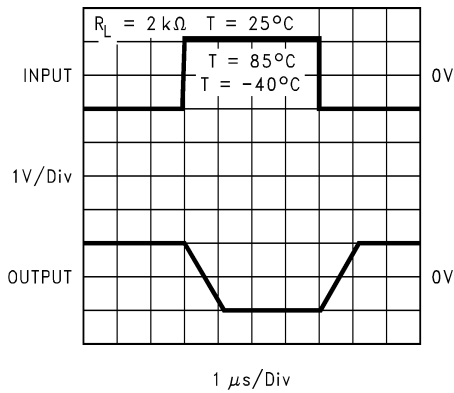
DS100128-21

**Non-Inverting Small Signal Pulse Response**



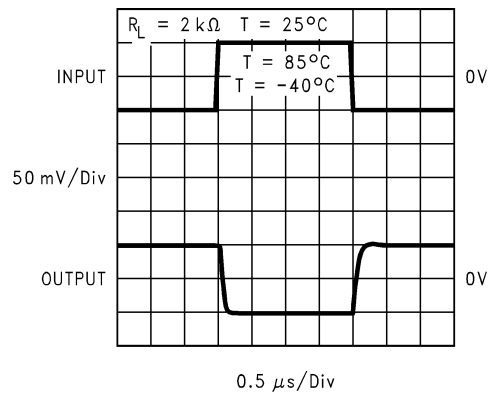
DS100128-24

**Inverting Large Signal Pulse Response**



DS100128-27

**Inverting Small Signal Pulse Response**



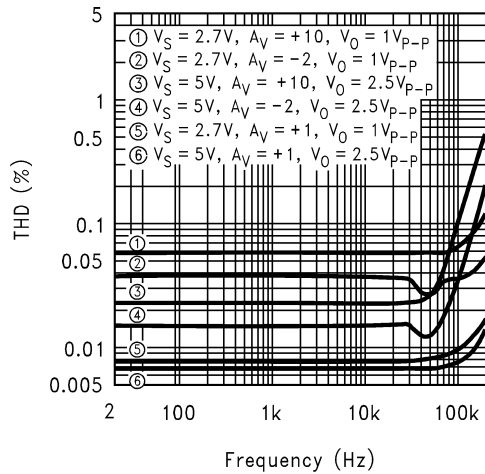
DS100128-30

## Typical Performance Characteristics

Unless otherwise specified,  $V_S = +5V$ , single supply,

$T_A = 25^\circ C$ . (Continued)

### THD vs. Frequency



DS100128-82

### APPLICATION NOTE

This application note is divided into two sections: design considerations and Application Circuits.

#### 1.0 Design Considerations

This section covers the following design considerations:

1. Frequency and Phase Response Considerations
2. Unity-Gain Pulse Response Considerations
3. Input Bias Current Considerations

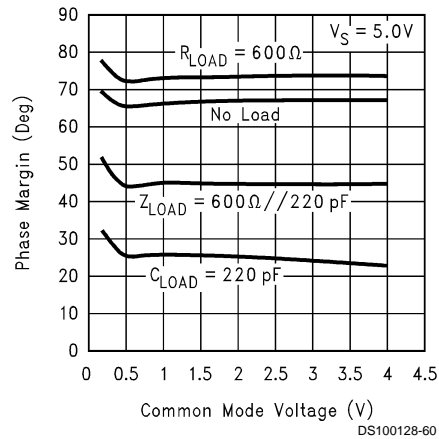
#### 1.1 Frequency and Phase Response Considerations

The relationship between open-loop frequency response and open-loop phase response determines the closed-loop stability performance (negative feedback). The open-loop phase response causes the feedback signal to shift towards becoming positive feedback, thus becoming unstable. The further the output phase angle is from the input phase angle, the more stable the negative feedback will operate. Phase Margin ( $\phi_m$ ) specifies this output-to-input phase relationship at the unity-gain crossover point. Zero degrees of phase-margin means that the input and output are completely in phase with each other and will sustain oscillation at the unity-gain frequency.

The AC tables show  $\phi_m$  for a no load condition. But  $\phi_m$  changes with load. The Gain and Phase margin vs Frequency plots in the curve section can be used to graphically determine the  $\phi_m$  for various loaded conditions. To do this, examine the phase angle portion of the plot, find the phase margin point at the unity-gain frequency, and determine how far this point is from zero degree of phase-margin. The larger the phase-margin, the more stable the circuit operation.

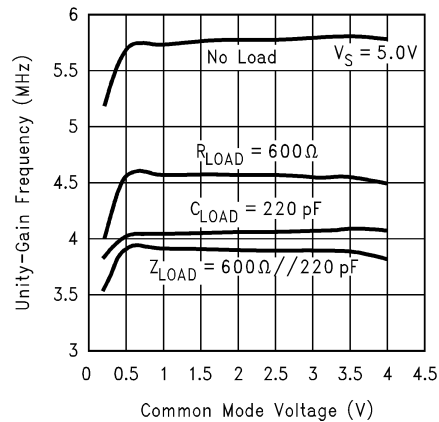
The bandwidth is also affected by load. The graphs of Figure 1 and Figure 2 provide a quick look at how various loads affect the  $\phi_m$  and the bandwidth of the LMV821/822/824 family. These graphs show capacitive loads reducing both  $\phi_m$  and bandwidth, while resistive loads reduce the bandwidth but increase the  $\phi_m$ . Notice how a  $600\Omega$  resistor can be added in parallel with 220 picofarads capacitance, to increase the  $\phi_m$   $20^\circ$  (approx.), but at the price of about a 100 kHz of bandwidth.

Overall, the LMV821/822/824 family provides good stability for loaded condition.



DS100128-60

FIGURE 1. Phase Margin vs Common Mode Voltage for Various Loads

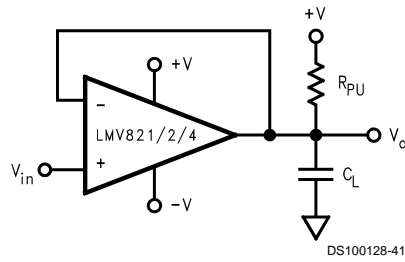


DS100128-61

FIGURE 2. Unity-Gain Frequency vs Common Mode Voltage for Various Loads

### 1.2 Unity Gain Pulse Response Considerations

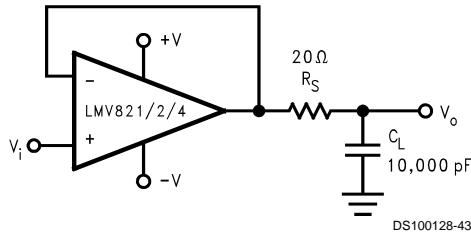
A pull-up resistor is well suited for increasing unity-gain, pulse response stability. For example, a 600 Ω pull-up resistor reduces the overshoot voltage by about 50%, when driving a 220 pF load. *Figure 3* shows how to implement the pull-up resistor for more pulse response stability.



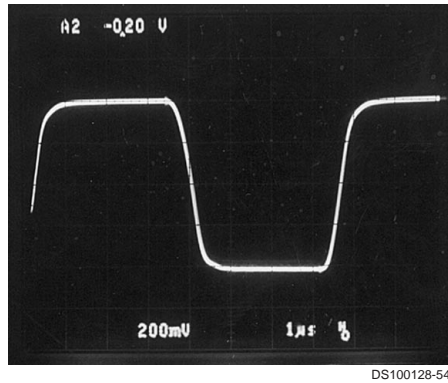
**FIGURE 3. Using a Pull-up Resistor at the Output for Stabilizing Capacitive Loads**

Higher capacitances can be driven by decreasing the value of the pull-up resistor, but its value shouldn't be reduced beyond the sinking capability of the part. An alternate approach is to use an isolation resistor as illustrated in *Figure 4*.

*Figure 5* shows the resulting pulse response from a LMV824, while driving a 10,000pF load through a 20 Ω isolation resistor.



**FIGURE 4. Using an Isolation Resistor to Drive Heavy Capacitive Loads**

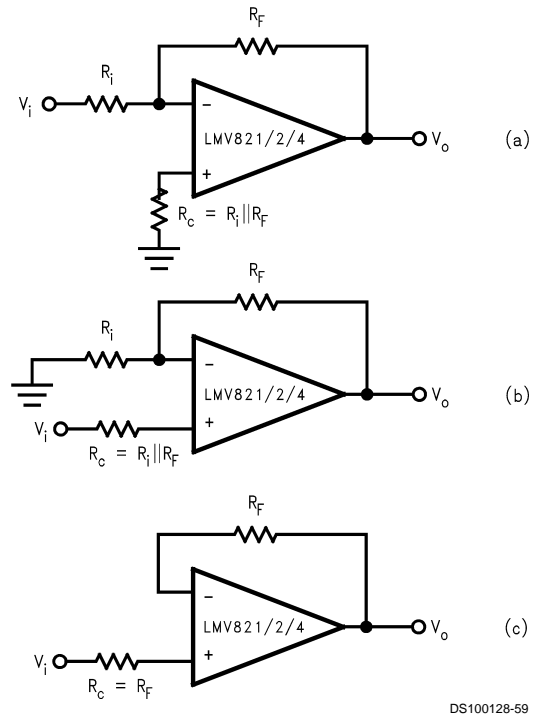


**FIGURE 5. Pulse Response per Figure 4**

### 1.3 Input Bias Current Consideration

Input bias current ( $I_B$ ) can develop a somewhat significant offset voltage. This offset is primarily due to  $I_B$  flowing through the negative feedback resistor,  $R_F$ . For example, if  $I_B$  is 90nA (max room) and  $R_F$  is 100 kΩ, then an offset of 9 mV will be developed ( $V_{OS} = I_B \times R_F$ ). Using a compensation resistor ( $R_C$ ), as shown in *Figure 6*, cancels out this affect. But the

input offset current ( $I_{OS}$ ) will still contribute to an offset voltage in the same manner - typically 0.05 mV at room temp.



**FIGURE 6. Canceling the Voltage Offset Effect of Input Bias Current**

## 2.0 APPLICATION CIRCUITS

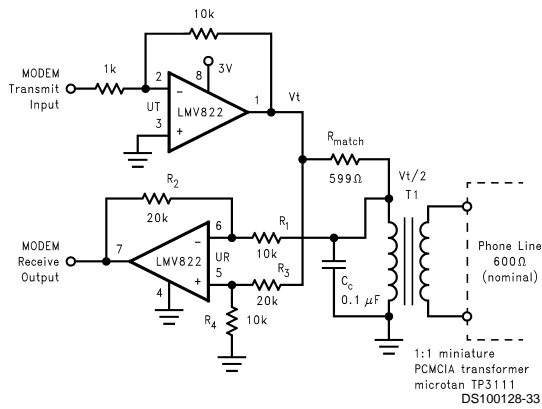
This section covers the following application circuits:

1. Telephone-Line Transceiver
2. "Simple" Mixer (Amplitude Modulator)
3. Dual Amplifier Active Filters (DAAFs)
  - a. Low-Pass Filter (LPF)
  - b. High-Pass Filter (HPF)
5. Tri-level Voltage Detector

### 2.1 Telephone-Line Transceiver

The telephone-line transceiver of *Figure 7* provides a full-duplexed connection through a PCMCIA, miniature transformer. The differential configuration of receiver portion (UR), cancels reception from the transmitter portion (UT). Note that the input signals for the differential configuration of UR, are the transmit voltage ( $V_T$ ) and  $V_T/2$ . This is because  $R_{match}$  is chosen to match the coupled telephone-line impedance; therefore dividing  $V_T$  by two (assuming  $R_1 \gg R_{match}$ ). The differential configuration of UR has its resistors chosen to cancel the  $V_T$  and  $V_T/2$  inputs according to the following equation:

$$V_0 = V_T \left( \frac{R_4}{R_3 + R_4} \right) \left( 1 + \frac{R_2}{R_1} \right) - \frac{V_T}{2} \left( \frac{R_2}{R_1} \right) = V_T \frac{1}{3} (3) - \frac{V_T}{2} (2) = 0$$



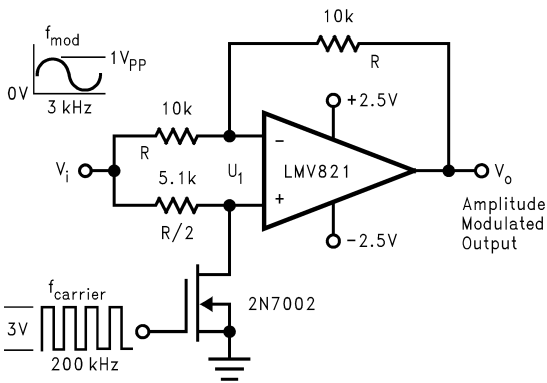
**FIGURE 7. Telephone-line Transceiver for a PCMCIA Modem Card**

Note that  $C_r$  is included for canceling out the inadequacies of the lossy, miniature transformer. Refer to application note AN-397 for detailed explanation.

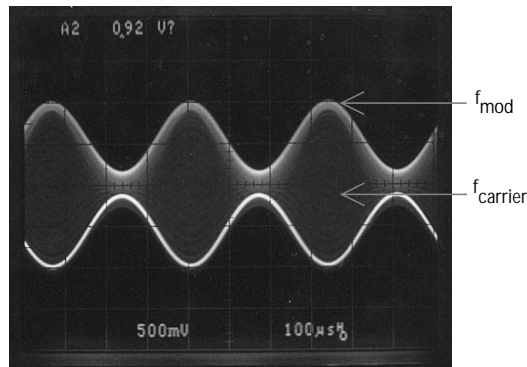
**2.2“Simple” Mixer (Amplitude Modulator)**

The mixer of *Figure 8* is simple and provides a unique form of amplitude modulation.  $V_i$  is the modulation frequency ( $F_M$ ), while a +3V square-wave at the gate of Q1, induces a carrier frequency ( $F_C$ ). Q1 switches (toggles) U1 between inverting and non-inverting unity gain configurations. Offsetting a sine wave above ground at  $V_i$  results in the oscilloscope photo of *Figure 9*.

The simple mixer can be applied to applications that utilize the Doppler Effect to measure the velocity of an object. The difference frequency is one of its output frequency components. This difference frequency magnitude ( $F_M - F_C$ ) is the key factor for determining an object’s velocity per the Doppler Effect. If a signal is transmitted to a moving object, the reflected frequency will be a different frequency. This difference in transmit and receive frequency is directly proportional to an object’s velocity.



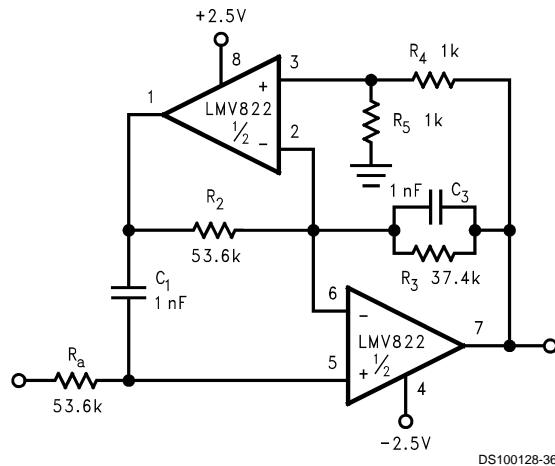
**FIGURE 8. Amplitude Modulator Circuit**



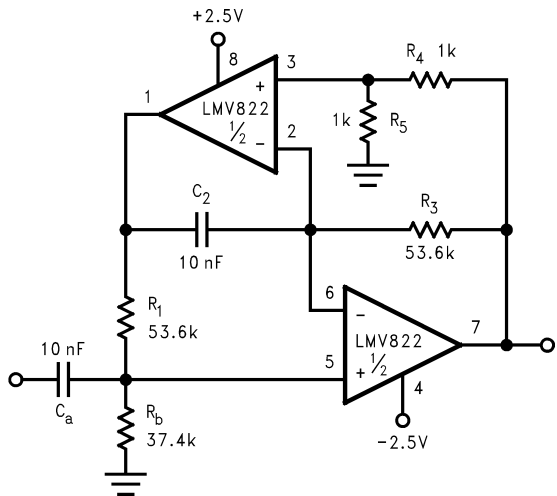
**FIGURE 9. Output signal per the Circuit of *Figure 8***

**2.4 Dual Amplifier Active Filters (DAAFs)**

The LMV822/24 bring economy and performance to DAAFs. The low-pass and the high-pass filters of *Figure 10* and *Figure 11* (respectively), offer one key feature: excellent sensitivity performance. Good sensitivity is when deviations in component values cause relatively small deviations in a filter’s parameter such as cutoff frequency ( $F_c$ ). Single amplifier active filters like the Sallen-Key provide relatively poor sensitivity performance that sometimes cause problems for high production runs; their parameters are much more likely to deviate out of specification than a DAAF would. The DAAFs of *Figure 10* and *Figure 11* are well suited for high volume production.



**FIGURE 10. Dual Amplifier, 3 kHz Low-Pass Active Filter with a Butterworth Response and a Pass Band Gain of Times Two**



DS100128-37

**FIGURE 11. Dual Amplifier, 300 Hz High-Pass Active Filter with a Butterworth Response and a Pass Band Gain of Times Two**

Table 1 provides sensitivity measurements for a 10 MΩ load condition. The left column shows the passive components for the 3 kHz low-pass DAAF. The third column shows the components for the 300 Hz high-pass DAAF. Their respective sensitivity measurements are shown to the right of each component column. Their values consists of the percent change in cutoff frequency (Fc) divided by the percent change in component value. The lower the sensitivity value, the better the performance.

Each resistor value was changed by about 10 percent, and this measured change was divided into the measured change in Fc. A positive or negative sign in front of the measured value, represents the direction Fc changes relative to components' direction of change. For example, a sensitivity value of negative 1.2, means that for a 1 percent increase in component value, Fc decreases by 1.2 percent. Note that this information provides insight on how to fine tune the cutoff frequency, if necessary. It should be also noted that R4 and R5 of each circuit also caused variations in the pass band gain. Increasing R4 by ten percent, increased the gain by 0.4 dB, while increasing R5 by ten percent, decreased the gain by 0.4 dB.

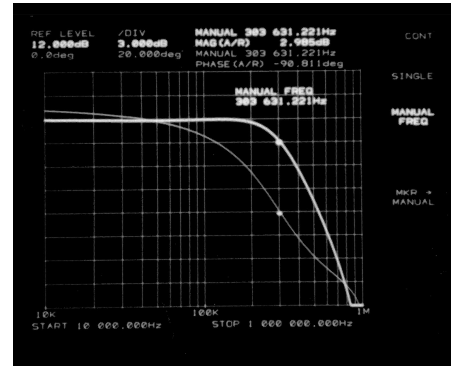
**TABLE 1.**

Component (LPF)	Sensitivity (LPF)	Component (HPF)	Sensitivity (HPF)
R <sub>a</sub>	-1.2	C <sub>a</sub>	-0.7
C <sub>1</sub>	-0.1	R <sub>b</sub>	-1.0
R <sub>2</sub>	-1.1	R <sub>1</sub>	+0.1
R <sub>3</sub>	+0.7	C <sub>2</sub>	-0.1
C <sub>3</sub>	-1.5	R <sub>3</sub>	+0.1
R <sub>4</sub>	-0.6	R <sub>4</sub>	-0.1
R <sub>5</sub>	+0.6	R <sub>5</sub>	+0.1

Active filters are also sensitive to an op amp's parameters -Gain and Bandwidth, in particular. The LMV822/24 provide a large gain and wide bandwidth. And DAAFs make excellent use of these feature specifications.

Single Amplifier versions require a large open-loop to closed-loop gain ratio - approximately 50 to 1, at the Fc of

the filter response. *Figure 12* shows an impressive photograph of a network analyzer measurement (hp3577A). The measurement was taken from a 300kHz version of *Figure 10*. At 300 kHz, the open-loop to closed-loop gain ratio @ Fc is about 5 to 1. This is 10 times lower than the 50 to 1 "rule of thumb" for Single Amplifier Active Filters.



DS100128-92

**FIGURE 12. 300 kHz, Low-Pass Filter, Butterworth Response as Measured by the HP3577A Network Analyzer**

In addition to performance, DAAFs are relatively easy to design and implement. The design equations for the low-pass and high-pass DAAFs are shown below. The first two equations calculate the Fc and the circuit Quality Factor (Q) for the LPF (*Figure 10*). The second two equations calculate the Fc and Q for the HPF (*Figure 11*).

$$\begin{aligned} \text{(LPF)} \quad F_c &= \frac{\sqrt{R_5}}{2\pi \sqrt{R_a} \cdot \sqrt{R_2} \cdot \sqrt{R_4} \cdot \sqrt{C_1} \cdot \sqrt{C_3}} \\ Q &= 2\pi F_c \sqrt{C_1} \cdot \sqrt{C_3} \\ \text{(HPF)} \quad F_c &= \frac{\sqrt{R_4}}{2\pi \sqrt{R_1} \cdot \sqrt{R_3} \cdot \sqrt{R_5} \cdot \sqrt{C_a} \cdot \sqrt{C_2}} \\ Q &= 2\pi F_c \sqrt{C_a} \cdot \sqrt{C_2} \end{aligned}$$

To simplify the design process, certain components are set equal to each other. Refer to *Figure 10* and *Figure 11*. These equal component values help to simplify the design equations as follows:

$$\begin{aligned} \text{(LPF)} \quad R_a &= R_2 = \frac{1}{2\pi F_c \sqrt{C_1} \cdot \sqrt{C_3}} \\ R_3 &= \frac{Q}{2\pi F_c \sqrt{C_1} \cdot \sqrt{C_3}} \\ \text{(HPF)} \quad R_1 &= R_3 = \frac{1}{2\pi F_c \sqrt{C_a} \cdot \sqrt{C_2}} \\ R_b &= \frac{Q}{2\pi F_c \sqrt{C_a} \cdot \sqrt{C_2}} \end{aligned}$$

To illustrate the design process/implementation, a 3 kHz, Butterworth response, low-pass filter DAAF (*Figure 10*) is designed as follows:

1. Choose C<sub>1</sub> = C<sub>3</sub> = C = 1 nF
2. Choose R<sub>4</sub> = R<sub>5</sub> = 1 kΩ
3. Calculate R<sub>a</sub> and R<sub>2</sub> for the desired Fc as follows:

$$R_a = R_2 = \frac{1}{2\pi(F_C)C}$$

$$= \frac{1}{2\pi(3 \text{ kHz}) 1 \text{ nF}}$$

$$= 53.1 \text{ k}\Omega$$

$$\cong 53.6 \text{ k}\Omega \text{ (Practical Value)}$$

4. Calculate  $R_3$  for the desired Q. The desired Q for a Butterworth (Maximally Flat) response is 0.707 (45 degrees into the s-plane).  $R_3$  calculates as follows:

$$R_3 = \frac{Q}{2\pi(F_C)C}$$

$$= \frac{0.707}{2\pi(3 \text{ kHz}) 1 \text{ nF}}$$

$$= 37.5 \text{ k}\Omega$$

$$\cong 37.4 \text{ k}\Omega \text{ (Practical Value)}$$

Notice that  $R_3$  could also be calculated as 0.707 of  $R_a$  or  $R_2$ . The circuit was implemented and its cutoff frequency measured. The cutoff frequency measured at 2.92 kHz.

The circuit also showed good repeatability. Ten different LMV822 samples were placed in the circuit. The corresponding change in the cutoff frequency was less than a percent.

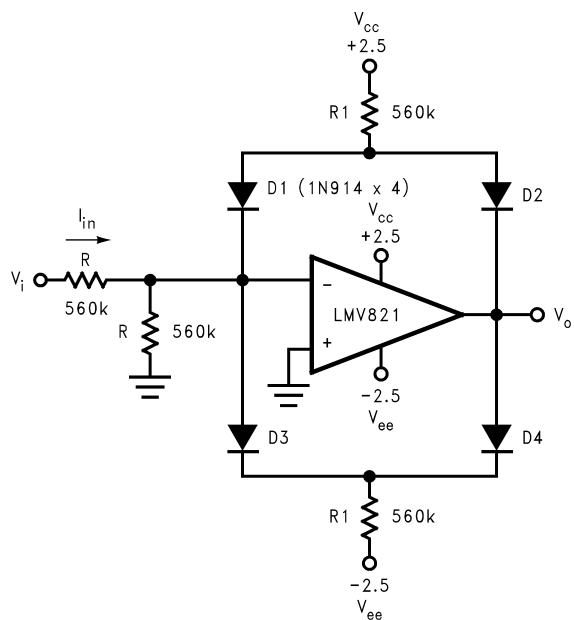


FIGURE 13. Tri-level Voltage Detector

### 2.5 Tri-level Voltage Detector

The tri-level voltage detector of Figure 13 provides a type of window comparator function. It detects three different input voltage ranges: Min-range, Mid-range, and Max-range. The output voltage ( $V_O$ ) is at  $V_{CC}$  for the Min-range.  $V_O$  is clamped at GND for the Mid-range. For the Max-range,  $V_O$  is at  $V_{ee}$ . Figure 14 shows a  $V_O$  vs.  $V_I$  oscilloscope photo per the circuit of Figure 13.

Its operation is as follows:  $V_I$  deviating from GND, causes the diode bridge to absorb  $I_{IN}$  to maintain a clamped condition ( $V_O = 0V$ ). Eventually,  $I_{IN}$  reaches the bias limit of the diode bridge. When this limit is reached, the clamping effect stops and the op amp responds open loop. The design equation directly preceding Figure 14, shows how to determine the clamping range. The equation solves for the input voltage band on each side GND. The mid-range is twice this voltage band.

$$\Delta V = \frac{R}{R_1} (V_{CC} - V_{Diode})$$

DS100128-89

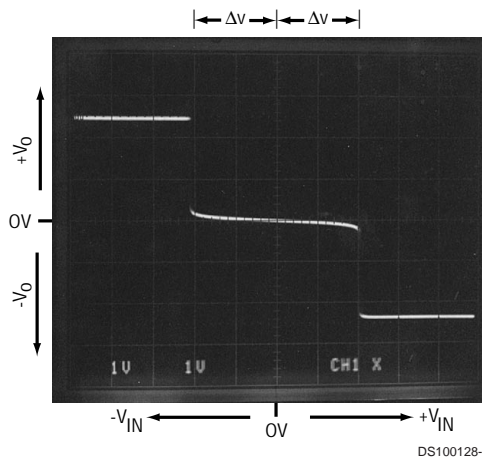
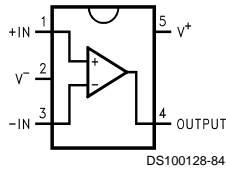


FIGURE 14. X, Y Oscilloscope Trace showing  $V_{OUT}$  vs  $V_{IN}$  per the Circuit of Figure 13



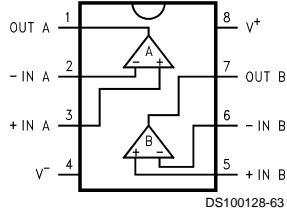
## Connection Diagrams

5-Pin SC70-5/SOT23-5



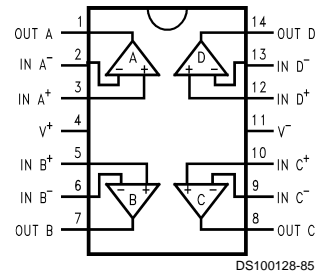
Top View

8-Pin SO/MSOP



Top View

14-Pin SO/TSSOP



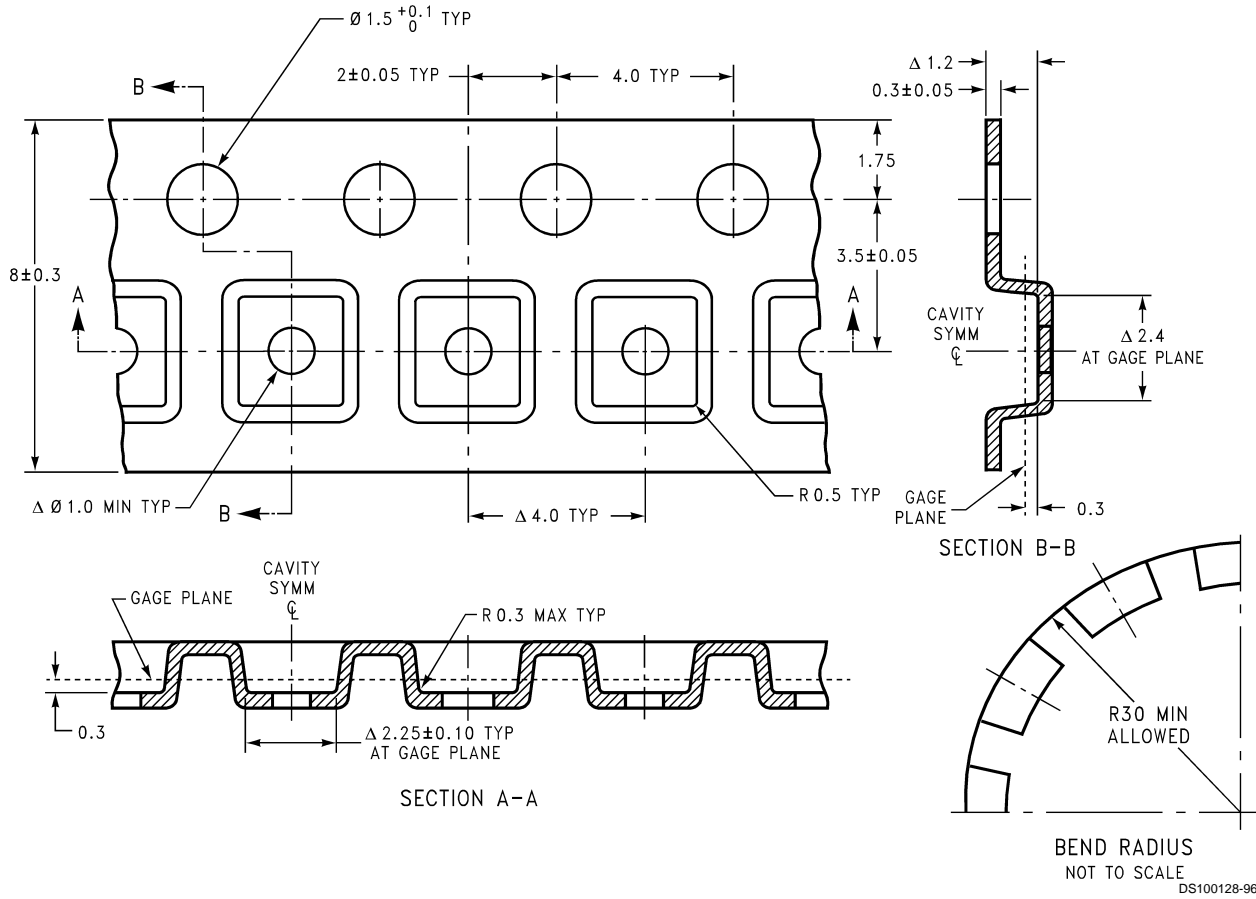
Top View

## Ordering Information

Package	Temperature Range	Packaging Marking	Transport Media	NSC Drawing
	Industrial -40°C to +85°C			
5-Pin SC-70-5	LMV821M7	A15	1k Units Tape and Reel	MAA05
	LMV821M7X	A15	3k Units Tape and Reel	
5-Pin SOT23-5	LMV821M5	A14	1k Units Tape and Reel	MA05B
	LMV821M5X	A14	3k Units Tape and Reel	
8-Pin SO	LMV822M	LMV822M	Rails	M08A
	LMV822MX	LMV822M	2.5k Units Tape and Reel	
8-Pin MSOP	LMV822MM	LMV822	1k Units Tape and Reel	MUA08A
	LMV822MMX	LMV822	3.5k Units Tape and Reel	
14-Pin SO	LMV824M	LMV824M	Rails	M14A
	LMV824MX	LMV824M	2.5k Units Tape and Reel	
14-Pin TSSOP	LMV824MT	LMV824MT	Rails	MTC14
	LMV824MTX	LMV824MT	2.5k Units Tape and Reel	



### SC70-5 Tape and Reel Specification

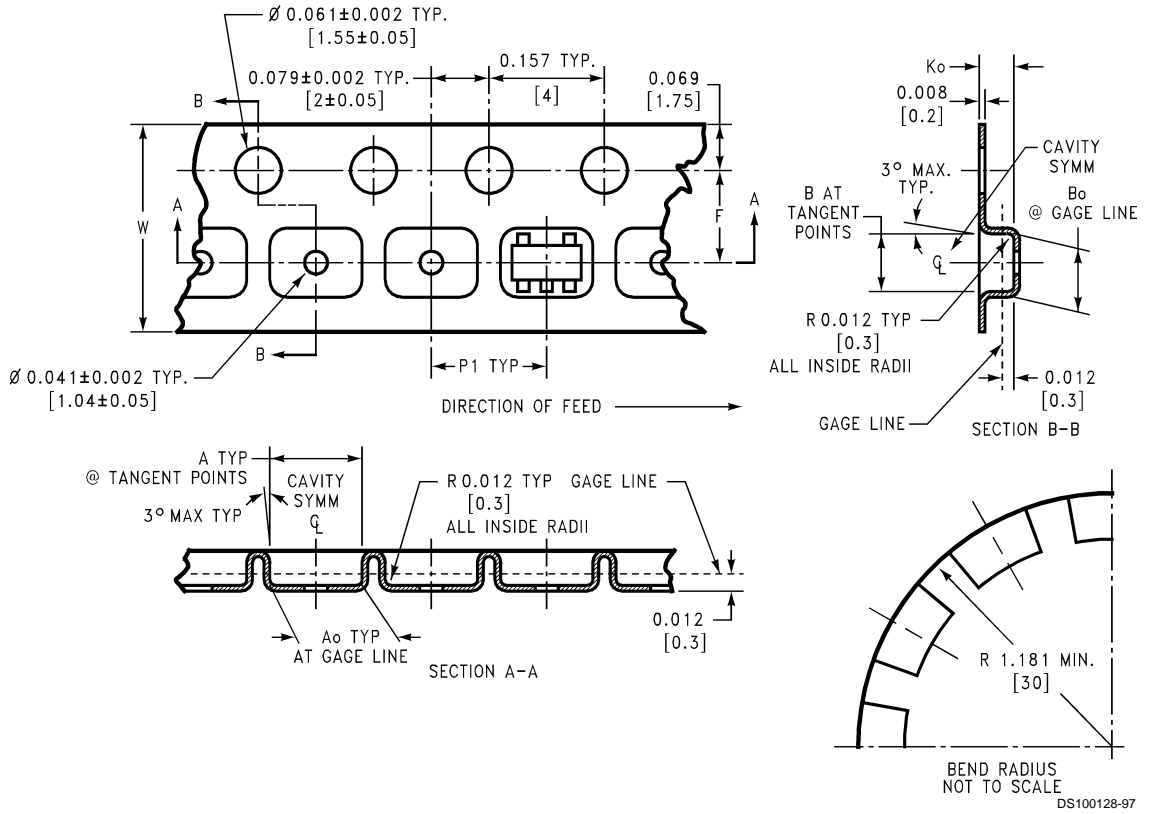


### SOT-23-5 Tape and Reel Specification

#### Tape Format

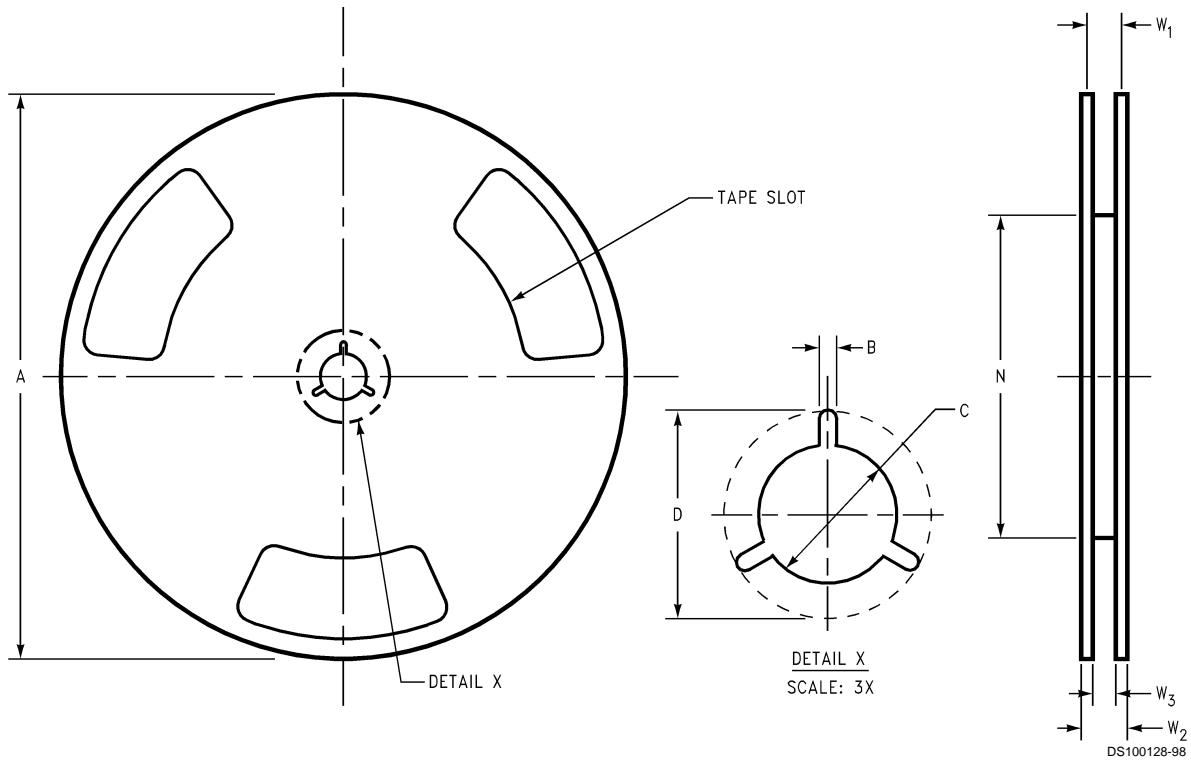
Tape Section	# Cavities	Cavity Status	Cover Tape Status
Leader (Start End)	0 (min)	Empty	Sealed
	75 (min)	Empty	Sealed
Carrier	3000	Filled	Sealed
	250	Filled	Sealed
Trailer (Hub End)	125 (min)	Empty	Sealed
	0 (min)	Empty	Sealed

# Tape Dimensions



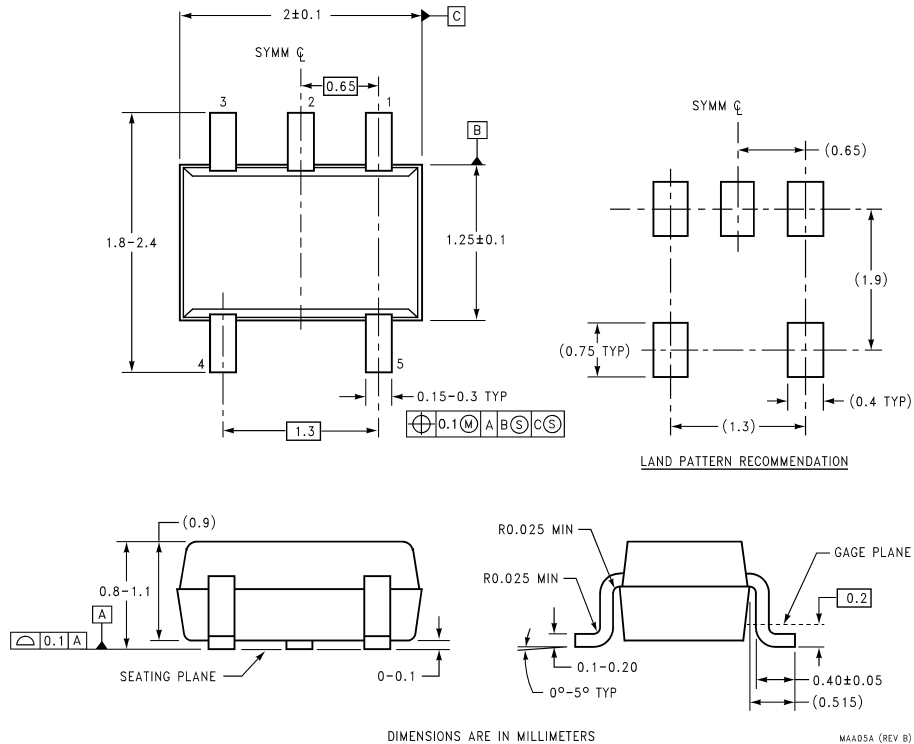
<b>8 mm</b>	<b>0.130</b>	<b>0.124</b>	<b>0.130</b>	<b>0.126</b>	<b>0.138 ± 0.002</b>	<b>0.055 ± 0.004</b>	<b>0.157</b>	<b>0.315 ± 0.012</b>
	<b>(3.3)</b>	<b>(3.15)</b>	<b>(3.3)</b>	<b>(3.2)</b>	<b>(3.5 ± 0.05)</b>	<b>(1.4 ± 0.11)</b>	<b>(4)</b>	<b>(8 ± 0.3)</b>
Tape Size	DIM A	DIM Ao	DIM B	DIM Bo	DIM F	DIM Ko	DIM P1	DIM W

# Reel Dimensions

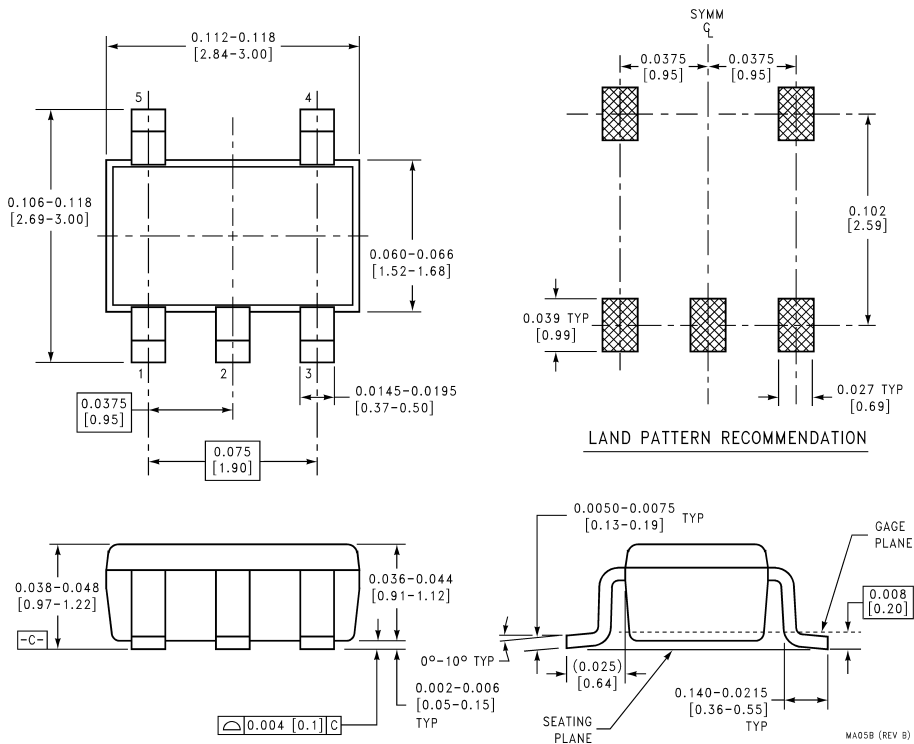


<b>8 mm</b>	<b>7.00</b>	<b>0.059</b>	<b>0.512</b>	<b>0.795</b>	<b>2.165</b>	<b>0.331 + 0.059/-0.000</b>	<b>0.567</b>	<b>W1 + 0.078/-0.039</b>
	<b>330.00</b>	<b>1.50</b>	<b>13.00</b>	<b>20.20</b>	<b>55.00</b>	<b>8.40 + 1.50/-0.00</b>	<b>14.40</b>	<b>W1 + 2.00/-1.00</b>
Tape Size	A	B	C	D	N	W1	W2	W3

**Physical Dimensions** inches (millimeters) unless otherwise noted

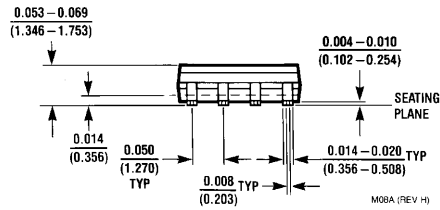
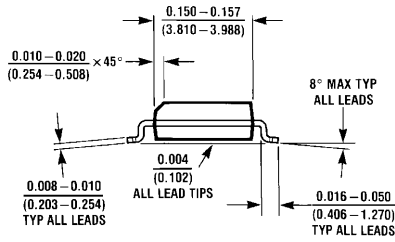
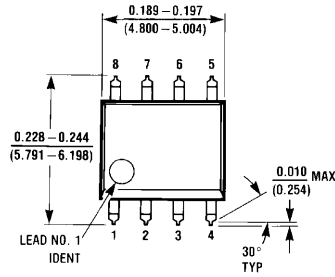


**SC70-5**  
**Order Number LMV821M7 or LMV821M7X**  
**NS Package Number MAA05**

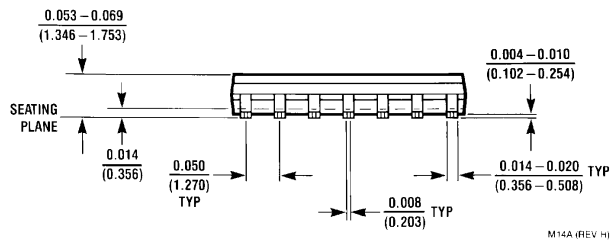
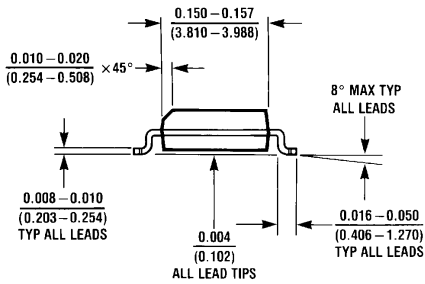
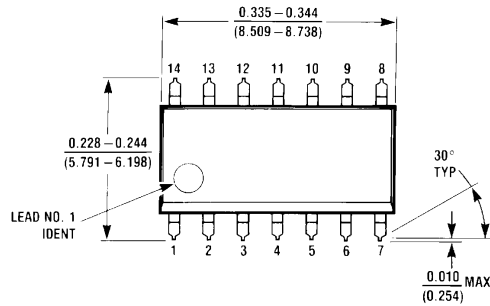


**SOT 23-5**  
**Order Number LMV821M5 or LMV821M5X**  
**NS Package Number MA05B**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)

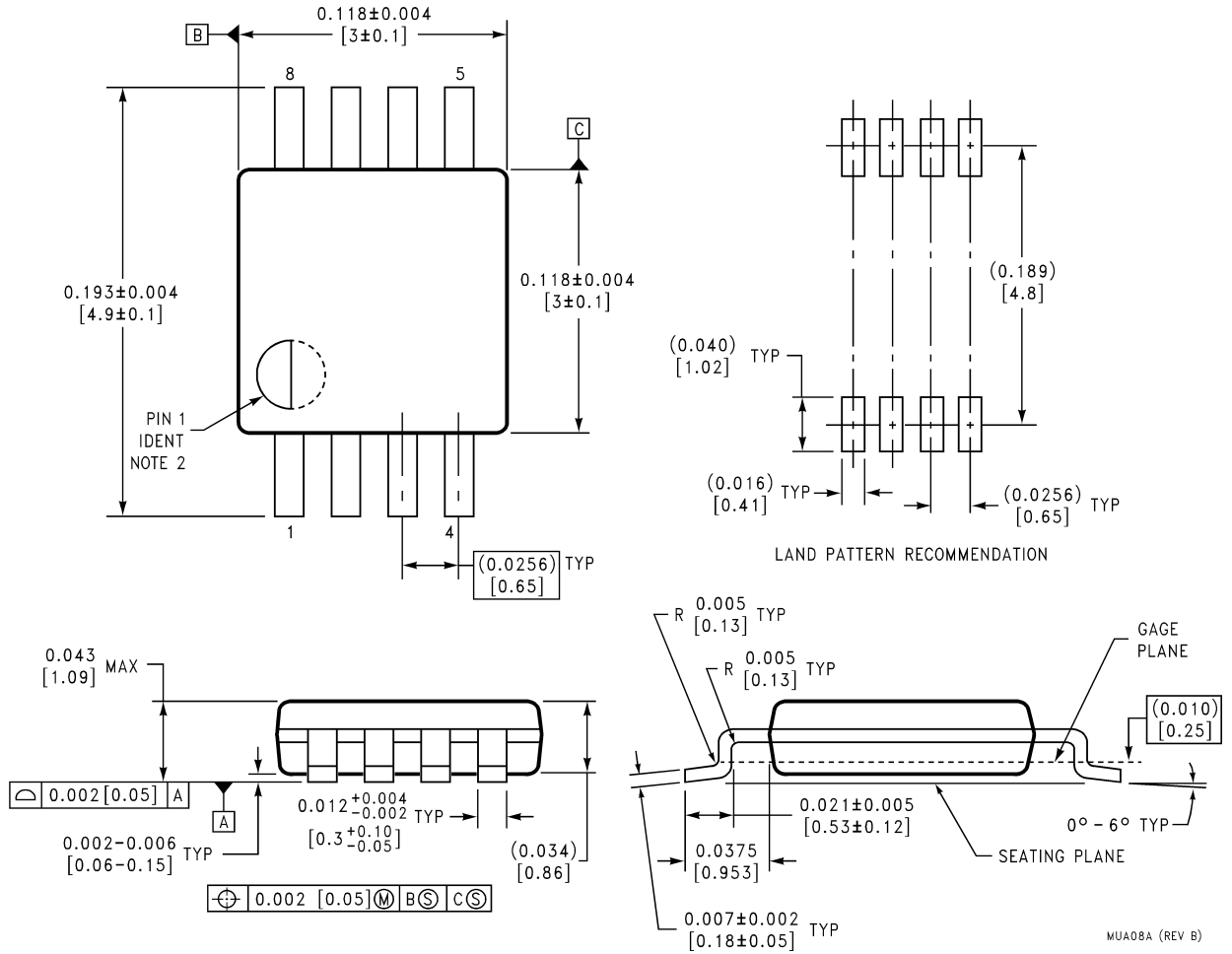


**8-Pin Small Outline**  
**Order Number LMV822M or LMV822MX**  
**NS Package Number M08A**



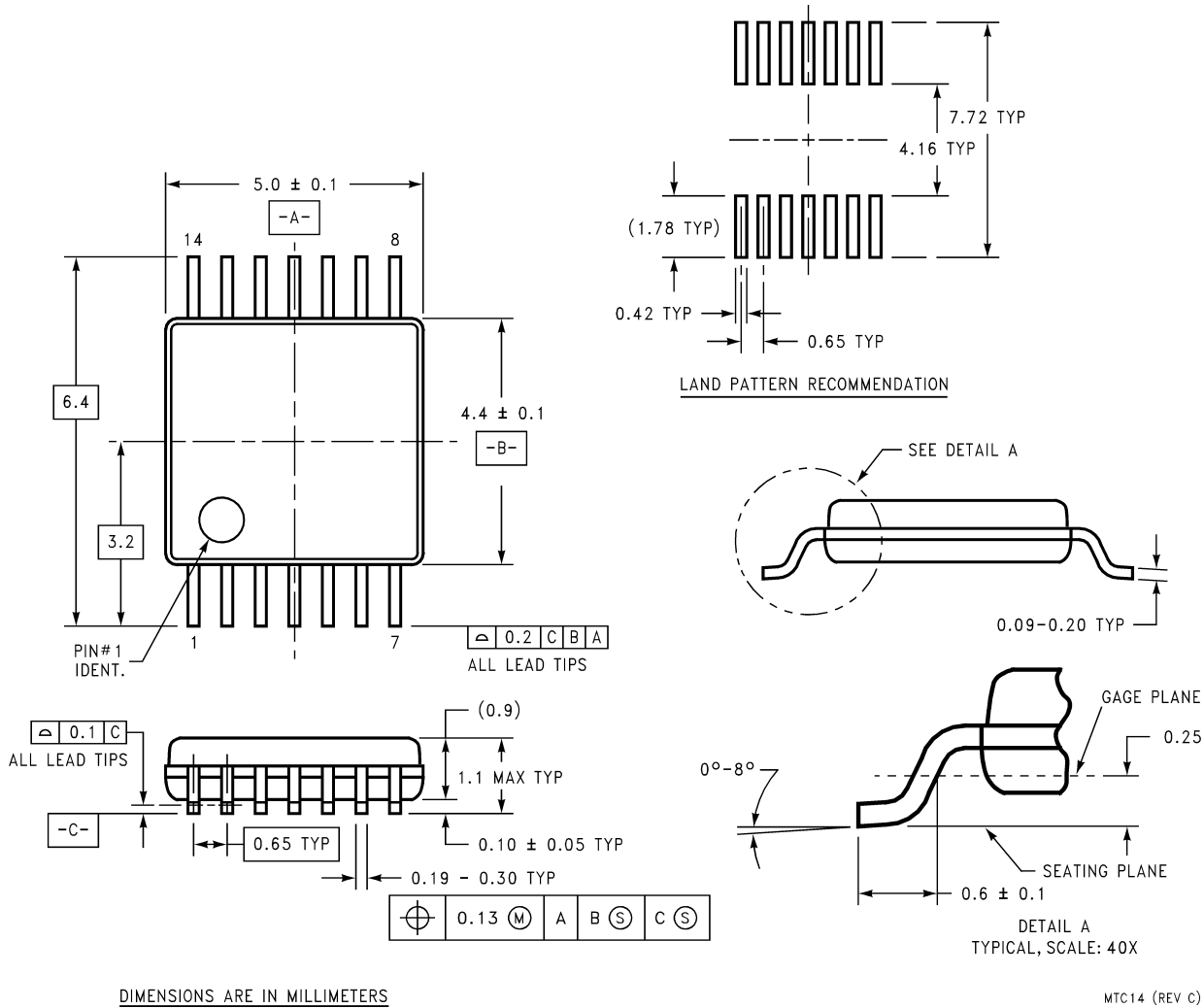
**14-Pin Small Outline**  
**Order Number LMV824M or LMV824MX**  
**NS Package Number M14A**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**8-Pin MSOP**  
**Order Number LMV822MM or LMV822MMX**  
**NS Package Number MUA08A**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**14-Pin TSSOP**  
**Order Number LMV824MTC or LMV824MTCX**  
**NS Package Number MTC14**

**LIFE SUPPORT POLICY**

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT AND GENERAL COUNSEL OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

**National Semiconductor Corporation**  
 Americas  
 Tel: 1-800-272-9959  
 Fax: 1-800-737-7018  
 Email: support@nsc.com  
 www.national.com

**National Semiconductor Europe**  
 Fax: +49 (0) 180-530 85 86  
 Email: europe.support@nsc.com  
 Deutsch Tel: +49 (0) 69 9508 6208  
 English Tel: +44 (0) 870 24 0 2171  
 Français Tel: +33 (0) 1 41 91 8790

**National Semiconductor Asia Pacific Customer Response Group**  
 Tel: 65-2544466  
 Fax: 65-2504466  
 Email: ap.support@nsc.com

**National Semiconductor Japan Ltd.**  
 Tel: 81-3-5639-7560  
 Fax: 81-3-5639-7507