

# LMX2330U/LMX2331U/LMX2332U PLLatinum™ Ultra Low Power Dual Frequency Synthesizer for RF Personal Communications

**LMX2330U 2.5 GHz/600 MHz**

**LMX2331U 2.0 GHz/600 MHz**

**LMX2332U 1.2 GHz/600 MHz**

## General Description

The LMX233xU devices are high performance frequency synthesizers with integrated dual modulus prescalers. The LMX233xU devices are designed for use as RF and IF local oscillators for dual conversion radio transceivers.

A 32/33 or a 64/65 prescale ratio can be selected for the 2.5 GHz LMX2330U RF synthesizer. A 64/65 or a 128/129 prescale ratio can be selected for both the LMX2331U and LMX2332U RF synthesizers. The IF circuitry contains an 8/9 or a 16/17 prescaler. Using a proprietary digital phase locked loop technique, the LMX233xU devices generate very stable, low noise control signals for RF and IF voltage controlled oscillators. Both the RF and IF synthesizers include a two-level programmable charge pump. The RF synthesizer has dedicated Fastlock circuitry.

Serial data is transferred to the devices via a three-wire interface (Data, LE, Clock). Supply voltages from 2.7V to 5.5V are supported. The LMX233xU family features ultra low current consumption:

LMX2330U (2.5 GHz)—3.3 mA, LMX2331U (2.0 GHz)—2.9 mA, LMX2332U (1.2 GHz)—2.5 mA at 3.0V.

The LMX233xU devices are available in 20-Pin TSSOP and 24-Pin CSP surface mount plastic packages.

## Features

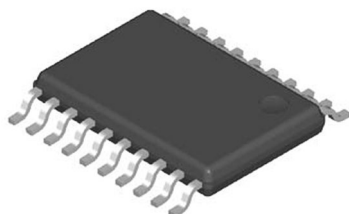
- Ultra Low Current Consumption
- Upgrade and Compatible to LMX233xL Family
- 2.7V to 5.5V Operation
- Selectable Synchronous or Asynchronous Powerdown Mode:  
 $I_{CC-PWDN} = 1 \mu A$  typical
- Selectable Dual Modulus Prescaler:
 

LMX2330U	RF: 32/33 or 64/65
LMX2331U	RF: 64/65 or 128/129
LMX2332U	RF: 64/65 or 128/129
LMX2330U/31U/32U	IF: 8/9 or 16/17
- Selectable Charge Pump TRI-STATE® Mode
- Programmable Charge Pump Current Levels  
 RF and IF: 0.95 or 3.8 mA
- Selectable Fastlock™ Mode for the RF Synthesizer
- Push-Pull Analog Lock Detect Output
- Available in 20-Pin TSSOP and 24-Pin Chip Scale Package (CSP)

## Applications

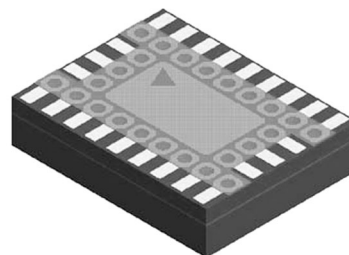
- Mobile Handsets  
 (GSM, GPRS, W-CDMA, CDMA, PCS, AMPS, PDC, DCS)
- Cordless Handsets  
 (DECT, DCT)
- Wireless Data
- Cable TV Tuners

Thin Shrink Small Outline Package (MTC20)



10136680

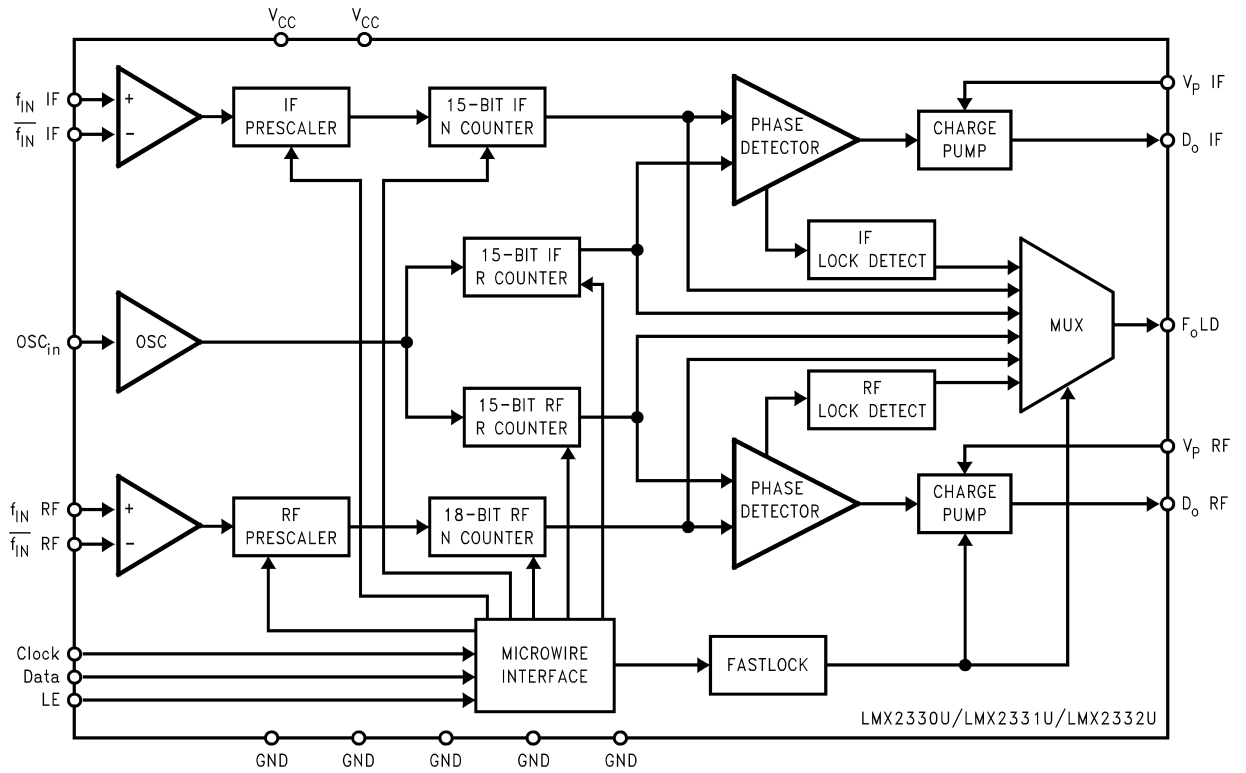
Chip Scale Package (SLB24A)



10136681

PLLatinum™ is a trademark of National Semiconductor Corporation.

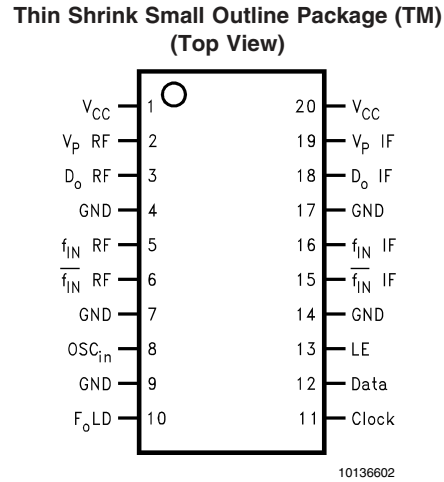
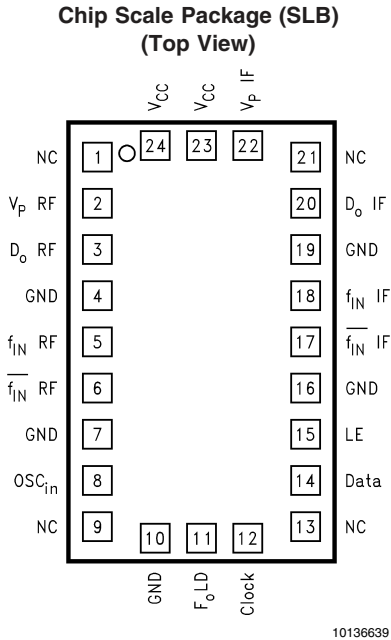
### Functional Block Diagram



LMX2330U/LMX2331U/LMX2332U

10136601

## Connection Diagrams



## Pin Descriptions

Pin Name	Pin No. 24-Pin CSP	Pin No. 20-Pin TSSOP	I/O	Description
V <sub>CC</sub>	24	1	—	Power supply bias for the RF PLL analog and digital circuits. V <sub>CC</sub> may range from 2.7V to 5.5V. Bypass capacitors should be placed as close as possible to this pin and be connected directly to the ground plane.
V <sub>P</sub> RF	2	2	—	RF PLL charge pump power supply. Must be ≥ V <sub>CC</sub> .
D <sub>O</sub> RF	3	3	O	RF PLL charge pump output. The output is connected to the external loop filter, which drives the input of the VCO.
GND	4	4	—	Ground for the RF PLL digital circuitry.
f <sub>IN</sub> RF	5	5	I	RF PLL prescaler input. Small signal input from the VCO.
f <sub>IN</sub> RF	6	6	I	RF PLL prescaler complementary input. For single ended operation, this pin should be AC grounded. The LMX233xU RF PLL can be driven differentially when the bypass capacitor is omitted.
GND	7	7	—	Ground for the RF PLL analog circuitry.
OSC <sub>in</sub>	8	8	I	Reference oscillator input. The input has an approximate V <sub>CC</sub> /2 threshold and can be driven from an external CMOS or TTL logic gate.
GND	10	9	—	Ground for the IF PLL digital circuits, MICROWIRE™, F <sub>O</sub> LD, and oscillator circuits.
F <sub>O</sub> LD	11	10	O	Programmable multiplexed output pin. Functions as a general purpose CMOS TRI-STATE output, RF/IF PLL push-pull analog lock detect output, N and R divider output or Fastlock output, which connects a parallel resistor to the external loop filter.
Clock	12	11	I	MICROWIRE Clock input. High impedance CMOS input. Data is clocked into the 22-bit shift register on the rising edge of Clock.
Data	14	12	I	MICROWIRE Data input. High impedance CMOS input. Binary serial data. The MSB of Data is shifted in first. The last two bits are the control bits.
LE	15	13	I	MICROWIRE Latch Enable input. High impedance CMOS input. When LE transitions HIGH, Data stored in the shift register is loaded into one of 4 internal control registers.
GND	16	14	—	Ground for the IF PLL analog circuitry.

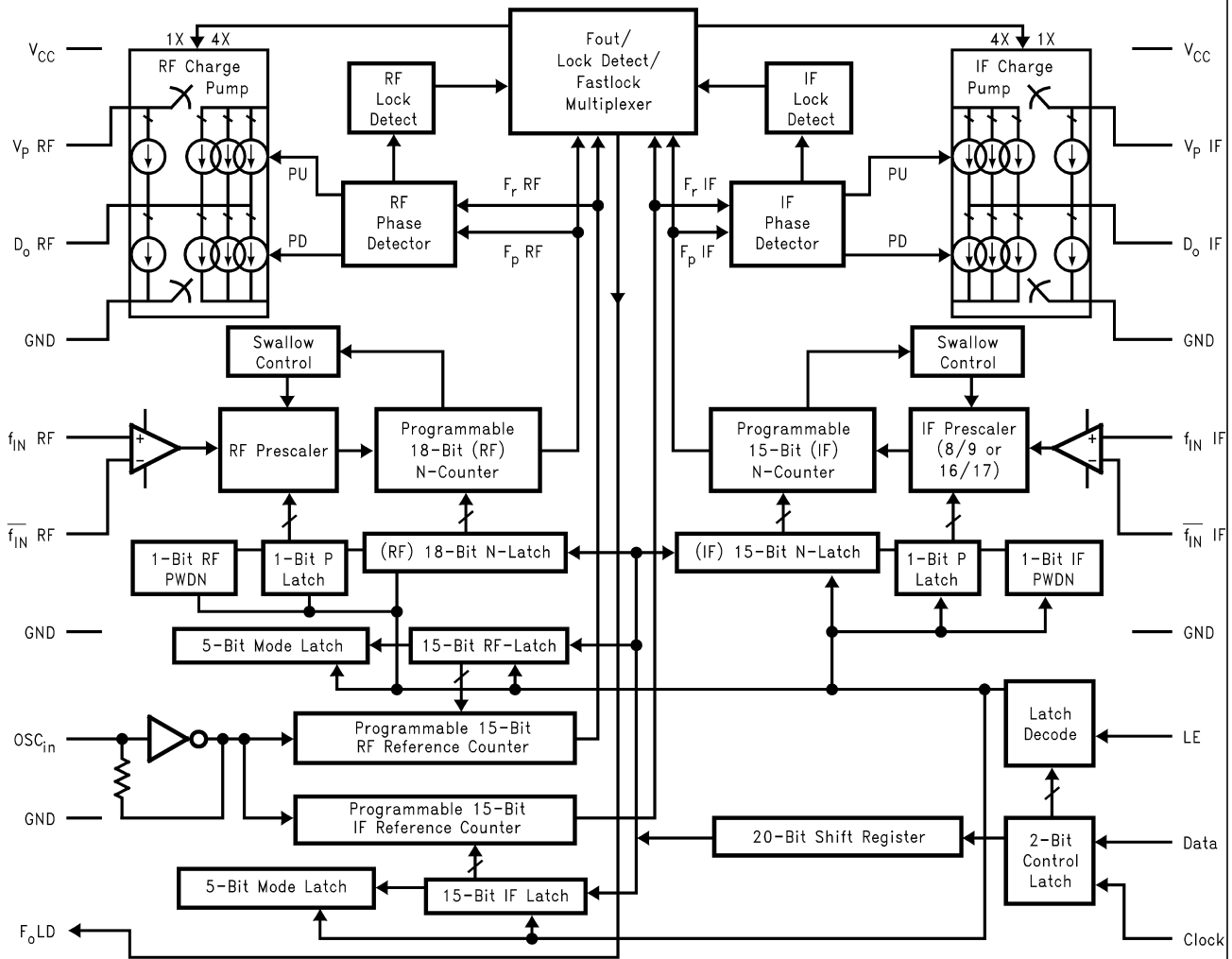
## Pin Descriptions (Continued)

Pin Name	Pin No. 24-Pin CSP	Pin No. 20-Pin TSSOP	I/O	Description
$\bar{f}_{IN}$ IF	17	15	I	IF PLL prescaler complementary input. For single ended operation, this pin should be AC grounded. The LMX233xU IF PLL can be driven differentially when the bypass capacitor is omitted.
$f_{IN}$ IF	18	16	I	IF PLL prescaler input. Small signal input from the VCO.
GND	19	17	—	Ground for the IF PLL digital circuitry, MICROWIRE, $F_{oLD}$ , and oscillator circuits.
$D_o$ IF	20	18	O	IF PLL charge pump output. The output is connected to the external loop filter, which drives the input of the VCO.
$V_P$ IF	22	19	—	IF PLL charge pump power supply. Must be $\geq V_{CC}$ .
$V_{CC}$	23	20	—	Power supply bias for the IF PLL analog and digital circuits, MICROWIRE, $F_{oLD}$ , and oscillator circuits. $V_{CC}$ may range from 2.7V to 5.5V. Bypass capacitors should be placed as close as possible to this pin and be connected directly to the ground plane.
NC	1, 9, 13, 21	X	—	No connect.

## Ordering Information

Model	Temperature Range	Package Description	Packing	NS Package Number
LMX2330USLBX	-40°C to +85°C	Chip Scale Package (CSP) Tape and Reel	2500 Units Per Reel	SLB24A
LMX2330UTM	-40°C to +85°C	Thin Shrink Small Outline Package (TSSOP)	73 Units Per Rail	MTC20
LMX2330UTMX	-40°C to +85°C	Thin Shrink Small Outline Package (TSSOP) Tape and Reel	2500 Units Per Reel	MTC20
LMX2331USLBX	-40°C to +85°C	Chip Scale Package (CSP) Tape and Reel	2500 Units Per Reel	SLB24A
LMX2331UTM	-40°C to +85°C	Thin Shrink Small Outline Package (TSSOP)	73 Units Per Rail	MTC20
LMX2331UTMX	-40°C to +85°C	Thin Shrink Small Outline Package (TSSOP) Tape and Reel	2500 Units Per Reel	MTC20
LMX2332USLBX	-40°C to +85°C	Chip Scale Package (CSP) Tape and Reel	2500 Units Per Reel	SLB24A
LMX2332UTM	-40°C to +85°C	Thin Shrink Small Outline Package (TSSOP)	73 Units Per Rail	MTC20
LMX2332UTMX	-40°C to +85°C	Thin Shrink Small Outline Package (TSSOP) Tape and Reel	2500 Units Per Reel	MTC20

### Detailed Block Diagram



10136603

**Notes:**

1. A 64/65 or 128/129 prescaler ratio can be selected for the LMX2331U and LMX2332U RF synthesizers. A 32/33 or 64/65 prescaler ratio can be selected for the LMX2330U RF synthesizer.
2.  $V_{CC}$  supplies power to the RF and IF prescalers, RF and IF feedback dividers, RF and IF reference dividers, RF and IF phase detectors, the  $OSC_{in}$  buffer, MICROWIRE, and  $F_{oLD}$  circuitry.
3.  $V_P$  RF and  $V_P$  IF supply power to the charge pumps. They can be run separately as long as  $V_P$  RF  $\geq V_{CC}$  and  $V_P$  IF  $\geq V_{CC}$ .

## Absolute Maximum Ratings (Notes 1,

2, 3)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Power Supply Voltage

$V_{CC}$ to GND	-0.3V to +6.5V
$V_P$ RF to GND	-0.3V to +6.5V
$V_P$ IF to GND	-0.3V to +6.5V

Voltage on any pin to GND ( $V_I$ )

$V_I$ must be < +6.5V	-0.3V to $V_{CC}+0.3V$
-----------------------	------------------------

Storage Temperature Range ( $T_S$ ) -65°C to +150°C

Lead Temperature (solder 4 s) ( $T_L$ ) +260°C

TSSOP  $\theta_{JA}$  Thermal Impedance 114.5°C/W

CSP  $\theta_{JA}$  Thermal Impedance 112°C/W

## Recommended Operating Conditions (Note 1)

Power Supply Voltage

$V_{CC}$  to GND +2.7V to +5.5V

$V_P$  RF to GND  $V_{CC}$  to +5.5V

$V_P$  IF to GND  $V_{CC}$  to +5.5V

Operating Temperature ( $T_A$ ) -40°C to +85°C

**Note 1:** Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Recommended Operating Conditions indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, refer to the Electrical Characteristics section. The guaranteed specifications apply only for the conditions listed.

**Note 2:** This device is a high performance RF integrated circuit with an ESD rating <2 kV and is ESD sensitive. Handling and assembly of this device should only be done at ESD protected work stations.

**Note 3:** GND = 0V

## Electrical Characteristics

$V_{CC} = V_P$  RF =  $V_P$  IF = 3.0V, -40°C ≤  $T_A$  ≤ +85°C, unless otherwise specified

Symbol	Parameter	Conditions	Value			Units	
			Min	Typ	Max		
<b>I<sub>CC</sub> PARAMETERS</b>							
$I_{CCRF+IF}$	Power Supply Current, RF + IF Synthesizers	LMX2330U	Clock, Data and LE = GND		3.3	4.3	mA
		LMX2331U	OSC <sub>in</sub> = GND		2.9	3.8	mA
		LMX2332U	PWDN RF Bit = 0 PWDN IF Bit = 0		2.5	3.3	mA
$I_{CCRF}$	Power Supply Current, RF Synthesizer Only	LMX2330U	Clock, Data and LE = GND		2.3	3.0	mA
		LMX2331U	OSC <sub>in</sub> = GND		1.9	2.5	mA
		LMX2332U	PWDN RF Bit = 0 PWDN IF Bit = 1		1.5	2.0	mA
$I_{CCIF}$	Power Supply Current, IF Synthesizer Only	LMX233xU	Clock, Data and LE = GND OSC <sub>in</sub> = GND PWDN RF Bit = 1 PWDN IF Bit = 0		1.0	1.3	mA
$I_{CC-PWDN}$	Powerdown Current	LMX233xU	Clock, Data and LE = GND OSC <sub>in</sub> = GND PWDN RF Bit = 1 PWDN IF Bit = 1		1.0	10.0	μA
<b>RF SYNTHESIZER PARAMETERS</b>							
$f_{IN}$ RF	RF Operating Frequency	LMX2330U		500		2500	MHz
		LMX2331U		200		2000	MHz
		LMX2332U		100		1200	MHz
$N_{RF}$	RF N Divider Range		Prescaler = 32/33 (Note 4)	96		65631	
			Prescaler = 64/65 (Note 4)	192		131135	
			Prescaler = 128/129 (Note 4)	384		262143	
$R_{RF}$	RF R Divider Range			3		32767	
$F_{\phi RF}$	RF Phase Detector Frequency					10	MHz

**Electrical Characteristics** (Continued) $V_{CC} = V_P$  RF =  $V_P$  IF = 3.0V,  $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$ , unless otherwise specified

Symbol	Parameter	Conditions	Value			Units
			Min	Typ	Max	
<b>RF SYNTHESIZER PARAMETERS</b>						
P <sub>f<sub>IN</sub> RF</sub>	RF Input Sensitivity	$2.7\text{V} \leq V_{CC} \leq 3.0\text{V}$ (Note 5)	-15		0	dBm
		$3.0 < V_{CC} \leq 5.5\text{V}$ (Note 5)	-10		0	dBm
ID <sub>o</sub> RF SOURCE	RF Charge Pump Output Source Current	$VD_o$ RF = $V_P$ RF/2 ID <sub>o</sub> RF Bit = 0 (Note 6)		-0.95		mA
		$VD_o$ RF = $V_P$ RF/2 ID <sub>o</sub> RF Bit = 1 (Note 6)		-3.80		mA
ID <sub>o</sub> RF SINK	RF Charge Pump Output Sink Current	$VD_o$ RF = $V_P$ RF/2 ID <sub>o</sub> RF Bit = 0 (Note 6)		0.95		mA
		$VD_o$ RF = $V_P$ RF/2 ID <sub>o</sub> RF Bit = 1 (Note 6)		3.80		mA
ID <sub>o</sub> RF TRI-STATE	RF Charge Pump Output TRI-STATE Current	$0.5\text{V} \leq VD_o$ RF $\leq V_P$ RF - 0.5V (Note 6)	-2.5		2.5	nA
ID <sub>o</sub> RF SINK Vs ID <sub>o</sub> RF SOURCE	RF Charge Pump Output Sink Current Vs Charge Pump Output Source Current Mismatch	$VD_o$ RF = $V_P$ RF/2 $T_A = +25^\circ\text{C}$ (Note 7)		3	10	%
ID <sub>o</sub> RF Vs VD <sub>o</sub> RF	RF Charge Pump Output Current Magnitude Variation Vs Charge Pump Output Voltage	$0.5\text{V} \leq VD_o$ RF $\leq V_P$ RF - 0.5V $T_A = +25^\circ\text{C}$ (Note 7)		10	15	%
ID <sub>o</sub> RF Vs T <sub>A</sub>	RF Charge Pump Output Current Magnitude Variation Vs Temperature	$VD_o$ RF = $V_P$ RF/2 (Note 7)		10		%
<b>IF SYNTHESIZER PARAMETERS</b>						
f <sub>IN</sub> IF	IF Operating Frequency	LMX2330U		45	600	MHz
		LMX2331U		45	600	MHz
		LMX2332U		45	600	MHz
N <sub>IF</sub>	IF N Divider Range	Prescaler = 8/9 (Note 4)		24	16391	
		Prescaler = 16/17 (Note 4)		48	32767	
R <sub>IF</sub>	IF R Divider Range			3	32767	
F <sub>φIF</sub>	IF Phase Detector Frequency				10	MHz
P <sub>f<sub>IN</sub> IF</sub>	IF Input Sensitivity	$2.7\text{V} \leq V_{CC} \leq 5.5\text{V}$ (Note 5)	-10		0	dBm

**Electrical Characteristics** (Continued) $V_{CC} = V_P$  RF =  $V_P$  IF = 3.0V,  $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ , unless otherwise specified

Symbol	Parameter	Conditions	Value			Units
			Min	Typ	Max	
<b>IF SYNTHESIZER PARAMETERS</b>						
ID <sub>o</sub> IF SOURCE	IF Charge Pump Output Source Current	VD <sub>o</sub> IF = V <sub>P</sub> IF/2 ID <sub>o</sub> IF Bit = 0 (Note 6)		-0.95		mA
		VD <sub>o</sub> IF = V <sub>P</sub> IF/2 ID <sub>o</sub> IF Bit = 1 (Note 6)		-3.80		mA
ID <sub>o</sub> IF SINK	IF Charge Pump Output Sink Current	VD <sub>o</sub> IF = V <sub>P</sub> IF/2 ID <sub>o</sub> IF Bit = 0 (Note 6)		0.95		mA
		VD <sub>o</sub> IF = V <sub>P</sub> IF/2 ID <sub>o</sub> IF Bit = 1 (Note 6)		3.80		mA
ID <sub>o</sub> IF TRI-STATE	IF Charge Pump Output TRI-STATE Current	$0.5\text{V} \leq \text{VD}_o \text{ IF} \leq V_P \text{ IF} - 0.5\text{V}$ (Note 6)	-2.5		2.5	nA
ID <sub>o</sub> IF SINK Vs ID <sub>o</sub> IF SOURCE	IF Charge Pump Output Sink Current Vs Charge Pump Output Source Current Mismatch	VD <sub>o</sub> IF = V <sub>P</sub> IF/2 T <sub>A</sub> = +25°C (Note 7)		3	10	%
ID <sub>o</sub> IF Vs VD <sub>o</sub> IF	IF Charge Pump Output Current Magnitude Variation Vs Charge Pump Output Voltage	$0.5\text{V} \leq \text{VD}_o \text{ IF} \leq V_P \text{ IF} - 0.5\text{V}$ T <sub>A</sub> = +25°C (Note 7)		10	15	%
ID <sub>o</sub> IF Vs T <sub>A</sub>	IF Charge Pump Output Current Magnitude Variation Vs Temperature	VD <sub>o</sub> IF = V <sub>P</sub> IF/2 (Note 7)		10		%
<b>OSCILLATOR PARAMETERS</b>						
F <sub>OSC</sub>	Oscillator Operating Frequency		2		40	MHz
V <sub>OSC</sub>	Oscillator Sensitivity	(Note 8)	0.5		V <sub>CC</sub>	V <sub>PP</sub>
I <sub>OSC</sub>	Oscillator Input Current	V <sub>OSC</sub> = V <sub>CC</sub> = 5.5V			100	μA
		V <sub>OSC</sub> = 0V, V <sub>CC</sub> = 5.5V	-100			μA
<b>DIGITAL INTERFACE (Data, LE, Clock, F<sub>o</sub>LD)</b>						
V <sub>IH</sub>	High-Level Input Voltage		0.8 V <sub>CC</sub>			V
V <sub>IL</sub>	Low-Level Input Voltage				0.2 V <sub>CC</sub>	V
I <sub>IH</sub>	High-Level Input Current	V <sub>IH</sub> = V <sub>CC</sub> = 5.5V	-1.0		1.0	μA
I <sub>IL</sub>	Low-Level Input Current	V <sub>IL</sub> = 0V, V <sub>CC</sub> = 5.5V	-1.0		1.0	μA
V <sub>OH</sub>	High-Level Output Voltage	I <sub>OH</sub> = -500 μA	V <sub>CC</sub> - 0.4			V
V <sub>OL</sub>	Low-Level Output Voltage	I <sub>OL</sub> = 500 μA			0.4	V
<b>MICROWIRE INTERFACE</b>						
t <sub>CS</sub>	Data to Clock Set Up Time	(Note 9)	50			ns
t <sub>CH</sub>	Data to Clock Hold Time	(Note 9)	10			ns
t <sub>CWH</sub>	Clock Pulse Width HIGH	(Note 9)	50			ns
t <sub>CWL</sub>	Clock Pulse Width LOW	(Note 9)	50			ns
t <sub>ES</sub>	Clock to Load Enable Set Up Time	(Note 9)	50			ns
t <sub>EW</sub>	Latch Enable Pulse Width	(Note 9)	50			ns

### Electrical Characteristics (Continued)

$V_{CC} = V_P$  RF =  $V_P$  IF = 3.0V,  $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ , unless otherwise specified

Symbol	Parameter	Conditions	Value			Units
			Min	Typ	Max	
<b>PHASE NOISE CHARACTERISTICS</b>						
$L_N(f)$ RF	RF Synthesizer Normalized Phase Noise Contribution (Note 10)	TCXO Reference Source ID <sub>o</sub> RF Bit = 1		-212.0		dBc/Hz
$L(f)$ RF	RF Synthesizer Single Side Band Phase Noise Measured	LMX2330U	$f_{IN}$ RF = 2450 MHz $f$ = 1 kHz Offset $F_{\phi RF}$ = 200 kHz Loop Bandwidth = 7.5 kHz $N$ = 12250 $F_{OSC}$ = 10 MHz $V_{OSC}$ = 0.632 $V_{PP}$ ID <sub>o</sub> RF Bit = 1 PWDN IF Bit = 1 $T_A$ = +25°C (Note 11)	-77.24		dBc/Hz
		LMX2331U	$f_{IN}$ RF = 1960 MHz $f$ = 1 kHz Offset $F_{\phi RF}$ = 200 kHz Loop Bandwidth = 15 kHz $N$ = 9800 $F_{OSC}$ = 10 MHz $V_{OSC}$ = 0.632 $V_{PP}$ ID <sub>o</sub> RF Bit = 1 PWDN IF Bit = 1 $T_A$ = +25°C (Note 11)	-79.18		dBc/Hz
		LMX2332U	$f_{IN}$ RF = 900 MHz $f$ = 1 kHz Offset $F_{\phi RF}$ = 200 kHz Loop Bandwidth = 12 kHz $N$ = 4500 $F_{OSC}$ = 10 MHz $V_{OSC}$ = 0.632 $V_{PP}$ ID <sub>o</sub> RF Bit = 1 PWDN IF Bit = 1 $T_A$ = +25°C (Note 11)	-85.94		dBc/Hz

## Electrical Characteristics (Continued)

$V_{CC} = V_P$  RF =  $V_P$  IF = 3.0V,  $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ , unless otherwise specified

Symbol	Parameter		Conditions	Value			Units
				Min	Typ	Max	
<b>PHASE NOISE CHARACTERISTICS</b>							
$L_N(f)$ IF	IF Synthesizer Normalized Phase Noise Contribution (Note 10)		TCXO Reference Source $ID_o$ IF Bit = 1		-212.0		dBc/Hz
$L(f)$ IF	IF Synthesizer Single Side Band Phase Noise Measured	LMX233xU	$f_{IN}$ IF = 200 MHz $f = 1$ kHz Offset $F_{\phi IF} = 200$ kHz Loop Bandwidth = 18 kHz $N = 1000$ $F_{OSC} = 10$ MHz $V_{OSC} = 0.632 V_{PP}$ $ID_o$ IF Bit = 1 PWDN RF Bit = 1 $T_A = +25^{\circ}\text{C}$ (Note 11)		-99.00		dBc/Hz

**Note 4:** Some of the values in this range are illegal divide ratios ( $B < A$ ). To obtain continuous legal division, the Minimum Divide Ratio must be calculated. Use  $N \geq P * (P-1)$ , where P is the value of the prescaler selected.

**Note 5:** Refer to the LMX233xU  $f_{IN}$  Sensitivity Test Setup section

**Note 6:** Refer to the LMX233xU Charge Pump Test Setup section

**Note 7:** Refer to the Charge Pump Current Specification Definitions for details on how these measurements are made.

**Note 8:** Refer to the LMX233xU  $OSC_{in}$  Sensitivity Test Setup section

**Note 9:** Refer to the LMX233xU Serial Data Input Timing section

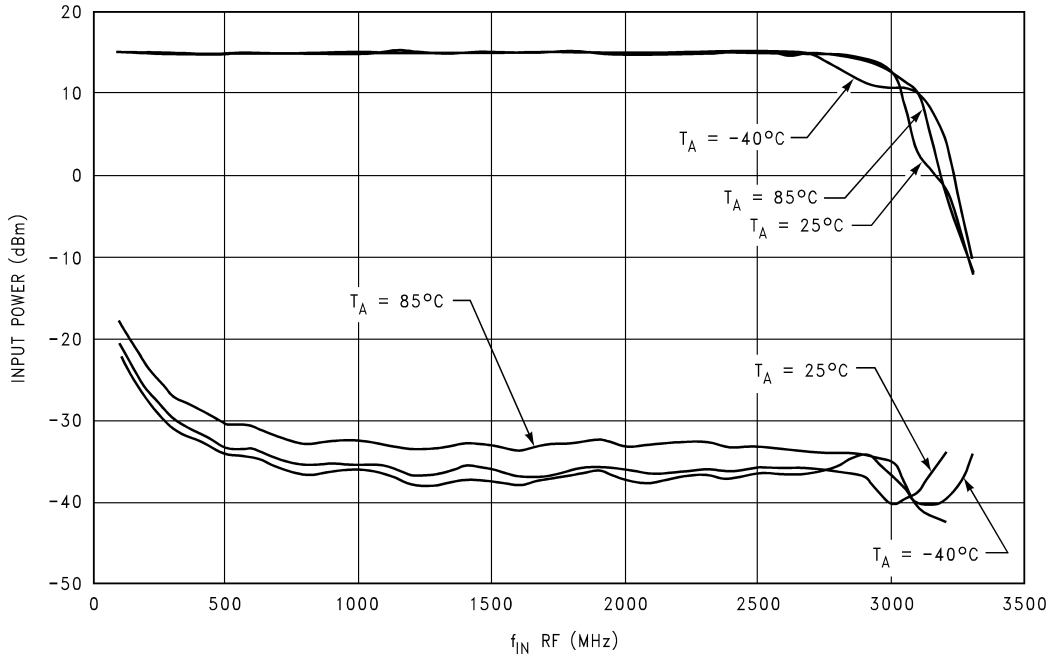
**Note 10:** Normalized Phase Noise Contribution is defined as :  $L_N(f) = L(f) - 20 \log(N) - 10 \log(F_{\phi})$ , where  $L(f)$  is defined as the single side band phase noise measured at an offset frequency,  $f$ , in a 1 Hz bandwidth. The offset frequency,  $f$ , must be chosen sufficiently smaller than the PLL's loop bandwidth, yet large enough to avoid substantial phase noise contribution from the reference source.  $N$  is the value selected for the feedback divider and  $F_{\phi}$  is the RF/IF phase detector comparison frequency.

**Note 11:** The synthesizer phase noise is measured with the LMX2330TMEB/LMX2330SLBEB Evaluation boards and the HP8566B Spectrum Analyzer.

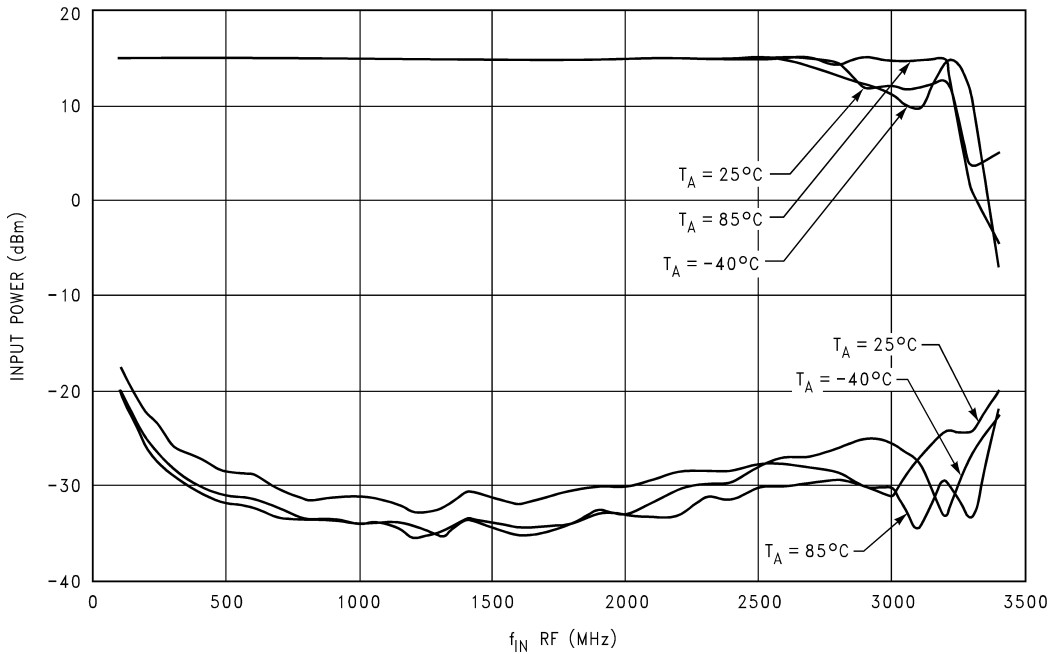
# Typical Performance Characteristics

## Sensitivity

LMX2330U  $f_{IN}$  RF Input Power Vs Frequency  
 $V_{CC} = V_P$  RF = 3.0V



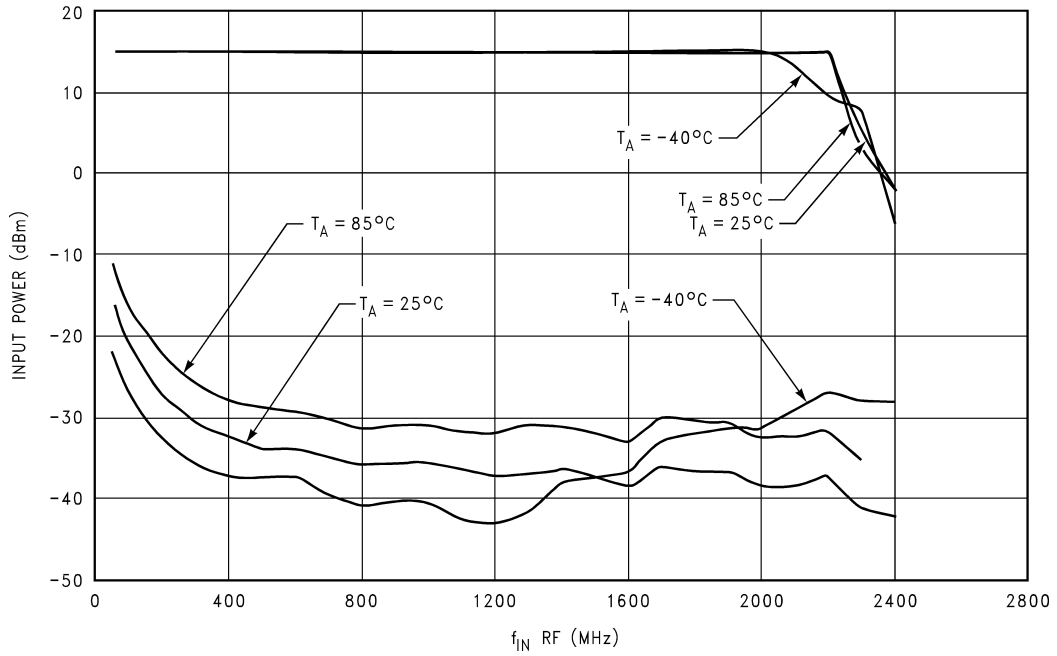
LMX2330U  $f_{IN}$  RF Input Power Vs Frequency  
 $V_{CC} = V_P$  RF = 5.5V



# Typical Performance Characteristics

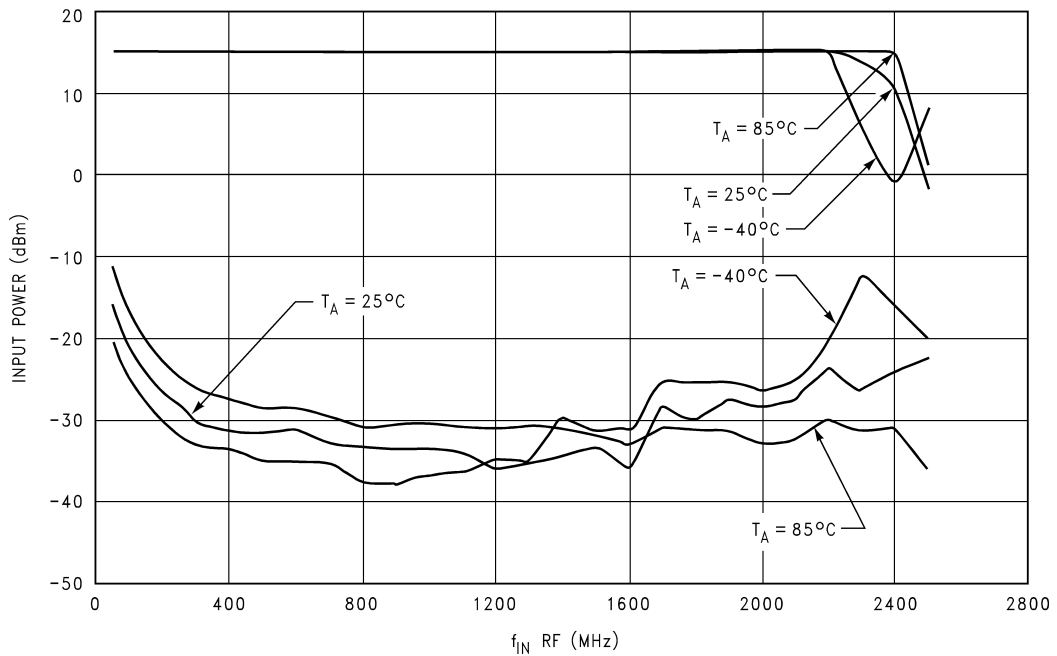
## Sensitivity (Continued)

LMX2331U  $f_{IN}$  RF Input Power Vs Frequency  
 $V_{CC} = V_P$  RF = 3.0V



10136644

LMX2331U  $f_{IN}$  RF Input Power Vs Frequency  
 $V_{CC} = V_P$  RF = 5.5V

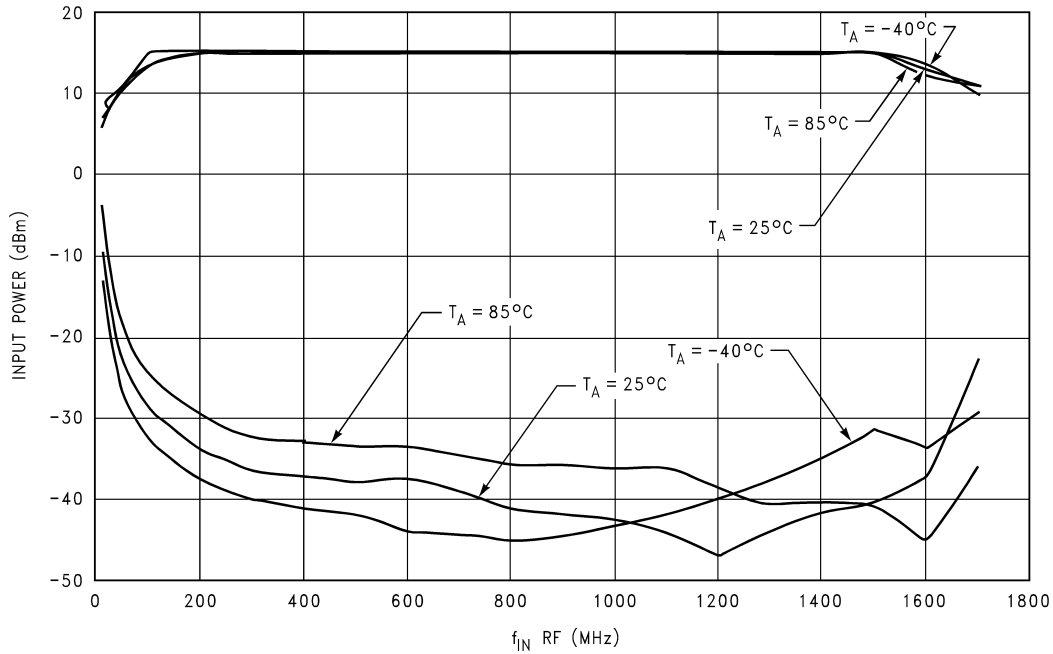


10136645

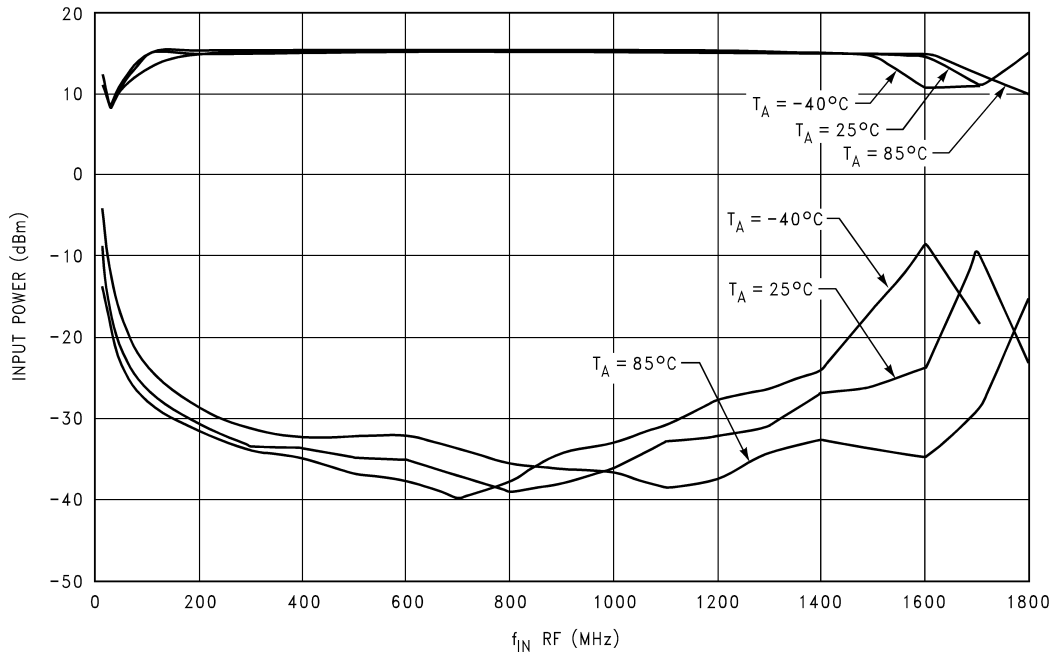
# Typical Performance Characteristics

## Sensitivity (Continued)

LMX2332U  $f_{IN}$  RF Input Power Vs Frequency  
 $V_{CC} = V_P$  RF = 3.0V



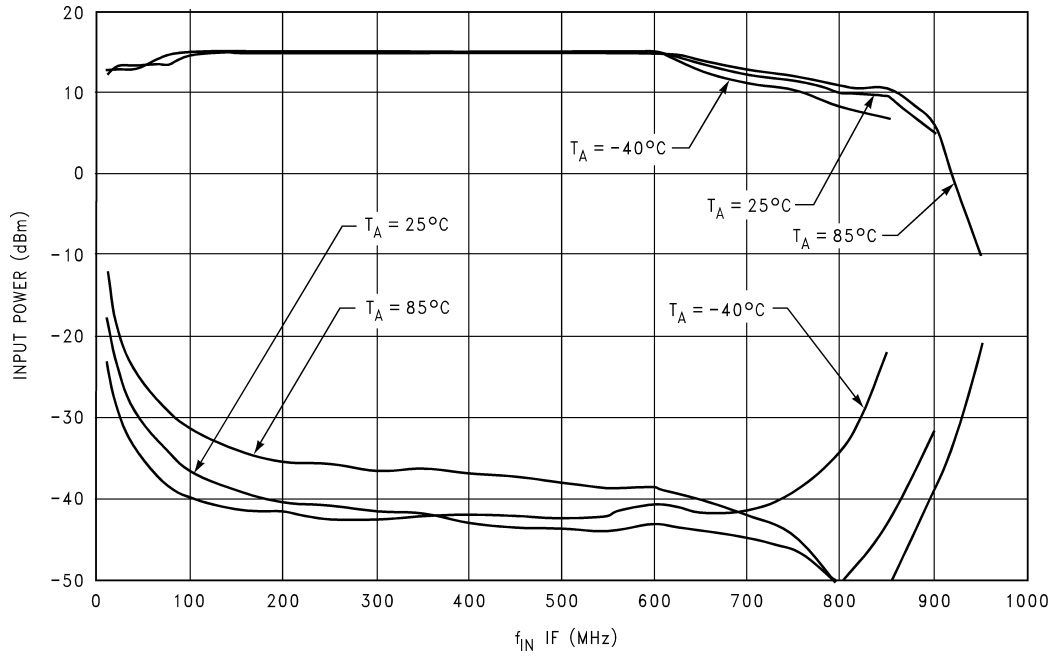
LMX2332U  $f_{IN}$  RF Input Power Vs Frequency  
 $V_{CC} = V_P$  RF = 5.5V



# Typical Performance Characteristics

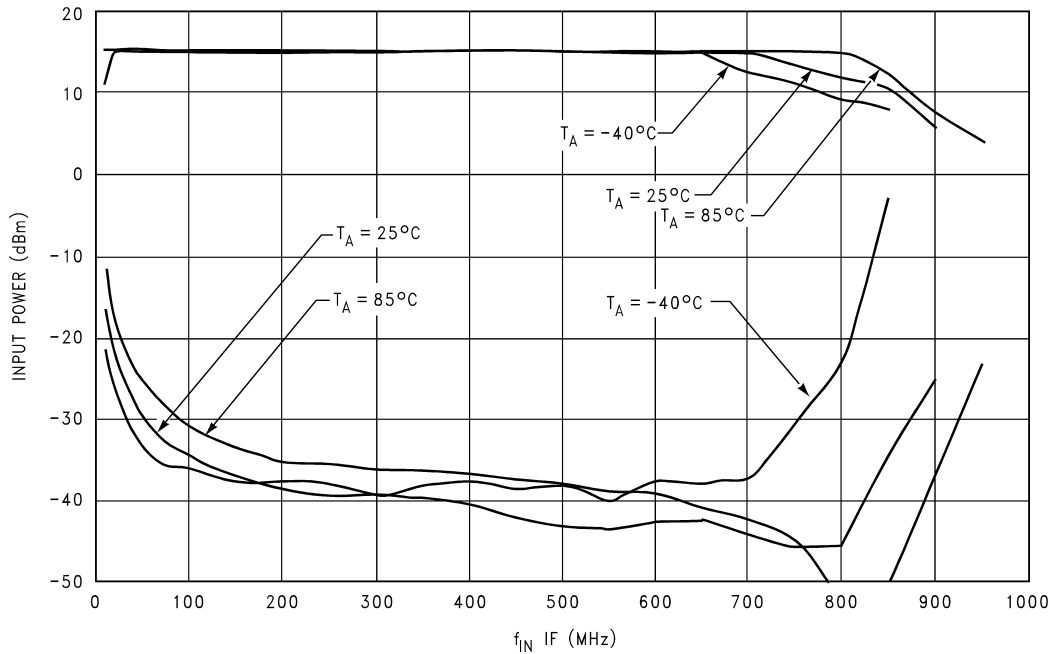
## Sensitivity (Continued)

LMX233xU  $f_{IN}$  IF Input Power Vs Frequency  
 $V_{CC} = V_P$  IF = 3.0V



10136648

LMX233xU  $f_{IN}$  IF Input Power Vs Frequency  
 $V_{CC} = V_P$  IF = 5.5V

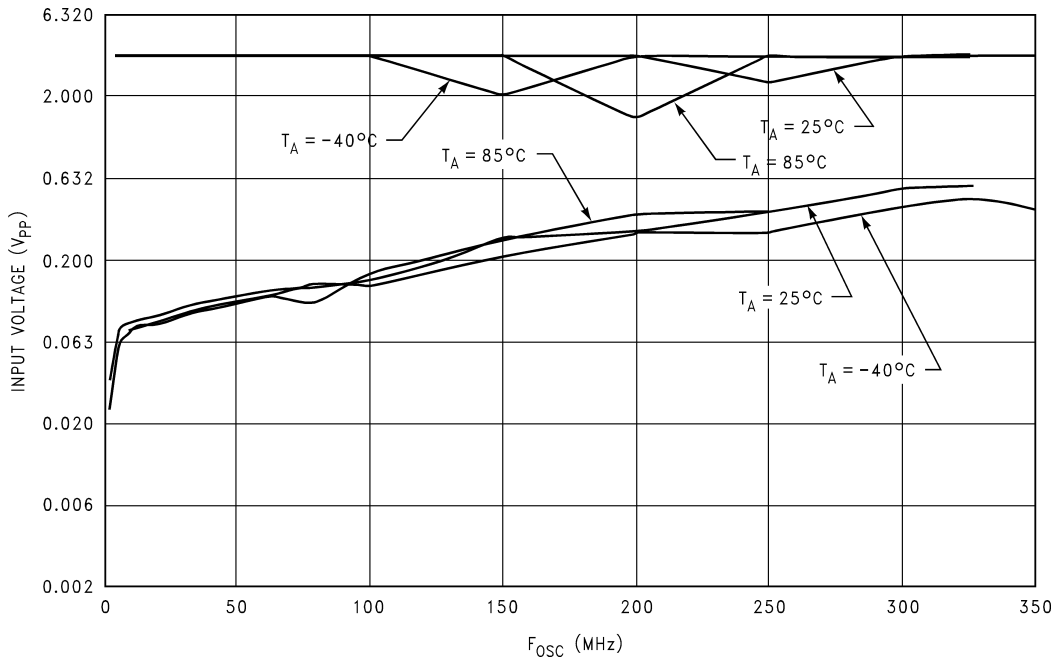


10136649

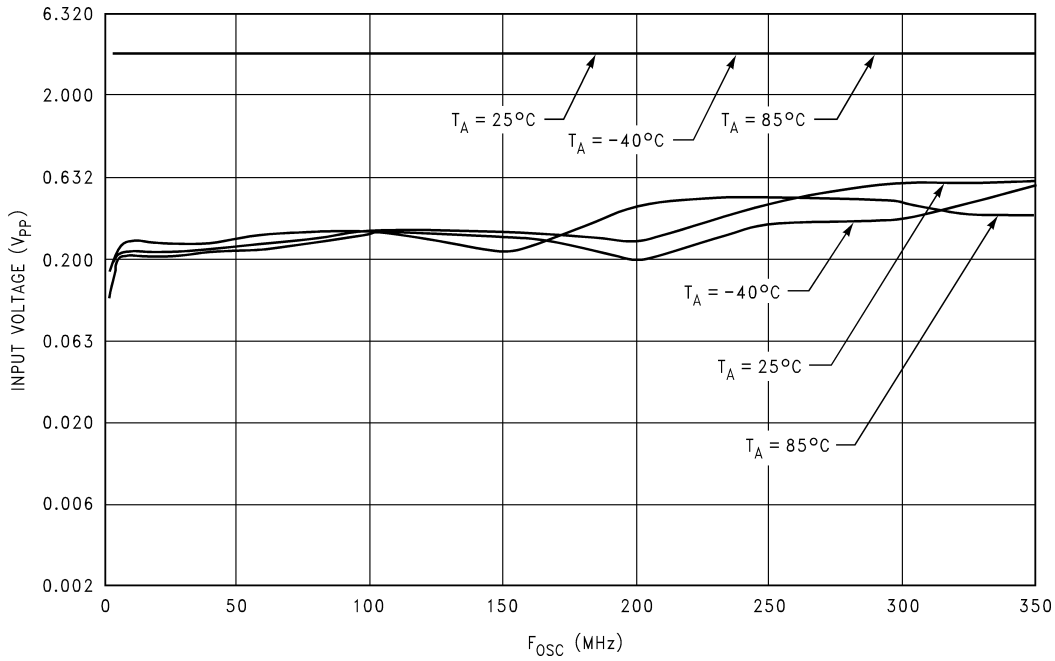
# Typical Performance Characteristics

## Sensitivity (Continued)

LMX233xU OSC<sub>in</sub> Input Voltage Vs Frequency  
V<sub>CC</sub> = 3.0V

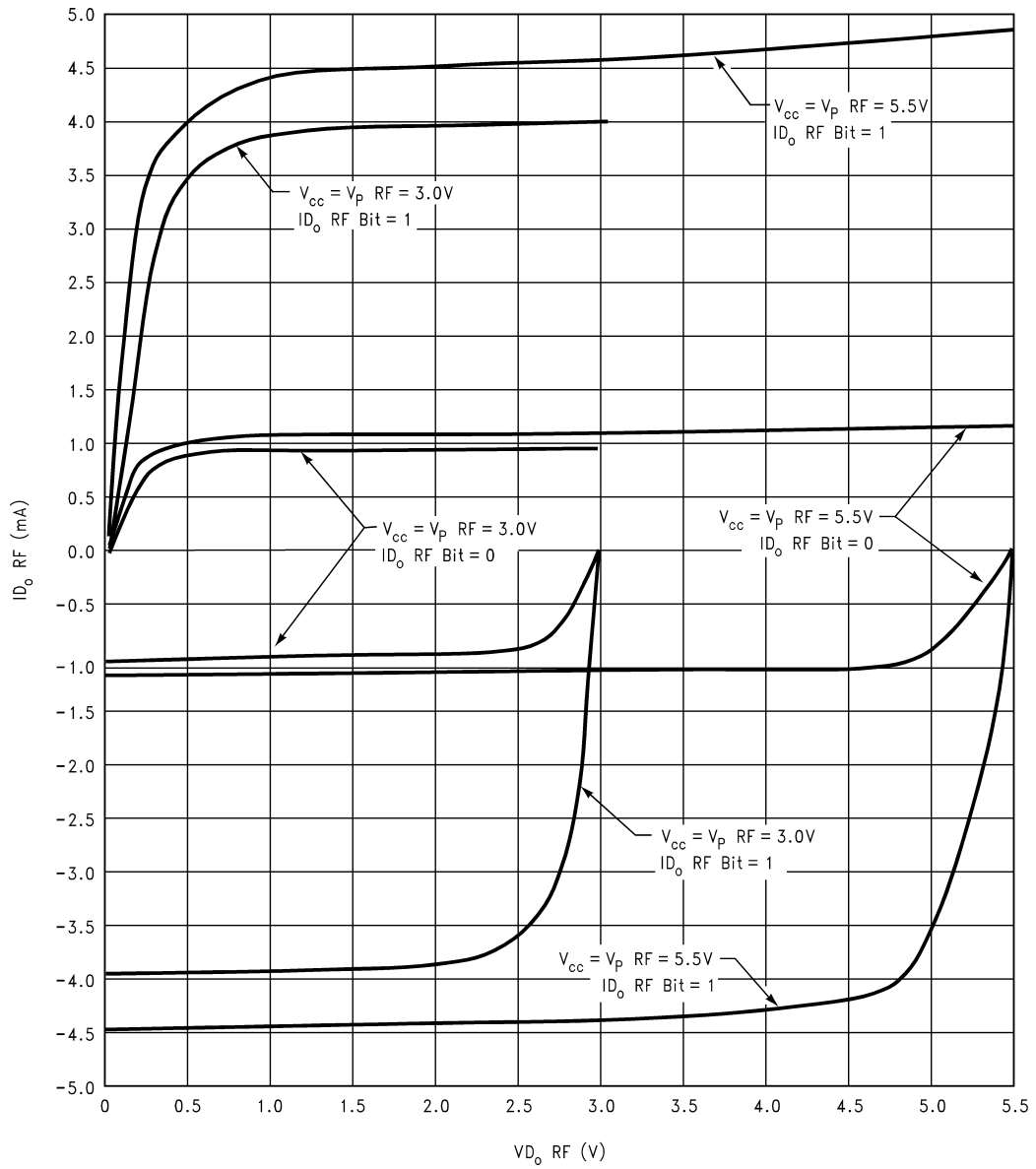


LMX233xU OSC<sub>in</sub> Input Voltage Vs Frequency  
V<sub>CC</sub> = 5.5V



# Typical Performance Characteristics Charge Pump

LMX233xU RF Charge Pump Sweeps  
 $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$

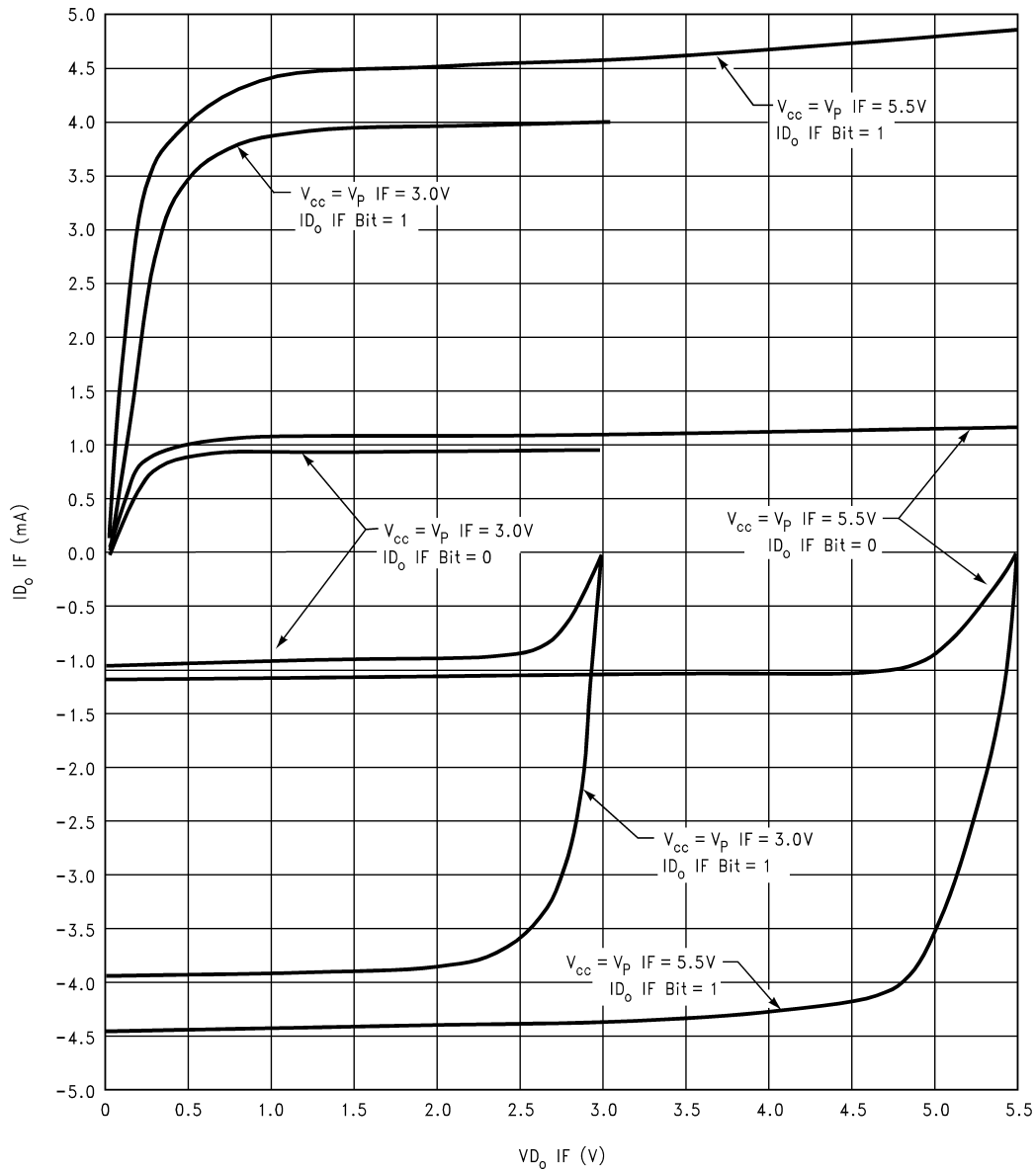


10136660

# Typical Performance Characteristics

## Charge Pump (Continued)

LMX233xU IF Charge Pump Sweeps  
 $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$

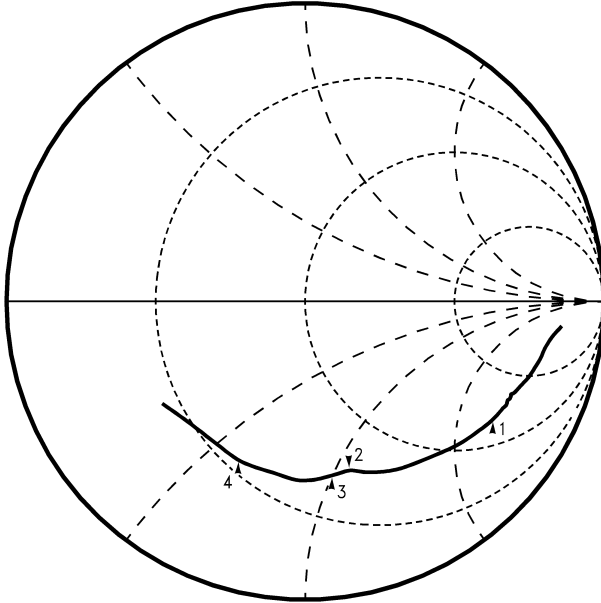


10136661

# Typical Performance Characteristics

## Input Impedance

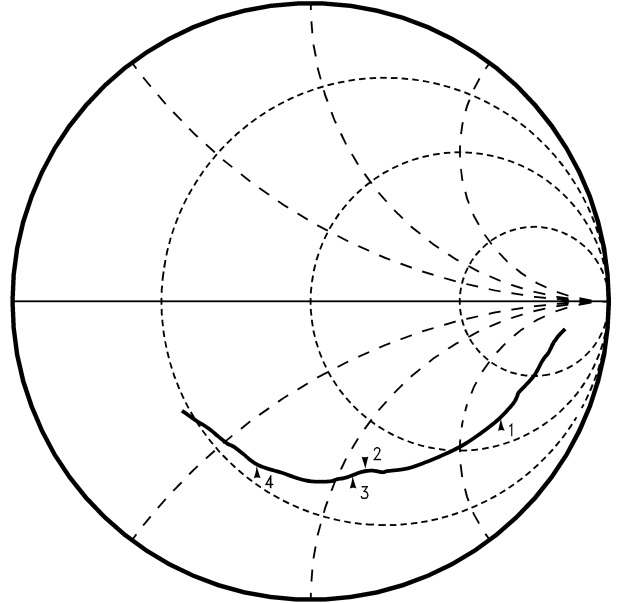
LMX233xU TSSOP  $f_{IN}$  RF Input Impedance  
 $V_{CC} = 3.0V, T_A = +25^\circ C$



Marker 1 = 900 MHz  
 Marker 2 = 1800 MHz  
 Marker 3 = 1900 MHz  
 Marker 4 = 2500 MHz

10136666

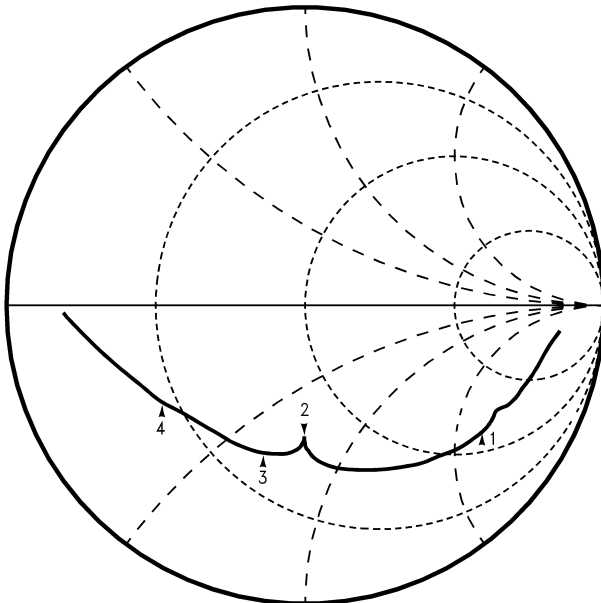
LMX233xU TSSOP  $f_{IN}$  RF Input Impedance  
 $V_{CC} = 5.5V, T_A = +25^\circ C$



Marker 1 = 900 MHz  
 Marker 2 = 1800 MHz  
 Marker 3 = 1900 MHz  
 Marker 4 = 2500 MHz

10136667

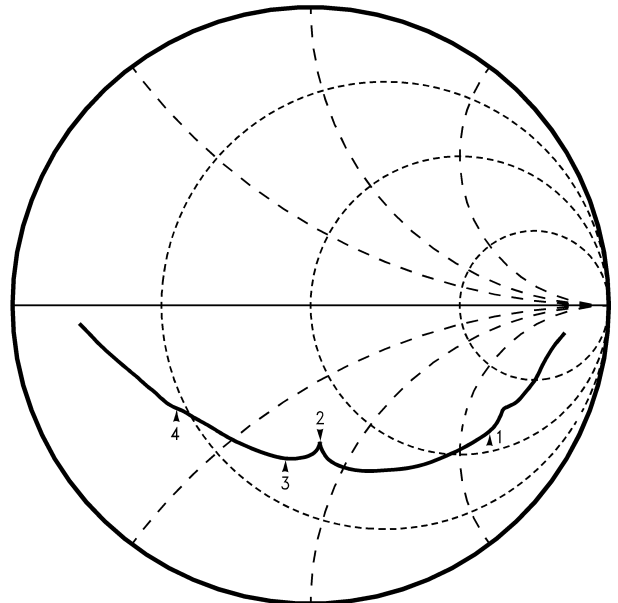
LMX233xU CSP  $f_{IN}$  RF Input Impedance  
 $V_{CC} = 3.0V, T_A = +25^\circ C$



Marker 1 = 900 MHz  
 Marker 2 = 1800 MHz  
 Marker 3 = 1900 MHz  
 Marker 4 = 2500 MHz

10136668

LMX233xU CSP  $f_{IN}$  RF Input Impedance  
 $V_{CC} = 5.5V, T_A = +25^\circ C$



Marker 1 = 900 MHz  
 Marker 2 = 1800 MHz  
 Marker 3 = 1900 MHz  
 Marker 4 = 2500 MHz

10136669

# Typical Performance Characteristics

## Input Impedance (Continued)

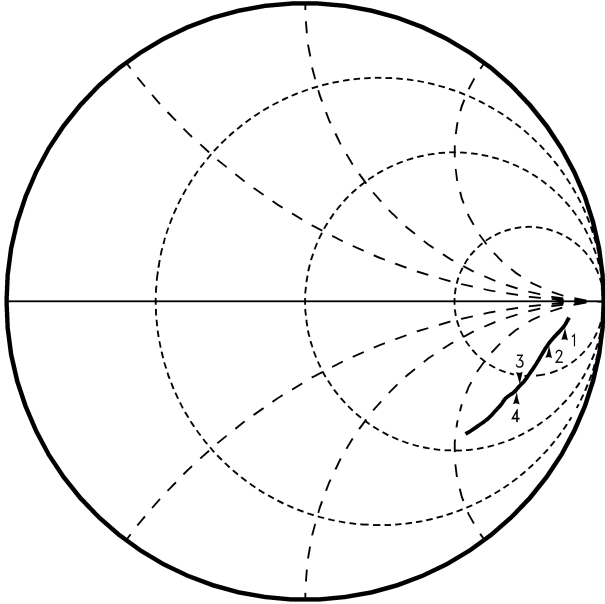
LMX233xU TSSOP and LMX233xU CSP  $f_{in}$  RF Input Impedance Table

$f_{in}$ RF (MHz)	LMX233xU TSSOP $Z_{in}$ RF						LMX233xU CSP $Z_{in}$ RF													
	$V_{cc} = V_p$ RF = 3.0V ( $T_A = 25^\circ\text{C}$ )			$V_{cc} = V_p$ RF = 5.5V ( $T_A = 25^\circ\text{C}$ )			$V_{cc} = V_p$ RF = 3.0V ( $T_A = 25^\circ\text{C}$ )			$V_{cc} = V_p$ RF = 5.5V ( $T_A = 25^\circ\text{C}$ )										
	$\angle\Gamma$	$R_{Z_{in}}$ RF ( $\Omega$ )	$\eta_{in}$ $Z_{in}$ RF ( $\Omega$ )	$\angle\Gamma$	$R_{Z_{in}}$ RF ( $\Omega$ )	$\eta_{in}$ $Z_{in}$ RF ( $\Omega$ )	$\angle\Gamma$	$R_{Z_{in}}$ RF ( $\Omega$ )	$\eta_{in}$ $Z_{in}$ RF ( $\Omega$ )	$\angle\Gamma$	$R_{Z_{in}}$ RF ( $\Omega$ )	$\eta_{in}$ $Z_{in}$ RF ( $\Omega$ )								
100	0.862	-6.23	499.774	-319.866	543.798	0.862	-6.07	448.230	-318.841	550.064	0.864	-6.44	431.004	-330.013	542.838	0.864	-6.30	438.240	-327.814	547.281
200	0.834	-9.30	307.614	-272.274	410.803	0.834	-9.00	316.479	-271.581	417.031	0.836	-9.88	291.252	-277.923	402.577	0.836	-9.57	300.190	-277.552	408.838
300	0.820	-12.11	237.700	-249.291	344.452	0.821	-11.66	247.264	-251.098	352.406	0.821	-13.24	215.318	-248.361	328.702	0.821	-12.76	224.624	-249.637	335.819
400	0.808	-15.25	185.048	-227.171	293.001	0.808	-14.61	194.668	-229.054	300.601	0.808	-16.88	163.190	-219.893	273.832	0.808	-16.24	171.345	-222.518	280.844
500	0.796	-18.51	147.785	-203.923	251.843	0.796	-17.66	156.935	-207.313	260.014	0.793	-20.90	126.193	-191.939	229.707	0.794	-20.00	133.885	-196.200	237.528
600	0.781	-21.81	122.091	-181.461	218.710	0.782	-20.70	130.906	-185.850	227.325	0.775	-24.82	102.956	-168.026	197.060	0.777	-23.70	109.531	-172.887	204.663
700	0.765	-24.72	106.107	-163.758	195.129	0.767	-23.45	113.780	-168.514	203.329	0.749	-28.29	90.820	-146.582	172.437	0.752	-27.02	96.279	-151.333	179.363
800	0.760	-28.35	87.984	-150.524	174.352	0.762	-26.97	94.255	-155.481	181.819	0.742	-31.22	79.737	-136.782	158.327	0.746	-29.85	84.470	-141.473	164.772
<b>900</b>	<b>0.747</b>	<b>-32.60</b>	<b>73.777</b>	<b>-134.500</b>	<b>153.406</b>	<b>0.750</b>	<b>-30.95</b>	<b>79.270</b>	<b>-139.668</b>	<b>160.596</b>	<b>0.739</b>	<b>-36.04</b>	<b>64.577</b>	<b>-123.951</b>	<b>139.764</b>	<b>0.742</b>	<b>-34.37</b>	<b>69.006</b>	<b>-128.610</b>	<b>145.954</b>
1000	0.732	-36.68	64.122	-120.908	136.859	0.735	-34.73	69.215	-126.104	143.851	0.719	-41.44	55.019	-108.415	121.577	0.723	-39.46	58.684	-113.123	127.439
1100	0.717	-41.25	55.780	-108.398	121.908	0.720	-39.12	60.041	-113.215	128.151	0.694	-47.27	48.056	-94.403	105.931	0.698	-45.08	51.159	-98.547	111.035
1200	0.698	-46.24	49.180	-96.605	108.403	0.702	-43.84	52.848	-101.254	114.216	0.669	-53.59	42.269	-82.401	92.610	0.674	-51.01	45.061	-86.388	97.434
1300	0.678	-51.43	43.982	-86.291	96.853	0.683	-48.77	47.173	-90.676	102.212	0.641	-60.42	37.856	-71.653	81.039	0.647	-57.50	40.230	-75.400	85.461
1400	0.663	-56.68	39.397	-77.901	87.296	0.667	-53.71	42.317	-82.070	92.337	0.610	-68.33	34.108	-61.481	70.308	0.613	-64.90	36.477	-64.872	74.424
1500	0.649	-62.08	35.566	-70.500	78.963	0.653	-58.74	38.281	-74.569	83.821	0.577	-77.01	31.049	-52.388	60.898	0.581	-73.18	33.064	-55.554	64.649
1600	0.630	-67.58	32.912	-63.544	71.562	0.634	-63.96	35.335	-67.423	76.121	0.539	-84.86	29.732	-44.952	53.895	0.543	-80.36	31.654	-48.119	57.597
1700	0.608	-72.22	31.565	-57.996	66.030	0.614	-68.51	33.590	-61.632	70.191	0.477	-97.97	26.359	-35.225	43.264	0.487	-94.99	33.106	-42.105	53.562
<b>1800</b>	<b>0.596</b>	<b>-75.66</b>	<b>30.440</b>	<b>-54.462</b>	<b>62.392</b>	<b>0.601</b>	<b>-71.81</b>	<b>32.358</b>	<b>-57.943</b>	<b>66.366</b>	<b>0.455</b>	<b>89.90</b>	<b>32.829</b>	<b>-37.624</b>	<b>49.933</b>	<b>0.468</b>	<b>-85.87</b>	<b>33.886</b>	<b>-40.554</b>	<b>52.847</b>
<b>1900</b>	<b>0.598</b>	<b>-80.06</b>	<b>27.915</b>	<b>-51.164</b>	<b>58.284</b>	<b>0.602</b>	<b>-76.22</b>	<b>29.678</b>	<b>-54.335</b>	<b>61.912</b>	<b>0.493</b>	<b>87.34</b>	<b>29.357</b>	<b>-38.214</b>	<b>48.189</b>	<b>0.500</b>	<b>-88.90</b>	<b>29.576</b>	<b>-39.369</b>	<b>49.241</b>
2000	0.607	-85.31	24.914	-47.651	53.771	0.607	-81.32	26.675	-50.603	57.203	0.520	79.89	25.120	-35.225	43.264	0.521	84.05	26.396	-37.576	45.921
2100	0.612	89.24	22.502	-43.994	49.414	0.611	-86.42	21.612	42.064	47.292	0.529	70.97	22.177	-30.771	37.930	0.525	75.52	23.556	-33.043	40.580
2200	0.605	84.09	21.289	-40.358	45.629	0.602	88.61	22.901	-43.251	48.940	0.531	61.99	20.155	-26.331	33.159	0.524	66.93	21.544	-28.595	35.802
2300	0.594	78.44	20.367	-36.566	41.855	0.589	83.13	21.961	-39.298	45.018	0.533	52.71	18.533	-21.975	28.747	0.525	57.61	19.706	-24.119	31.146
2400	0.590	72.27	19.111	-32.907	38.054	0.584	77.11	20.598	-35.536	41.074	0.550	43.18	16.578	-17.883	24.385	0.537	47.69	17.671	-19.749	26.501
<b>2500</b>	<b>0.586</b>	<b>67.24</b>	<b>18.297</b>	<b>-30.064</b>	<b>35.194</b>	<b>0.576</b>	<b>72.09</b>	<b>19.792</b>	<b>-32.516</b>	<b>38.066</b>	<b>0.563</b>	<b>34.44</b>	<b>14.340</b>	<b>-14.328</b>	<b>20.272</b>	<b>0.566</b>	<b>38.69</b>	<b>15.416</b>	<b>-16.055</b>	<b>22.257</b>

# Typical Performance Characteristics

## Input Impedance (Continued)

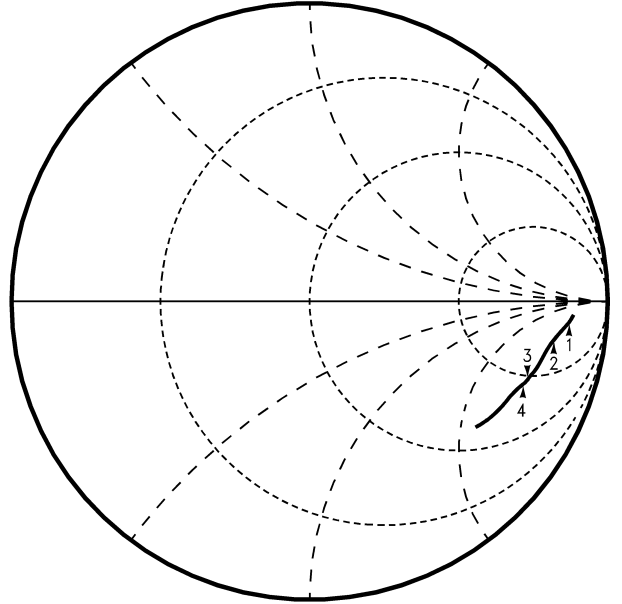
LMX233xU TSSOP  $f_{IN}$  IF Input Impedance  
 $V_{CC} = 3.0V, T_A = +25^\circ C$



Marker 1 = 50 MHz  
 Marker 2 = 200 MHz  
 Marker 3 = 500 MHz  
 Marker 4 = 600 MHz

10136671

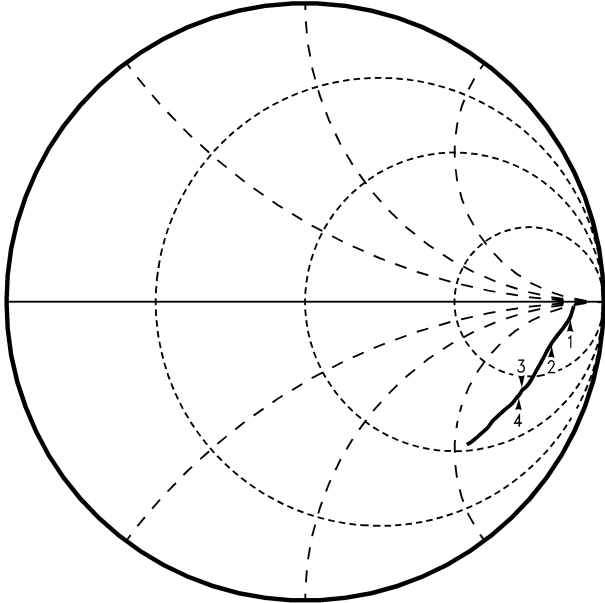
LMX233xU TSSOP  $f_{IN}$  IF Input Impedance  
 $V_{CC} = 5.5V, T_A = +25^\circ C$



Marker 1 = 50 MHz  
 Marker 2 = 200 MHz  
 Marker 3 = 500 MHz  
 Marker 4 = 600 MHz

10136672

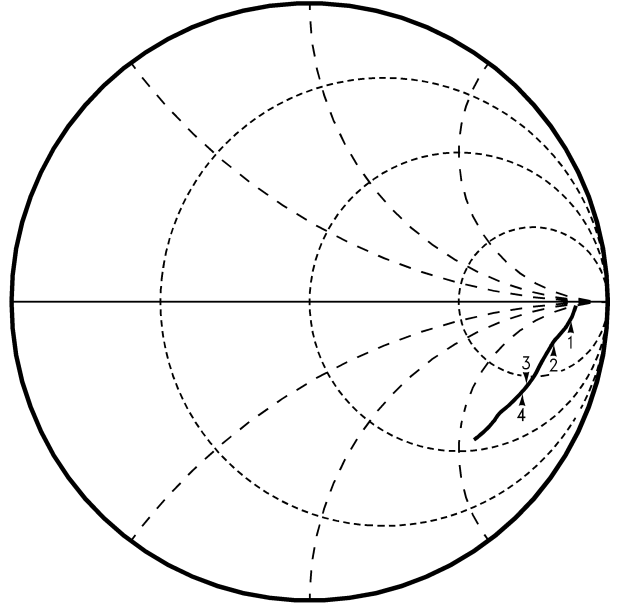
LMX233xU CSP  $f_{IN}$  IF Input Impedance  
 $V_{CC} = 3.0V, T_A = +25^\circ C$



Marker 1 = 50 MHz  
 Marker 2 = 200 MHz  
 Marker 3 = 500 MHz  
 Marker 4 = 600 MHz

10136673

LMX233xU CSP  $f_{IN}$  IF Input Impedance  
 $V_{CC} = 5.5V, T_A = +25^\circ C$



Marker 1 = 50 MHz  
 Marker 2 = 200 MHz  
 Marker 3 = 500 MHz  
 Marker 4 = 600 MHz

10136674

# Typical Performance Characteristics

## Input Impedance (Continued)

LMX233xU TSSOP and LMX233xU CSP  $f_{in}$  IF Input Impedance Table

$f_{in}$ IF (MHz)	LMX233xU TSSOP $Z_{in}$ IF						LMX233xU CSP $Z_{in}$ IF													
	$V_{cc} = V_p$ IF = 3.0V ( $T_A = 25^\circ\text{C}$ )			$V_{cc} = V_p$ IF = 5.5V ( $T_A = 25^\circ\text{C}$ )			$V_{cc} = V_p$ IF = 3.0V ( $T_A = 25^\circ\text{C}$ )			$V_{cc} = V_p$ IF = 5.5V ( $T_A = 25^\circ\text{C}$ )										
	$\angle\Gamma$	$R_{in}$ $Z_{in}$ IF ( $\Omega$ )	$\rho_{in}$ $Z_{in}$ IF ( $\Omega$ )	$\angle\Gamma$	$R_{in}$ $Z_{in}$ IF ( $\Omega$ )	$\rho_{in}$ $Z_{in}$ IF ( $\Omega$ )	$\angle\Gamma$	$R_{in}$ $Z_{in}$ IF ( $\Omega$ )	$\rho_{in}$ $Z_{in}$ IF ( $\Omega$ )	$\angle\Gamma$	$R_{in}$ $Z_{in}$ IF ( $\Omega$ )	$\rho_{in}$ $Z_{in}$ IF ( $\Omega$ )								
50	0.884	-3.93	621.523	-345.924	711.305	0.885	-3.81	630.568	-340.995	716.864	0.899	-1.69	874.934	-242.583	907.940	0.899	-1.67	874.127	-239.189	906.261
75	0.873	-5.30	503.424	-340.786	607.923	0.873	-5.18	511.352	-338.259	613.107	0.891	-3.44	683.122	-354.024	769.408	0.891	-3.33	692.599	-349.036	775.577
100	0.861	-6.42	429.629	-319.996	535.704	0.861	-6.24	438.666	-318.001	541.805	0.880	-4.98	535.334	-360.736	645.533	0.879	-4.85	543.967	-357.157	650.739
125	0.851	-7.27	384.494	-301.186	488.414	0.852	-7.10	391.664	-300.482	493.650	0.868	-6.23	445.309	-339.295	559.840	0.868	-6.06	454.188	-337.263	565.715
150	0.844	-8.11	349.099	-288.744	453.038	0.844	-7.90	356.461	-287.182	457.753	0.858	-7.26	388.975	-319.049	503.085	0.858	-7.07	397.015	-317.892	508.603
175	0.837	-8.85	322.082	-276.707	424.622	0.837	-8.57	330.546	-275.058	430.020	0.850	-8.18	348.616	-303.517	462.229	0.850	-7.98	356.200	-303.914	468.233
200	0.832	-9.54	300.314	-268.356	402.745	0.832	-9.22	309.296	-267.480	408.913	0.843	-9.07	316.481	-291.646	430.369	0.844	-8.84	324.033	-291.128	435.606
225	0.827	-10.29	279.576	-260.995	382.467	0.827	-9.95	288.264	-260.187	388.322	0.838	-9.93	289.893	-282.342	404.666	0.839	-9.66	297.640	-282.345	410.254
250	0.823	-11.04	261.205	-254.758	364.870	0.823	-10.64	270.659	-254.417	371.462	0.834	-10.77	267.263	-274.027	382.780	0.834	-10.45	275.672	-273.085	388.034
275	0.819	-11.80	244.399	-248.227	348.350	0.818	-11.38	253.507	-247.511	354.299	0.830	-11.63	247.024	-265.175	362.407	0.829	-11.24	256.102	-265.264	368.719
300	0.814	-12.58	228.964	-241.239	332.597	0.815	-12.14	237.587	-241.965	339.109	0.826	-12.50	228.671	-257.705	344.532	0.826	-12.08	237.603	-257.879	350.652
325	0.812	-13.36	214.910	-236.082	319.251	0.811	-12.84	224.277	-236.738	326.106	0.823	-13.38	212.305	-250.287	328.203	0.822	-12.90	221.471	-251.212	334.899
350	0.807	-14.18	201.728	-228.591	304.874	0.807	-13.62	210.927	-230.202	312.223	0.819	-14.23	198.231	-242.453	313.176	0.819	-13.73	206.868	-244.557	320.316
375	0.804	-14.98	189.889	-223.629	293.373	0.804	-14.44	198.121	-224.602	299.497	0.816	-15.21	183.656	-234.712	298.025	0.815	-14.63	192.740	-236.735	305.274
400	0.801	-15.85	178.372	-217.315	281.144	0.801	-15.20	187.401	-219.200	288.388	0.812	-16.09	172.185	-227.189	285.066	0.812	-15.48	180.755	-229.880	292.433
425	0.797	-16.72	167.895	-211.342	269.915	0.797	-16.02	176.917	-213.413	277.208	0.809	-17.02	160.959	-220.345	272.873	0.808	-16.36	169.600	-222.898	280.085
450	0.794	-17.57	158.542	-205.691	259.700	0.794	-16.81	167.586	-208.198	267.267	0.805	-17.99	150.694	-213.253	261.124	0.805	-17.28	158.914	-216.102	268.242
475	0.790	-18.41	150.375	-199.750	250.026	0.791	-17.67	158.301	-202.585	257.099	0.802	-18.98	141.126	-206.449	250.075	0.802	-18.16	149.611	-210.221	258.024
500	0.787	-19.24	142.803	-194.502	241.295	0.787	-18.43	150.871	-197.426	248.474	0.799	-19.92	132.835	-200.384	240.414	0.799	-19.09	140.765	-204.004	247.856
525	0.783	-20.10	135.793	-188.890	232.635	0.783	-19.20	144.065	-192.240	240.231	0.796	-20.90	125.186	-193.960	230.851	0.796	-20.03	132.797	-197.693	238.154
550	0.779	-20.93	129.745	-183.353	224.616	0.780	-19.97	137.814	-187.051	232.338	0.793	-21.89	118.197	-187.808	221.906	0.792	-20.97	125.698	-191.502	229.070
575	0.775	-21.73	124.298	-178.182	217.253	0.776	-20.75	131.967	-182.250	224.954	0.789	-22.85	112.161	-181.851	213.658	0.789	-21.92	118.871	-185.881	220.640
600	0.770	-22.59	119.110	-172.763	209.843	0.771	-21.53	126.693	-176.798	217.506	0.785	-23.86	106.393	-175.910	205.581	0.785	-22.85	113.154	-180.132	212.723

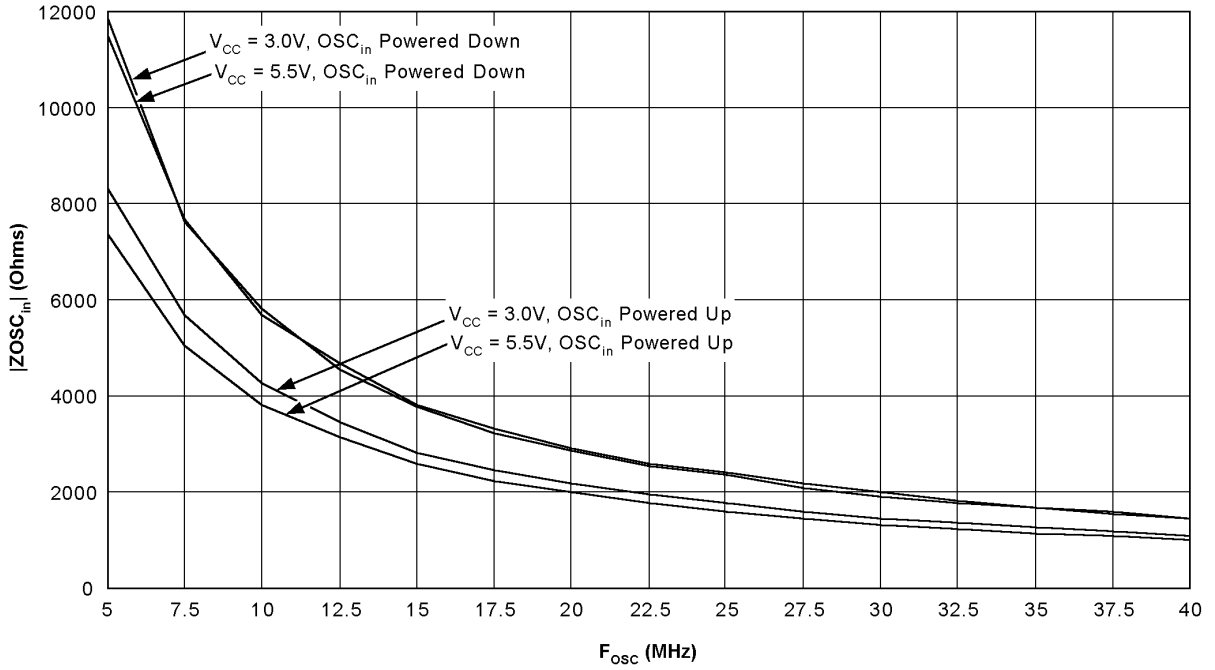
10136675

LMX2330U/LMX2331U/LMX2332U

# Typical Performance Characteristics

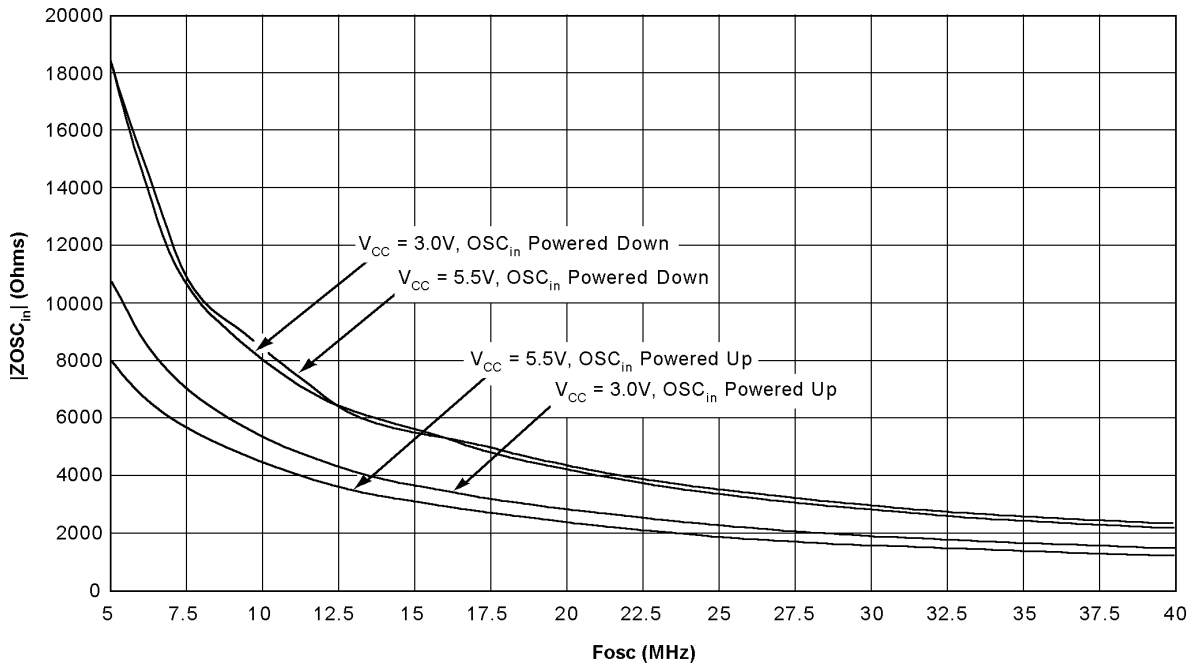
## Input Impedance (Continued)

LMX233xU TSSOP OSC<sub>in</sub> Input Impedance Vs Frequency  
T<sub>A</sub> = +25°C



10136676

LMX233xU CSP OSC<sub>in</sub> Input Impedance Vs Frequency  
T<sub>A</sub> = +25°C



10136677

# Typical Performance Characteristics

## Input Impedance (Continued)

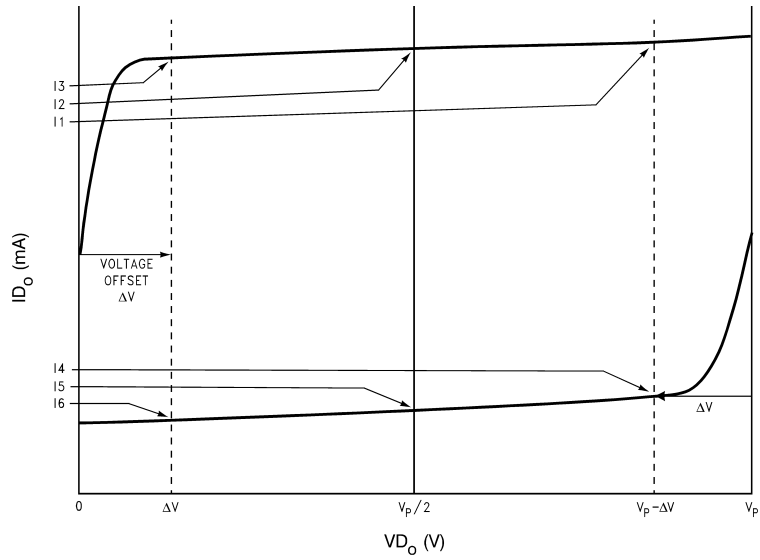
LMX233xU TSSOP and LMX233xU CSP OSC<sub>in</sub> Input Impedance Table

F <sub>osc</sub> (MHz)	LMX233xU TSSOP ZOSC <sub>in</sub>												LMX233xU CSP ZOSC <sub>in</sub>											
	V <sub>cc</sub> = 3.0V (T <sub>A</sub> = 25°C)				V <sub>cc</sub> = 5.5V (T <sub>A</sub> = 25°C)				V <sub>cc</sub> = 3.0V (T <sub>A</sub> = 25°C)				V <sub>cc</sub> = 5.5V (T <sub>A</sub> = 25°C)				V <sub>cc</sub> = 5.5V (T <sub>A</sub> = 25°C)							
	OSC <sub>in</sub> BUFFER POWERED UP		OSC <sub>in</sub> BUFFER POWERED DOWN		OSC <sub>in</sub> BUFFER POWERED UP		OSC <sub>in</sub> BUFFER POWERED DOWN		OSC <sub>in</sub> BUFFER POWERED UP		OSC <sub>in</sub> BUFFER POWERED DOWN		OSC <sub>in</sub> BUFFER POWERED UP		OSC <sub>in</sub> BUFFER POWERED DOWN		OSC <sub>in</sub> BUFFER POWERED UP		OSC <sub>in</sub> BUFFER POWERED DOWN					
Re ZOSC <sub>in</sub> (Ω)	Im ZOSC <sub>in</sub> (Ω)	Re ZOSC <sub>in</sub> (Ω)	Im ZOSC <sub>in</sub> (Ω)	Re ZOSC <sub>in</sub> (Ω)	Im ZOSC <sub>in</sub> (Ω)	Re ZOSC <sub>in</sub> (Ω)	Im ZOSC <sub>in</sub> (Ω)	Re ZOSC <sub>in</sub> (Ω)	Im ZOSC <sub>in</sub> (Ω)	Re ZOSC <sub>in</sub> (Ω)	Im ZOSC <sub>in</sub> (Ω)	Re ZOSC <sub>in</sub> (Ω)	Im ZOSC <sub>in</sub> (Ω)	Re ZOSC <sub>in</sub> (Ω)	Im ZOSC <sub>in</sub> (Ω)	Re ZOSC <sub>in</sub> (Ω)	Im ZOSC <sub>in</sub> (Ω)	Re ZOSC <sub>in</sub> (Ω)	Im ZOSC <sub>in</sub> (Ω)					
5.0	2291.113	-8000.376	6321.972	985.863	-11825.209	11866.234	2832.878	-6774.525	7342.982	1246.071	-11436.600	11504.282	5107.688	-9526.374	10809.27	4154.104	-18073.24	18544.50	4698.960	-6544.007	8056.318	4154.104	-18073.24	18544.50
7.5	1202.389	-5538.197	5667.218	294.460	-7640.322	7645.994	1287.479	-4861.053	5023.579	520.098	-7675.309	7692.910	2249.081	-6544.475	6920.146	1571.331	-10205.48	10325.74	2626.329	-4998.105	5646.119	1812.311	-10602.90	10756.68
10.0	791.970	-4218.658	4292.353	266.942	-5793.060	5799.207	739.926	-3754.673	3826.886	484.656	-5659.675	5680.388	1664.886	-5170.920	5432.335	1066.661	-8350.651	8418.499	1625.723	-4208.219	4512.261	976.808	-8900.590	8654.633
12.5	527.864	-3418.978	3459.456	197.874	-4547.094	4551.397	544.280	-3078.945	3126.584	196.239	-4685.189	4669.295	1048.750	-4245.537	4373.153	727.756	-6341.105	6382.730	1182.342	-3466.982	3663.045	899.697	-6248.932	6313.967
15.0	343.020	-2439.847	2460.085	161.801	-3761.566	3765.044	416.644	-2536.243	2570.238	160.236	-3799.626	3803.003	872.629	-3558.426	3663.861	442.319	-5658.273	5675.536	856.006	-2977.931	3098.519	436.542	-5712.788	5729.443
17.5	316.446	-2439.847	2460.085	141.326	-3203.351	3206.467	309.867	-2192.584	2214.372	196.400	-3305.741	3311.570	691.377	-3158.030	3232.825	296.061	-4799.917	4809.039	697.781	-2605.886	2697.692	309.618	-4985.007	4994.613
20.0	228.626	-2178.146	2191.096	63.505	-2879.931	2880.631	227.640	-1974.267	1987.347	73.816	-2917.281	2918.215	559.597	-2791.912	2847.441	194.872	-4242.475	4248.948	554.417	-2318.961	2384.315	303.378	-4345.597	4356.174
22.5	211.659	-1932.535	1944.091	98.108	-2543.330	2545.222	214.873	-1741.101	1754.310	103.131	-2608.411	2610.449	442.147	-2512.522	2551.129	170.072	-3402.400	3406.648	424.599	-1865.270	1912.986	174.460	-3506.895	3511.232
25.0	163.618	-1762.903	1770.480	89.270	-2340.221	2341.923	169.812	-1589.814	1598.857	67.246	-2388.967	2389.913	444.524	-2261.024	2304.307	191.739	-3114.867	3120.763	379.086	-1714.793	1756.195	159.273	-3213.478	3217.422
27.5	163.733	-1589.620	1598.030	69.675	-2106.253	2107.405	160.401	-1435.713	1444.646	69.923	-2161.702	2162.832	367.245	-2060.013	2092.491	188.280	-2837.317	2843.557	357.340	-1567.979	1608.182	157.424	-2934.223	2938.443
30.0	148.446	-1463.071	1470.583	81.310	-1926.869	1928.604	141.501	-1314.929	1322.520	67.843	-1984.769	1985.928	356.692	-1893.442	1926.747	188.280	-2664.486	2667.608	332.065	-1461.571	1498.818	157.389	-2780.469	2784.920
32.5	130.683	-1340.206	1346.562	46.548	-1750.824	1751.443	121.612	-1213.403	1219.482	37.610	-1812.700	1813.090	348.916	-1776.540	1810.480	129.014	-2471.170	2473.011	299.913	-1358.120	1390.840	125.630	-2600.472	2603.500
35.0	126.059	-1255.034	1261.349	38.046	-1662.230	1662.666	116.385	-1131.429	1137.399	45.646	-1689.748	1690.365	302.932	-1648.356	1675.961	95.424	-2331.694	2334.664	284.654	-1274.370	1305.774	144.727	-2419.904	2424.228
37.5	115.848	-1178.954	1184.632	37.202	-1547.816	1548.263	109.381	-1064.461	1070.066	36.346	-1591.439	1591.854	300.020	-1549.601	1578.377	117.732	-2182.473	2183.987	273.323	-1199.918	1230.654	152.283	-2302.913	2307.942
40.0	108.280	-1089.931	1095.296	36.351	-1439.460	1439.919	100.267	-985.544	990.631	39.180	-1470.482	1471.004	281.334	-1454.298	1481.260	81.318	-2182.473	2183.987	273.323	-1199.918	1230.654	152.283	-2302.913	2307.942

10136678

LMX2330U/LMX2331U/LMX2332U

## Charge Pump Current Specification Definitions



10136637

I1 = Charge Pump Sink Current at  $VD_o = V_p - \Delta V$

I2 = Charge Pump Sink Current at  $VD_o = V_p/2$

I3 = Charge Pump Sink Current at  $VD_o = \Delta V$

I4 = Charge Pump Source Current at  $VD_o = V_p - \Delta V$

I5 = Charge Pump Source Current at  $VD_o = V_p/2$

I6 = Charge Pump Source Current at  $VD_o = \Delta V$

$\Delta V$  = Voltage offset from the positive and negative rails. Dependent on the VCO tuning range relative to  $V_{CC}$  and GND. Typical values are between 0.5V and 1.0V.

$V_p$  refers to either  $V_p$  RF or  $V_p$  IF

$VD_o$  refers to either  $VD_o$  RF or  $VD_o$  IF

$ID_o$  refers to either  $ID_o$  RF or  $ID_o$  IF

### Charge Pump Output Current Magnitude Variation Vs Charge Pump Output Voltage

$$ID_o \text{ Vs } VD_o = \frac{(|I1| - |I3|)}{(|I1| + |I3|)} \times 100\%$$

$$= \frac{(|I4| - |I6|)}{(|I4| + |I6|)} \times 100\%$$

10136663

### Charge Pump Output Sink Current Vs Charge Pump Output Source Current Mismatch

$$ID_o \text{ SINK Vs } ID_o \text{ SOURCE} = \frac{|I2| - |I5|}{\frac{1}{2}(|I2| + |I5|)} \times 100\%$$

10136664

### Charge Pump Output Current Magnitude Variation Vs Temperature

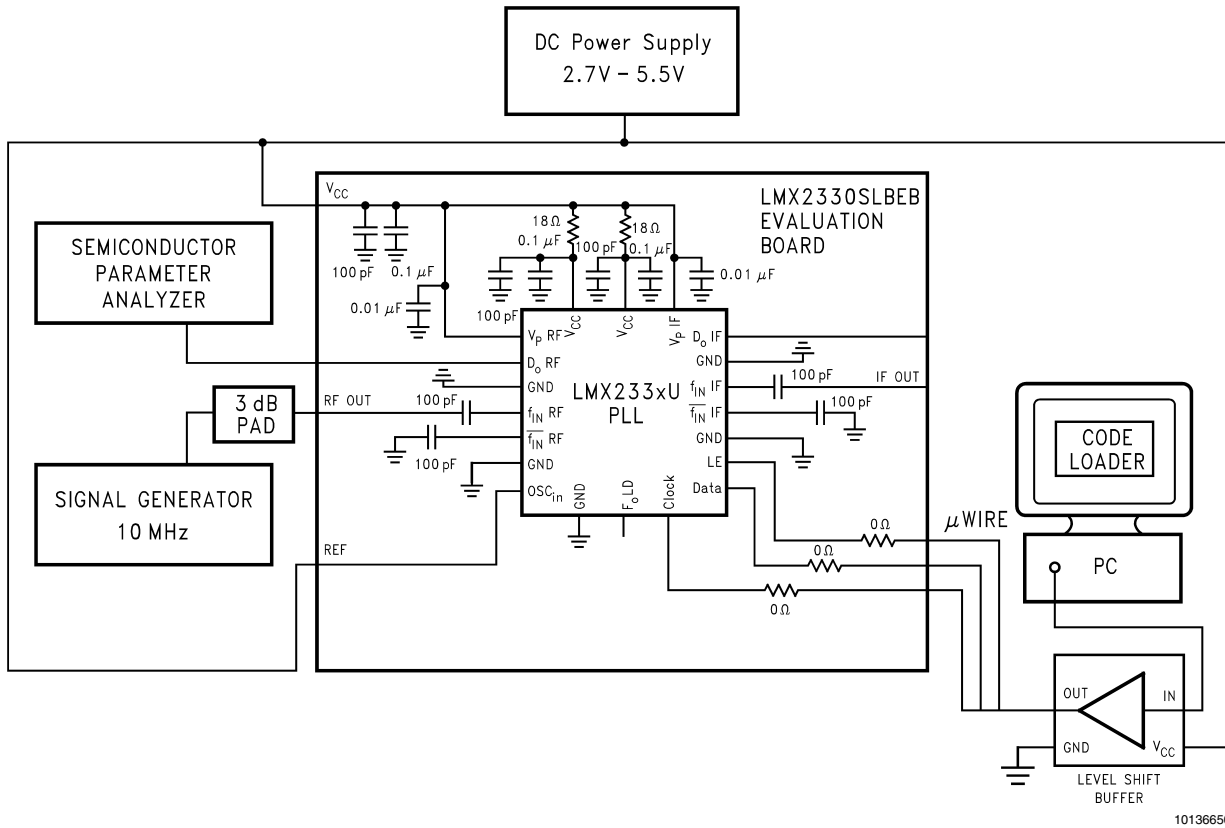
$$ID_o \text{ Vs } T_A = \frac{|I2|_{T_A=25^\circ C} - |I2|_{T_A}}{|I2|_{T_A=25^\circ C}} \times 100\%$$

$$= \frac{|I5|_{T_A=25^\circ C} - |I5|_{T_A}}{|I5|_{T_A=25^\circ C}} \times 100\%$$

10136665

## Test Setups

LMX233xU Charge Pump Test Setup



10136650

The block diagram above illustrates the setup required to measure the LMX233xU device's RF charge pump sink current. The same setup is used for a LMX2330TMEB Evaluation Board. The IF charge pump measurement setup is similar to the RF charge pump measurement setup. The purpose of this test is to assess the functionality of the RF charge pump.

This setup uses an open loop configuration. A power supply is connected to  $V_{CC}$  and swept from 2.7V to 5.5V. By means of a signal generator, a 10 MHz signal is typically applied to the  $f_{IN}$  RF pin. The signal is one of two inputs to the phase detector. The 3 dB pad provides a 50  $\Omega$  match between the PLL and the signal generator. The  $OSC_{in}$  pin is tied to  $V_{CC}$ . This establishes the other input to the phase detector. Alternatively, this input can be tied directly to the ground plane. With the  $D_O$  RF pin connected to a Semiconducter Parameter Analyzer in this way, the sink, source, and TRI-STATE currents can be measured by simply toggling the **Phase Detector Polarity** and **Charge Pump State** states in Code Loader. Similarly, the LOW and HIGH currents can be measured by switching the **Charge Pump Gain's** state between **1X** and **4X** in Code Loader.

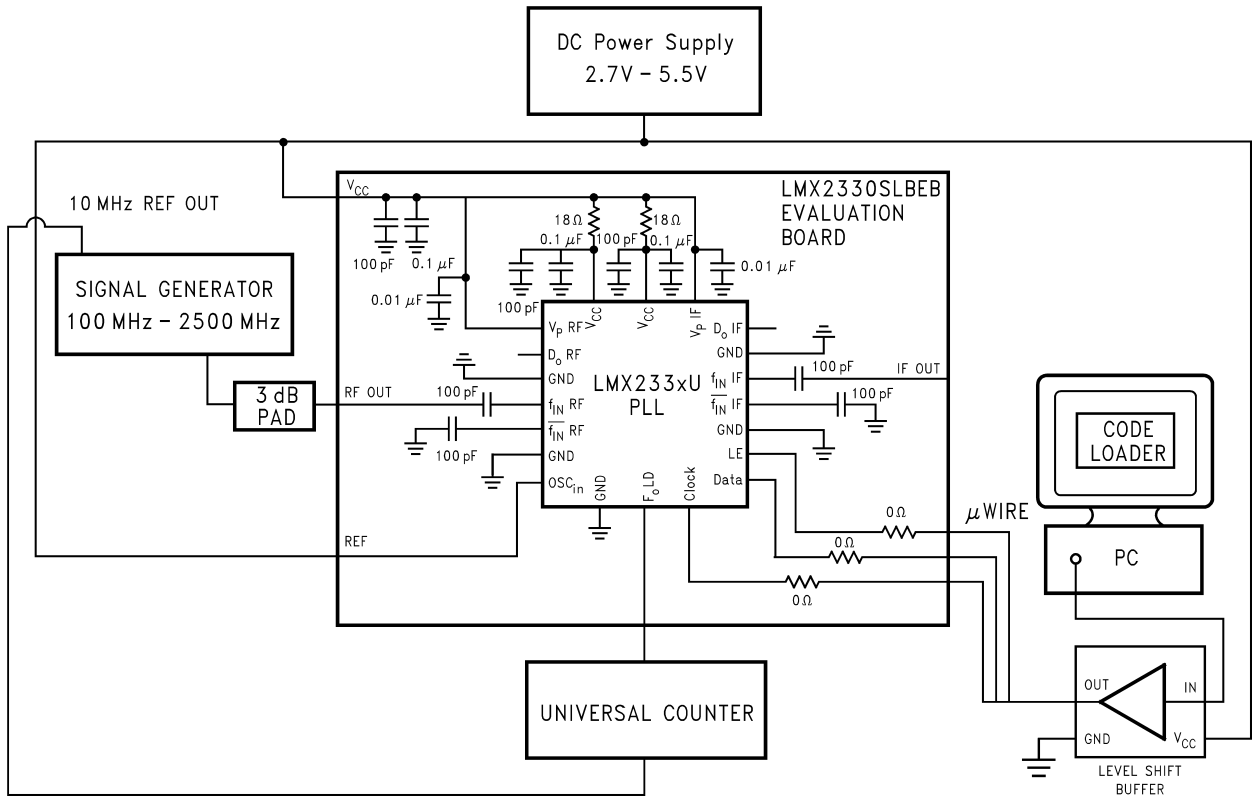
Let  $F_r$  represent the frequency of the signal applied to the  $OSC_{in}$  pin, which is simply zero in this case (DC), and let  $F_p$  represent the frequency of the signal applied to the  $f_{IN}$  RF pin. The phase detector is sensitive to the rising edges of  $F_r$  and  $F_p$ . Assuming positive VCO characteristics; the charge pump turns ON and sinks current when the first rising edge of  $F_p$  is detected. Since  $F_r$  has no rising edge, the charge pump continues to sink current indefinitely.

Toggling the **Phase Detector Polarity** state to negative VCO characteristics allows the measurement of the RF charge pump source current. Likewise, selecting **TRI-STATE** (TRI-STATE  $ID_O$  RF Bit = 1) for **Charge Pump State** in Code Loader facilitates the measurement of the TRI-STATE current.

The measurements are repeated at different temperatures, namely  $T_A = -40^\circ\text{C}$ ,  $+25^\circ\text{C}$ , and  $+85^\circ\text{C}$ .

## Test Setups (Continued)

LMX233xU  $f_{IN}$  Sensitivity Test Setup



10136640

The block diagram above illustrates the setup required to measure the LMX233xU device's RF input sensitivity level. The same setup is used for a LMX2330TMEB Evaluation Board. The IF input sensitivity test setup is similar to the RF sensitivity test setup. The purpose of this test is to measure the acceptable signal level to the  $f_{IN}$  RF input of the PLL chip. Outside the acceptable signal range, the feedback divider begins to divide incorrectly and miscount the frequency.

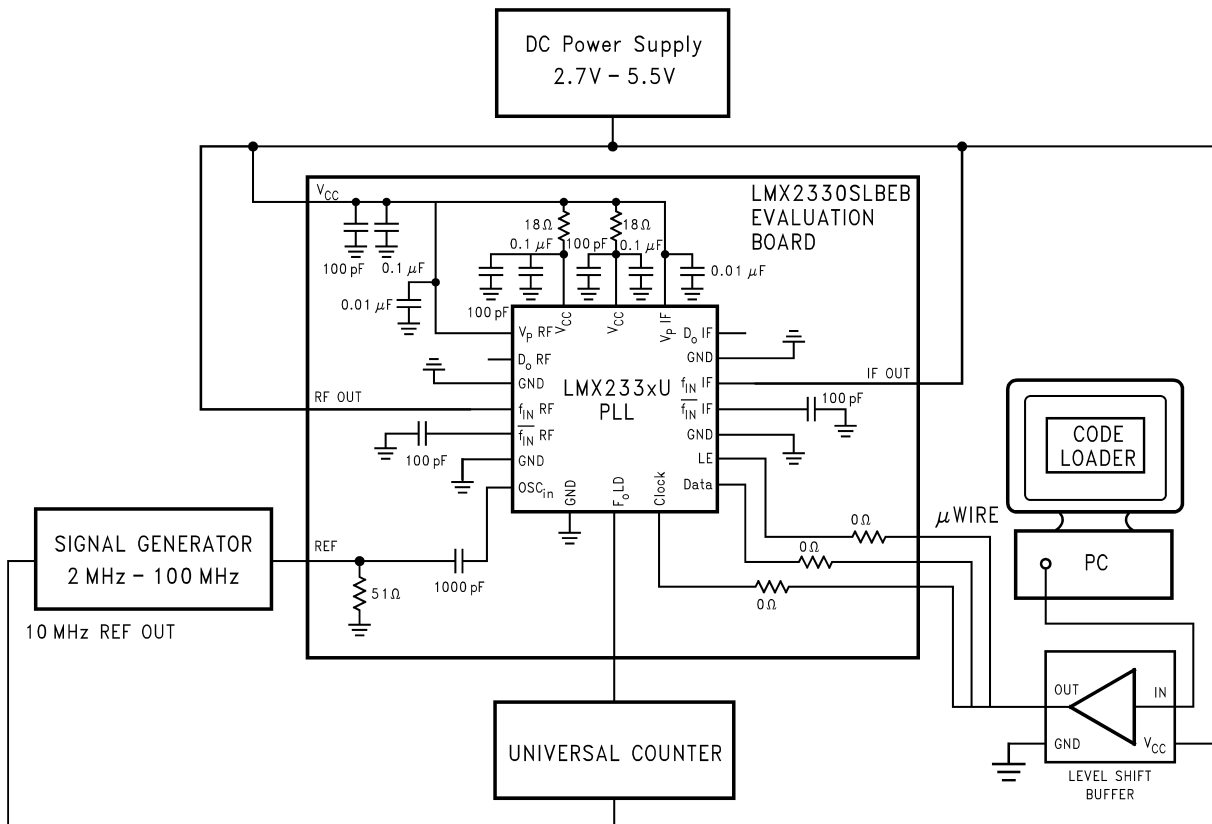
The setup uses an open loop configuration. A power supply is connected to  $V_{CC}$  and swept from 2.7V to 5.5V. The IF PLL is powered down (PWDN IF Bit = 1). By means of a signal generator, an RF signal is applied to the  $f_{IN}$  RF pin. The 3 dB pad provides a 50  $\Omega$  match between the PLL and the signal generator. The  $OSC_{in}$  pin is tied to  $V_{CC}$ . The N value is typically set to 10000 in Code Loader, i.e. RF N\_CNTRB Word = 156 and RF N\_CNTRA Word = 16 for PRE RF Bit = 1 (LMX2330U) or PRE RF = 0 (LMX2331U and LMX2332U). The feedback divider output is routed to the  $F_{0LD}$  pin by selecting the **RF PLL N Divider Output** word ( $F_{0LD}$  Word =

6 or 14) in Code Loader. A Universal Counter is connected to the  $F_{0LD}$  pin and tied to the 10 MHz reference output of the signal generator. The output of the feedback divider is thus monitored and should be equal to  $f_{IN}$  RF / N.

The  $f_{IN}$  RF input frequency and power level are then swept with the signal generator. The measurements are repeated at different temperatures, namely  $T_A = -40^\circ\text{C}$ ,  $+25^\circ\text{C}$ , and  $+85^\circ\text{C}$ . Sensitivity is reached when the frequency error of the divided RF input is greater than or equal to 1 Hz. The power attenuation from the cable and the 3 dB pad must be accounted for. The feedback divider will actually miscount if too much or too little power is applied to the  $f_{IN}$  RF input. Therefore, the allowed input power level will be bounded by the upper and lower sensitivity limits. In a typical application, if the power level to the  $f_{IN}$  RF input approaches the sensitivity limits, this can introduce spurs and degradation in phase noise. When the power level gets even closer to these limits, or exceeds it, then the RF PLL loses lock.

## Test Setups (Continued)

LMX233xU OSC<sub>in</sub> Sensitivity Test Setup



10136641

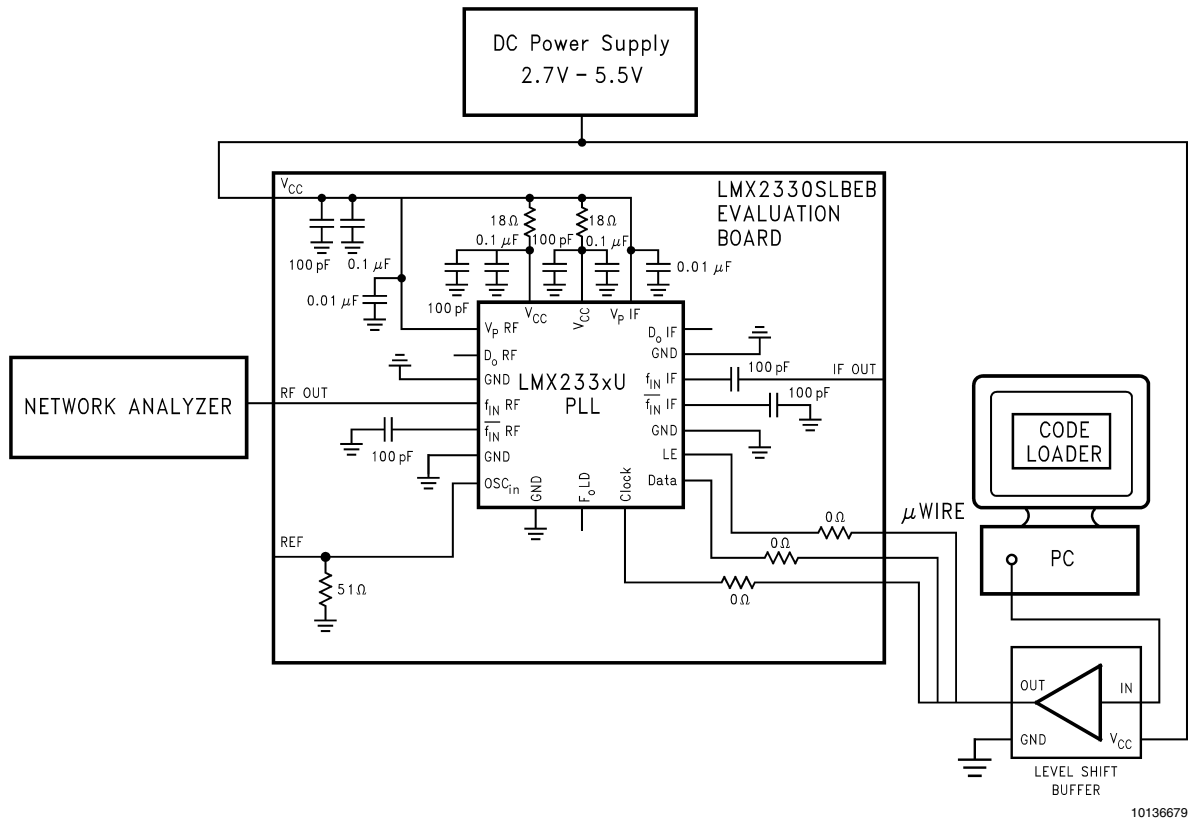
The block diagram above illustrates the setup required to measure the LMX233xU device's OSC<sub>in</sub> buffer sensitivity level. The same setup is used for a LMX2330TMEB Evaluation Board. This setup is similar to the f<sub>IN</sub> sensitivity setup except that the signal generator is now connected to the OSC<sub>in</sub> pin and both f<sub>IN</sub> pins are tied to V<sub>CC</sub>. The 51 Ω shunt resistor matches the OSC<sub>in</sub> input to the signal generator. The R counter is typically set to 1000, i.e. RF R\_CNTR Word = 1000 or IF R\_CNTR Word = 1000. The reference divider output is routed to the F<sub>oLD</sub> pin by selecting the **RF PLL R Divider Output** word (F<sub>oLD</sub> Word = 2 or 10) or the **IF PLL R Divider Output** word (F<sub>oLD</sub> Word = 1 or 9) in Code Loader.

Similarly, a Universal Counter is connected to the F<sub>oLD</sub> pin and is tied to the 10 MHz reference output from the signal generator. The output of the reference divider is monitored and should be equal to OSC<sub>in</sub>/ RF R\_CNTR or OSC<sub>in</sub>/ IF R\_CNTR.

Again, V<sub>CC</sub> is swept from 2.7V to 5.5V. The OSC<sub>in</sub> input frequency and voltage level are then swept with the signal generator. The measurements are repeated at different temperatures, namely T<sub>A</sub> = -40°C, +25°C, and +85°C. Sensitivity is reached when the frequency error of the divided input signal is greater than or equal to 1 Hz.

Test Setups (Continued)

LMX233xU  $f_{IN}$  Impedance Test Setup



The block diagram above illustrates the setup required to measure the LMX233xU device's RF input impedance. The IF input impedance and reference oscillator impedance setups are very much similar. The same setup is used for a LMX2330TMEB Evaluation Board. Measuring the device's input impedance facilitates the design of appropriate matching networks to match the PLL to the VCO, or in more critical situations, to the characteristic impedance of the printed circuit board (PCB) trace, to prevent undesired transmission line effects.

Before the actual measurements are taken, the Network Analyzer needs to be calibrated, i.e. the error coefficients need to be calculated. Therefore, three standards will be used to calculate these coefficients: an **open**, **short** and a **matched load**. A 1-port calibration is implemented here.

To calculate the coefficients, the PLL chip is first removed from the PCB. The Network Analyzer port is then connected to the RF OUT connector of the evaluation board and the desired operating frequency is set. The typical frequency range selected for the LMX233xU device's RF synthesizer is from 100 MHz to 2500 MHz. The standards will be located down the length of the RF OUT transmission line. The transmission line adds electrical length and acts as an offset from the reference plane of the Network Analyzer; therefore, it

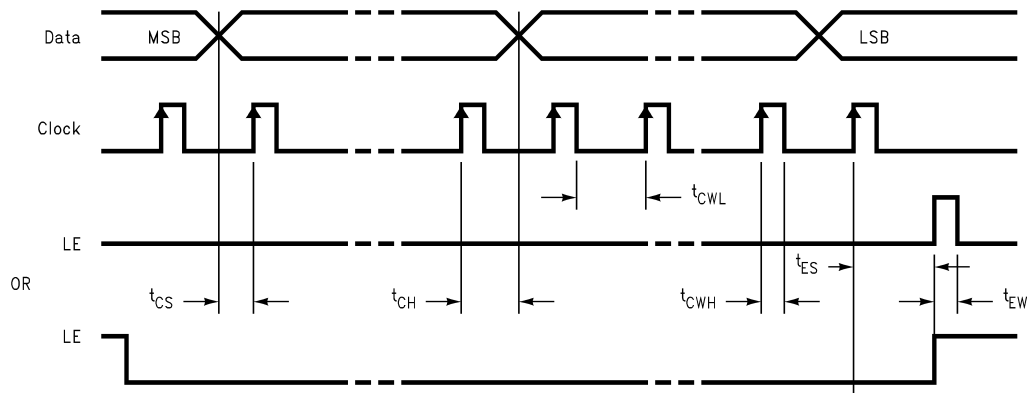
must be included in the calibration. Although not shown, 0 Ω resistors are used to complete the RF OUT transmission line (trace).

To implement an **open** standard, the end of the RF OUT trace is simply left open. To implement a **short** standard, a 0 Ω resistor is placed at the end of the RF OUT transmission line. Last of all, to implement a **matched load** standard, two 100 Ω resistors in parallel are placed at the end of the RF OUT transmission line. The Network Analyzer calculates the calibration coefficients based on the measured  $S_{11}$  parameters. With this all done, calibration is now complete.

The PLL chip is then placed on the PCB. A power supply is connected to  $V_{CC}$  and swept from 2.7V to 5.5V. The  $OSC_{in}$  pin is tied to the ground plane. Alternatively, the  $OSC_{in}$  pin can be tied to  $V_{CC}$ . In this setup, the complementary input ( $\bar{f}_{IN}$  RF) is AC coupled to ground. With the Network Analyzer still connected to RF OUT, the measured  $f_{IN}$  RF impedance is displayed.

**Note:** The impedance of the reference oscillator is measured when the oscillator buffer is powered up (PVDN RF Bit = 0 or PVDN IF Bit = 0), and when the oscillator buffer is powered down (PVDN RF Bit = 1 and PVDN IF Bit = 1).

## LMX233xU Serial Data Input Timing



10136610

**Notes:**

1. Data is clocked into the 22-bit shift register on the rising edge of Clock
2. The MSB of Data is shifted in first.

## 1.0 Functional Description

The basic phase-lock-loop (PLL) configuration consists of a high-stability crystal reference oscillator, a frequency synthesizer such as the National Semiconductor LMX233xU, a voltage controlled oscillator (VCO), and a passive loop filter. The frequency synthesizer includes a phase detector, current mode charge pump, programmable reference R and feedback N frequency dividers. The VCO frequency is established by dividing the crystal reference signal down via the reference divider to obtain a comparison reference frequency. This reference signal,  $F_r$ , is then presented to the input of a phase/frequency detector and compared with the feedback signal,  $F_p$ , which was obtained by dividing the VCO frequency down by way of the feedback divider. The phase/frequency detector measures the phase error between the  $F_r$  and  $F_p$  signals and outputs control signals that are directly proportional to the phase error. The charge pump then pumps charge into or out of the loop filter based on the magnitude and direction of the phase error. The loop filter converts the charge into a stable control voltage for the VCO. The phase/frequency detector's function is to adjust the voltage presented to the VCO until the feedback signal's frequency and phase match that of the reference signal. When this "Phase-Locked" condition exists, the VCO frequency will be N times that of the comparison frequency, where N is the feedback divider ratio.

### 1.1 REFERENCE OSCILLATOR INPUT

The reference oscillator frequency for both the RF and IF PLLs is provided from an external reference via the  $OSC_{in}$  pin. The reference buffer circuit supports input frequencies from 5 to 40 MHz with a minimum input sensitivity of  $0.5 V_{PP}$ . The reference buffer circuit has an approximate  $V_{CC}/2$  input threshold and can be driven from an external CMOS or TTL logic gate. Typically, the  $OSC_{in}$  pin is connected to the output of a crystal oscillator.

### 1.2 REFERENCE DIVIDERS (R COUNTERS)

The reference dividers divide the reference input signal,  $OSC_{in}$ , by a factor of R. The output of the reference divider circuits feeds the reference input of the phase detector. This reference input to the phase detector is often referred to as the comparison frequency. The divide ratio should be chosen such that the maximum phase comparison frequency ( $F_{\phi RF}$  or  $F_{\phi IF}$ ) of 10 MHz is not exceeded.

The RF and IF reference dividers are each comprised of 15-bit CMOS binary counters that support a continuous integer divide ratio from 3 to 32767. The RF and IF reference divider circuits are clocked by the output of the reference buffer circuit which is common to both.

### 1.3 PRESCALERS

The  $f_{IN}$  RF ( $f_{IN}$  IF) and  $\overline{f_{IN}}$  RF ( $\overline{f_{IN}}$  IF) input pins drive the input of a bipolar, differential-pair amplifier. The output of the bipolar, differential-pair amplifier drives a chain of ECL D-type flip-flops in a dual modulus configuration. The output of the prescaler is used to clock the subsequent feedback dividers. The RF and IF PLL complementary inputs can be driven differentially, or the negative input can be AC coupled to ground through an external capacitor for single ended configuration. A 32/33 or a 64/65 prescale ratio can be selected for the 2.5 GHz LMX2330U RF synthesizer. A 64/65 or a 128/129 prescale ratio can be selected for both the LMX2331U and LMX2332U RF synthesizers. The IF circuitry contains an 8/9 or a 16/17 prescaler.

### 1.4 PROGRAMMABLE FEEDBACK DIVIDERS (N COUNTERS)

The programmable feedback dividers operate in concert with the prescalers to divide the input signal,  $f_{IN}$ , by a factor of N. The output of the programmable reference divider is provided to the feedback input of the phase detector circuit. The divide ratio should be chosen such that the maximum phase comparison frequency ( $F_{\phi RF}$  or  $F_{\phi IF}$ ) of 10 MHz is not exceeded.

The programmable feedback divider circuit is comprised of an A counter (swallow counter) and a B counter (programmable binary counter). The RF  $N\_CNTRA$  counter is a 7-bit CMOS swallow counter, programmable from 0 to 127. The IF  $N\_CNTRA$  counter is also a 7-bit CMOS swallow counter, but programmable from 0 to 15. The three most significant bits are 'don't cares' in this case. The RF  $N\_CNTRB$  and IF  $N\_CNTRB$  counters are both 11-bit CMOS binary counters, programmable from 3 to 2047. A continuous integer divide ratio is achieved if  $N \geq P * (P-1)$ , where P is the value of the prescaler selected. Divide ratios less than the minimum continuous divide ratio are achievable as long as the binary programmable counter value is greater than the swallow counter value ( $N\_CNTRB \geq N\_CNTRA$ ). Refer to **Sections 2.6.1, 2.6.2, 2.7.1 and 2.7.2** for details on how to program the  $N\_CNTRA$  and  $N\_CNTRB$  counters. The following equations are useful in determining and programming a particular value of N:

$$N = (P \times N\_CNTRB) + N\_CNTRA$$

$$f_{IN} = N \times F_{\phi}$$

#### Definitions:

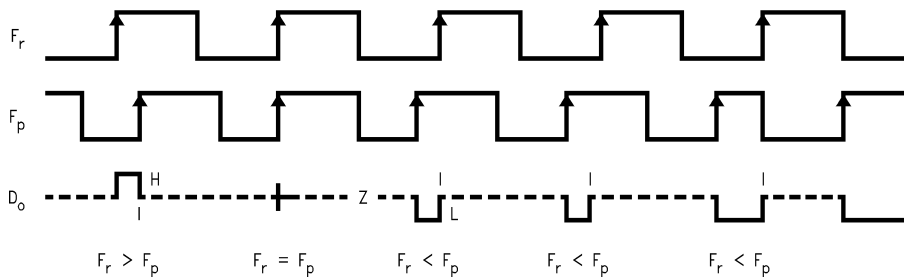
$F_{\phi}$ :	RF or IF phase detector comparison frequency
$f_{IN}$ :	RF or IF input frequency
$N\_CNTRA$ :	RF or IF A counter value
$N\_CNTRB$ :	RF or IF B counter value
P:	Preset modulus of the dual modulus prescaler
	LMX2330U RF synthesizer: P = 32 or 64
	LMX2331U RF synthesizer: P = 64 or 128
	LMX2332U RF synthesizer: P = 64 or 128
	LMX233xU IF synthesizer: P = 8 or 16

### 1.5 PHASE/FREQUENCY DETECTORS

The RF and IF phase/frequency detectors are driven from their respective N and R counter outputs. The maximum frequency for both the RF and IF phase detector inputs is 10 MHz. The phase/frequency detector outputs control the respective charge pumps. The polarity of the pump-up or pump-down control signals are programmed using the **PD\_POL RF** or **PD\_POL IF** control bits, depending on whether the RF or IF VCO characteristics are positive or negative. Refer to **Sections 2.4.2 and 2.5.2** for more details. The phase/frequency detectors have a detection range of  $-2\pi$  to  $+2\pi$ . The phase/frequency detectors also receive a feedback signal from the charge pump in order to eliminate dead zone.

## 1.0 Functional Description (Continued)

### PHASE COMPARATOR AND INTERNAL CHARGE PUMP CHARACTERISTICS



10136611

#### Notes:

1. The minimum width of the pump-up and pump-down current pulses occur at the  $D_o$  RF or  $D_o$  IF pins when the loop is phase locked.
2. The diagram assumes positive VCO characteristics, i.e. PD\_POL RF or PD\_POL IF = 1.
3.  $F_r$  is the phase detector input from the reference divider (R counter).
4.  $F_p$  is the phase detector input from the programmable feedback divider (N counter).
5.  $D_o$  refers to either the RF or IF charge pump output.

### 1.6 CHARGE PUMPS

The charge pump directs charge into or out of an external loop filter. The loop filter converts the charge into a stable control voltage which is applied to the tuning input of the VCO. The charge pump steers the VCO control voltage towards  $V_P$  RF or  $V_P$  IF during pump-up events and towards GND during pump-down events. When locked,  $D_o$  RF or  $D_o$  IF are primarily in a TRI-STATE mode with small corrections occurring at the phase comparator rate. The charge pump output current magnitude can be selected by toggling the  $ID_o$  RF or  $ID_o$  IF control bits.

### 1.7 MICROWIRE SERIAL INTERFACE

The programmable register set is accessed via the MICROWIRE serial interface. The interface is comprised of three signal pins: Clock, Data and LE (Latch Enable). Serial data is clocked into the 22-bit shift register on the rising edge of Clock. The last two bits decode the internal control register address. When LE transitions HIGH, data stored in the shift register is loaded into one of four control registers depending on the state of the address bits. The MSB of Data is loaded in first. The synthesizers can be programmed even in power down mode. A complete programming description is provided in **Section 2.0 Programming Description**.

### 1.8 MULTI-FUNCTION OUTPUTS

The LMX233xU device's  $F_oLD$  output pin is a multi-function output that can be configured as the RF FastLock output, a push-pull analog lock detect output, counter reset, or used to monitor the output of the various reference divider (R counter) or feedback divider (N counter) circuits. The  $F_oLD$  control word is used to select the desired output function. When the PLL is in powerdown mode, the  $F_oLD$  output is pulled to a LOW state. A complete programming description of the multi-function output is provided in **Section 2.8  $F_oLD$** .

#### 1.8.1 Push-Pull Analog Lock Detect Output

An analog lock detect status generated from the phase detector is available on the  $F_oLD$  output pin if selected. The lock detect output goes HIGH when the charge pump is inactive. It goes LOW when the charge pump is active during a comparison cycle. When viewed with an oscilloscope, narrow negative pulses are observed when the charge pump turns on. The lock detect output signal is a push-pull configuration.

Three separate lock detect signals are routed to the multiplexer. Two of these monitor the 'lock' status of the individual synthesizers. The third detects the condition when both the RF and IF synthesizers are in a 'locked state'. External circuitry however, is required to provide a steady DC signal to indicate when the PLL is in a locked state. Refer to **Section 2.8  $F_oLD$**  for details on how to program the different lock detect options.

# 1.0 Functional Description (Continued)

## 1.8.2 Open Drain FastLock Output

The LMX233xU Fastlock feature allows faster loop response time during lock acquisition. The loop response time (lock time) can be approximately halved if the loop bandwidth is doubled. In order to achieve this, the same gain/ phase relationship at twice the loop bandwidth must be maintained. This can be achieved by increasing the charge pump current from 0.95 mA (ID<sub>o</sub> RF Bit = 0) in the steady state mode, to 3.8 mA (ID<sub>o</sub> RF Bit = 1) in Fastlock. When the F<sub>o</sub>LD output is configured as a FastLock output, an open drain device is enabled. The open drain device switches in a parallel resistor R2' to ground, of equal value to resistor R2 of the external loop filter. The loop bandwidth is effectively doubled and stability is maintained. Once locked to the correct frequency, the PLL will return to a steady state condition. Refer to **Section 2.8 F<sub>o</sub>LD** for details on how to configure the F<sub>o</sub>LD output to an open drain Fastlock output.

## 1.8.3 Counter Reset

Three separate counter reset functions are provided. When the F<sub>o</sub>LD is programmed to **Reset IF Counters**, both the IF feedback divider and the IF reference divider are held at their load point. When the **Reset RF Counters** is programmed, both the RF feedback divider and the RF reference divider are held at their load point. When the **Reset All Counters** mode is enabled, all feedback dividers and reference dividers are held at their load point. When the device is programmed to normal operation, both the feedback divider and reference divider are enabled and resume counting in 'close' alignment to each other. Refer to **Section 2.8 F<sub>o</sub>LD** for more details.

## 1.8.4 Reference Divider and Feedback Divider Output

The outputs of the various N and R dividers can be monitored by selecting the appropriate F<sub>o</sub>LD word. This is essential when performing OSC<sub>in</sub> or f<sub>IN</sub> sensitivity measurements. Refer to the **Test Setups** section for more details. Refer to **Section 2.8 F<sub>o</sub>LD** for more details on how to route the appropriate divider output to the F<sub>o</sub>LD pin.

## 1.9 POWER CONTROL

Each synthesizer in the LMX233xU device is individually power controlled by device powerdown bits. The powerdown word is comprised of the **PWDN RF (PWDN IF)** bit, in conjunction with the **TRI-STATE ID<sub>o</sub> RF (TRI-STATE ID<sub>o</sub> IF)** bit. The powerdown control word is used to set the operating mode of the device. Refer to **Sections 2.4.4, 2.5.4, 2.6.4, and 2.7.4** for details on how to program the RF or IF powerdown bits.

When either the RF synthesizer or the IF synthesizer enters the powerdown mode, the respective prescaler, phase detector, and charge pump circuit are disabled. The D<sub>o</sub> RF (D<sub>o</sub> IF), f<sub>IN</sub> RF (f<sub>IN</sub> IF), and f<sub>IN</sub> RF (f<sub>IN</sub> IF) pins are all forced to a high impedance state. The reference divider and feedback divider circuits are held at the load point during powerdown. The oscillator buffer is disabled when both the RF and IF synthesizers are powered down. The OSC<sub>in</sub> pin is forced to a HIGH state through an approximate 100 kΩ resistance when this condition exists. When either synthesizer is activated, the respective prescaler, phase detector, charge pump circuit, and the oscillator buffer are all powered up. The feedback divider, and the reference divider are held at load point. This allows the reference oscillator, feedback divider, reference divider and prescaler circuitry to reach proper bias levels. After a finite delay, the feedback and reference dividers are enabled and they resume counting in 'close' alignment (the maximum error is one prescaler cycle). The MICROWIRE control register remains active and capable of loading and latching data while in the powerdown mode.

### Synchronous Powerdown Mode

In this mode, the powerdown function is gated by the charge pump. When the device is configured for synchronous powerdown, the device will enter the powerdown mode upon completion of the next charge pump pulse event.

### Asynchronous Powerdown Mode

In this mode, the powerdown function is NOT gated by the completion of a charge pump pulse event. When the device is configured for asynchronous powerdown, the part will go into powerdown mode immediately.

TRI-STATE ID <sub>o</sub>	PWDN	Operating Mode
0	0	PLL Active, Normal Operation
1	0	PLL Active, Charge Pump Output in High Impedance State
0	1	Synchronous Powerdown
1	1	Asynchronous Powerdown

#### Notes:

1. TRI-STATE ID<sub>o</sub> refers to either the TRI-STATE ID<sub>o</sub> RF or TRI-STATE ID<sub>o</sub> IF bit .
2. PWDN refers to either the PWDN RF or PWDN IF bit.

## 2.0 Programming Description

### 2.1 MICROWIRE INTERFACE

The 22-bit shift register is loaded via the MICROWIRE interface. The shift register consists of a 20-bit *Data[19:0] Field* and a 2-bit *Address[1:0] Field* as shown below. The Address Field is used to decode the internal control register address. When LE transitions HIGH, data stored in the shift register is loaded into one of 4 control registers depending on the state of the address bits. The MSB of Data is loaded in first. The Data Field assignments are shown in **Section 2.3 CONTROL REGISTER CONTENT MAP**.

MSB		LSB	
Data[19:0]		Address[1:0]	
21	2	1	0

### 2.2 CONTROL REGISTER LOCATION

The address bits Address[1:0] decode the internal register address. The table below shows how the address bits are mapped into the target control register.

Address[1:0] Field		Target Register
0	0	IF R
0	1	RF R
1	0	IF N
1	1	RF N

### 2.3 CONTROL REGISTER CONTENT MAP

The control register content map describes how the bits within each control register are allocated to specific control functions.

## 2.0 Programming Description (Continued)

Reg.	Most Significant Bit										SHIFT REGISTER BIT LOCATION										Least Significant Bit					
	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0				
	<i>Data Field</i>																									
<b>IF R</b>	F <sub>o</sub> LD0	F <sub>o</sub> LD2	TRI-STATE ID <sub>o</sub> IF	ID <sub>o</sub> IF	PD <sub>-</sub> POL IF	IF R_CNTR[14:0]																0		0		
<b>RF R</b>	F <sub>o</sub> LD1	F <sub>o</sub> LD3	TRI-STATE ID <sub>o</sub> RF	ID <sub>o</sub> RF	PD <sub>-</sub> POL RF	RF R_CNTR[14:0]																0		1		
<b>IF N</b>	PWDN IF	PRE IF					IF N_CNTRB[10:0]										IF N_CNTRA[6:0]						1		0	
<b>RF N</b>	PWDN RF	PRE RF					RF N_CNTRB[10:0]										RF N_CNTRA[6:0]						1		1	

## 2.0 Programming Description (Continued)

### 2.4 IF R REGISTER

The IF R register contains the IF R\_CNTR, PD\_POL IF, ID<sub>o</sub> IF, and TRI-STATE ID<sub>o</sub> IF control words, in addition to two bits that compose the F<sub>o</sub>LD control word. The detailed descriptions and programming information for each control word is discussed in the following sections. IF R\_CNTR[14:0]

Reg.	SHIFT REGISTER BIT LOCATION																	Least Significant Bit			
	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
	<i>Data Field</i>																			<i>Address Field</i>	
IF R	F <sub>o</sub> LD0	F <sub>o</sub> LD2	TRI-STATE ID <sub>o</sub> IF	ID <sub>o</sub> IF	PD_POL IF	IF R_CNTR[14:0]														0	0

#### 2.4.1 IF R\_CNTR[14:0] IF SYNTHESIZER PROGRAMMABLE REFERENCE DIVIDER (R COUNTER) IF R[2:16]

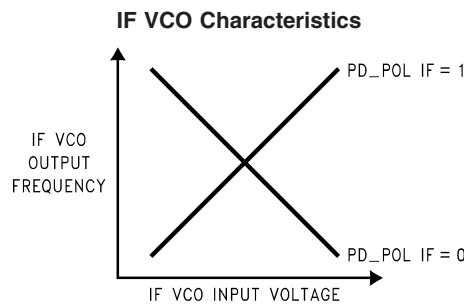
The IF reference divider (IF R\_CNTR) can be programmed to support divide ratios from 3 to 32767. Divide ratios less than 3 are prohibited.

Divide Ratio	IF R_CNTR[14:0]															
	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
3	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	
4	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	
32767	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	

#### 2.4.2 PD\_POL IF IF SYNTHESIZER PHASE DETECTOR POLARITY IF R[17]

The PD\_POL IF bit is used to control the IF synthesizer's phase detector polarity based on the VCO tuning characteristics.

Control Bit	Register Location	Description	Function	
			0	1
PD_POL IF	IF R[17]	IF Phase Detector Polarity	IF VCO Negative Tuning Characteristics	IF VCO Positive Tuning Characteristics



#### 2.4.3 ID<sub>o</sub> IF IF SYNTHESIZER CHARGE PUMP CURRENT GAIN IF R[18]

The ID<sub>o</sub> IF bit controls the IF synthesizer's charge pump gain. Two current levels are available.

Control Bit	Register Location	Description	Function	
			0	1
ID <sub>o</sub> IF	IF R[18]	IF Charge Pump Current Gain	LOW 0.95 mA	HIGH 3.80 mA

## 2.0 Programming Description (Continued)

### 2.4.4 TRI-STATE ID<sub>0</sub> IF IF SYNTHESIZER CHARGE PUMP TRI-STATE CURRENT IF R[19]

The TRI-STATE ID<sub>0</sub> IF bit allows the charge pump to be switched between a normal operating mode and a high impedance output state. This happens asynchronously with the change in the TRI-STATE ID<sub>0</sub> IF bit.

Furthermore, the TRI-STATE ID<sub>0</sub> IF bit operates in conjunction with the PWDN IF bit to set a synchronous or an asynchronous powerdown mode.

Control Bit	Register Location	Description	Function	
			0	1
TRI-STATE ID <sub>0</sub> IF	IF R[19]	IF Charge Pump TRI-STATE Current	IF Charge Pump Normal Operation	IF Charge Pump Output in High Impedance State

### 2.5 RF R REGISTER

The RF R register contains the RF R\_CNTR, PD\_POL RF, ID<sub>0</sub> RF, and TRI-STATE ID<sub>0</sub> RF control words, in addition to two bits that compose the F<sub>0</sub>LD control word. The detailed descriptions and programming information for each control word is discussed in the following sections.

Reg.	SHIFT REGISTER BIT LOCATION																				Least Significant Bit		
	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
	<i>Data Field</i>																				<i>Address Field</i>		
RF R	F <sub>0</sub> LD1	F <sub>0</sub> LD3	TRI-STATE ID <sub>0</sub> RF	ID <sub>0</sub> RF	PD_POL RF	RF R_CNTR[14:0]																0	1

### 2.5.1 RF R\_CNTR[14:0] RF SYNTHESIZER PROGRAMMABLE REFERENCE DIVIDER (R COUNTER) RF R[2:16]

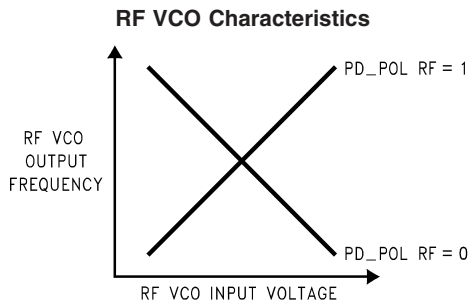
The RF reference divider (RF R\_CNTR) can be programmed to support divide ratios from 3 to 32767. Divide ratios less than 3 are prohibited.

Divide Ratio	RF R_CNTR[14:0]															
	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
3	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	
4	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	
32767	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	

### 2.5.2 PD\_POL RF RF SYNTHESIZER PHASE DETECTOR POLARITY RF R[17]

The PD\_POL RF bit is used to control the RF synthesizer's phase detector polarity based on the VCO tuning characteristics.

Control Bit	Register Location	Description	Function	
			0	1
PD_POL RF	RF R[17]	RF Phase Detector Polarity	RF VCO Negative Tuning Characteristics	RF VCO Positive Tuning Characteristics



10136682

## 2.0 Programming Description (Continued)

### 2.5.3 ID<sub>o</sub> RF RF SYNTHESIZER CHARGE PUMP CURRENT GAIN RF R[18]

The ID<sub>o</sub> RF bit controls the RF synthesizer's charge pump gain. Two current levels are available.

Control Bit	Register Location	Description	Function	
			0	1
ID <sub>o</sub> RF	RF R[18]	RF Charge Pump Current Gain	LOW 0.95 mA	HIGH 3.80 mA

### 2.5.4 TRI-STATE ID<sub>o</sub> RF RF SYNTHESIZER CHARGE PUMP TRI-STATE CURRENT RF R[19]

The TRI-STATE ID<sub>o</sub> RF bit allows the charge pump to be switched between a normal operating mode and a high impedance output state. This happens asynchronously with the change in the TRI-STATE ID<sub>o</sub> RF bit.

Furthermore, the TRI-STATE ID<sub>o</sub> RF bit operates in conjunction with the PWDN RF bit to set a synchronous or an asynchronous powerdown mode.

Control Bit	Register Location	Description	Function	
			0	1
TRI-STATE ID <sub>o</sub> RF	RF R[19]	RF Charge Pump TRI-STATE Current	RF Charge Pump Normal Operation	RF Charge Pump Output in High Impedance State

### 2.6 IF N REGISTER

The IF N register contains the IF N\_CNTRA, IF N\_CNTRB, PRE IF, and PWDN IF control words. The IF N\_CNTRA and IF N\_CNTRB control words are used to setup the programmable feedback divider. The detailed description and programming information for each control word is discussed in the following sections.

Reg.	SHIFT REGISTER BIT LOCATION																	Least Significant Bit			
	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
	<i>Data Field</i>																			<i>Address Field</i>	
IF N	PWDN IF	PRE IF	IF N_CNTRB[10:0]										IF N_CNTRA[6:0]						1	0	

### 2.6.1 IF N\_CNTRA[6:0] IF SYNTHESIZER SWALLOW COUNTER (A COUNTER) IF N[2:8]

The IF N\_CNTRA control word is used to setup the IF synthesizer's A counter. The A counter is a 7-bit swallow counter used in the programmable feedback divider. The IF N\_CNTRA control word can be programmed to values ranging from 0 to 15. The three most significant bits are 'don't care bits' in this case.

Divide Ratio	IF N_CNTRA[6:0]						
	6	5	4	3	2	1	0
0	X	X	X	0	0	0	0
1	X	X	X	0	0	0	1
•	•	•	•	•	•	•	•
15	X	X	X	1	1	1	1

### 2.6.2 IF N\_CNTRB[10:0] IF SYNTHESIZER PROGRAMMABLE BINARY COUNTER (B COUNTER) IF N[9:19]

The IF N\_CNTRB control word is used to setup the IF synthesizer's B counter. The B counter is an 11-bit programmable binary counter used in the programmable feedback divider. The IF N\_CNTRB control word can be programmed to values ranging from 3 to 2047.

Divide Ratio	IF N_CNTRB[10:0]										
	10	9	8	7	6	5	4	3	2	1	0
3	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	1	0	0
•	•	•	•	•	•	•	•	•	•	•	•
2047	1	1	1	1	1	1	1	1	1	1	1

## 2.0 Programming Description (Continued)

### 2.6.3 PRE IF IF SYNTHESIZER PRESCALER SELECT IF N[20]

The IF synthesizer utilizes a selectable dual modulus prescaler.

Control Bit	Register Location	Description	Function	
			0	1
PRE IF	IF N[20]	IF Prescaler Select	8/9 Prescaler Selected	16/17 Prescaler Selected

### 2.6.4 PWDN IF IF SYNTHESIZER POWERDOWN IF N[21]

The PWDN IF bit is used to switch the IF PLL between a powered up and powered down mode.

Furthermore, the PWDN IF bit operates in conjunction with the TRI-STATE ID<sub>0</sub> IF bit to set a synchronous or an asynchronous powerdown mode.

Control Bit	Register Location	Description	Function	
			0	1
PWDN IF	IF N[21]	IF Powerdown	IF PLL Active	IF PLL Powerdown

### 2.7 RF N REGISTER

The RF N register contains the RF N\_CNTRA, RF N\_CNTRB, PRE RF, and PWDN RF control words. The RF N\_CNTRA and RF N\_CNTRB control words are used to setup the programmable feedback divider. The detailed description and programming information for each control word is discussed in the following sections.

Reg.	SHIFT REGISTER BIT LOCATION																					
	Most Significant Bit										Least Significant Bit											
	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	<i>Data Field</i>																				<i>Address Field</i>	
RF N	PWDN RF	PRE RF	RF N_CNTRB[10:0]										RF N_CNTRA[6:0]						1	1		

#### 2.7.1 RF N\_CNTRA[6:0] RF SYNTHESIZER SWALLOW COUNTER (A COUNTER) RF N[2:8]

The RF N\_CNTRA control word is used to setup the RF synthesizer's A counter. The A counter is a 7-bit swallow counter used in the programmable feedback divider. The RF N\_CNTRA control word can be programmed to values ranging from 0 to 127.

Divide Ratio	RF N_CNTRA[6:0]						
	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
•	•	•	•	•	•	•	•
127	1	1	1	1	1	1	1

#### 2.7.2 RF N\_CNTRB[10:0] RF SYNTHESIZER PROGRAMMABLE BINARY COUNTER (B COUNTER) RF N[9:19]

The RF N\_CNTRB control word is used to setup the RF synthesizer's B counter. The B counter is an 11-bit programmable binary counter used in the programmable feedback divider. The RF N\_CNTRB control word can be programmed to values ranging from 3 to 2047.

Divide Ratio	RF N_CNTRB[10:0]										
	10	9	8	7	6	5	4	3	2	1	0
3	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	1	0	0
•	•	•	•	•	•	•	•	•	•	•	•
2047	1	1	1	1	1	1	1	1	1	1	1

## 2.0 Programming Description (Continued)

### 2.7.3 PRE RF RF SYNTHESIZER PRESCALER SELECT

RF N[20]

The RF synthesizer utilizes a selectable dual modulus prescaler.

#### LMX2330U RF Synthesizer Prescaler Select

Control Bit	Register Location	Description	Function	
			0	1
PRE RF	RF N[20]	RF Prescaler Select	32/33 Prescaler Selected	64/65 Prescaler Selected

#### LMX2331U and LMX2332U RF Synthesizer Prescaler Select

Control Bit	Register Location	Description	Function	
			0	1
PRE RF	RF N[20]	RF Prescaler Select	64/65 Prescaler Selected	128/129 Prescaler Selected

### 2.7.4 PWDN RF RF SYNTHESIZER POWERDOWN

RF N[21]

The PWDN RF bit is used to switch the RF PLL between a powered up and powered down mode.

Furthermore, the PWDN RF bit operates in conjunction with the TRI-STATE ID<sub>o</sub> RF bit to set a synchronous or an asynchronous powerdown mode.

Control Bit	Register Location	Description	Function	
			0	1
PWDN RF	RF N[21]	RF Powerdown	RF PLL Active	RF PLL Powerdown

## 2.0 Programming Description (Continued)

### 2.8 F<sub>o</sub>LD[3:0]

#### MULTI-FUNCTION OUTPUT SELECT

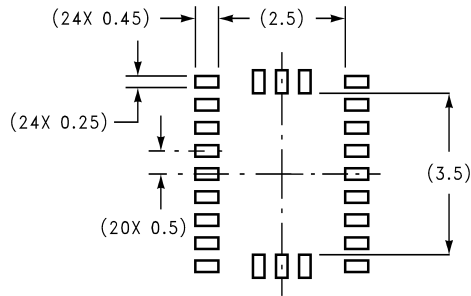
[RF R[20], IF R[20], RF R [21], IF R[21]]

The F<sub>o</sub>LD control word is used to select which signal is routed to the F<sub>o</sub>LD pin.

F <sub>o</sub> LD3	F <sub>o</sub> LD2	F <sub>o</sub> LD1	F <sub>o</sub> LD0	F <sub>o</sub> LD Output State
0	0	0	0	LOW Logic State Output
0	0	0	1	IF PLL R Divider Output, Push-Pull Output
0	0	1	0	RF PLL R Divider Output, Push-Pull Output
0	0	1	1	Open Drain Fastlock Output
0	1	0	0	IF PLL Analog Lock Detect, Push-Pull Output
0	1	0	1	IF PLL N Divider Output, Push-Pull Output
0	1	1	0	RF PLL N Divider Output, Push-Pull Output
0	1	1	1	Reset IF Counters, LOW Logic State Output
1	0	0	0	RF Analog Lock Detect, Push-Pull Output
1	0	0	1	IF PLL R Divider Output, Push-Pull Output
1	0	1	0	RF PLL R Divider Output, Push-Pull Output
1	0	1	1	Reset RF Counters, LOW Logic State Output
1	1	0	0	RF and IF Analog Lock Detect, Push-Pull Output
1	1	0	1	IF PLL N Divider Output, Push-Pull Output
1	1	1	0	RF PLL N Divider Output, Push-Pull Output
1	1	1	1	Reset All Counters, LOW Logic State Output

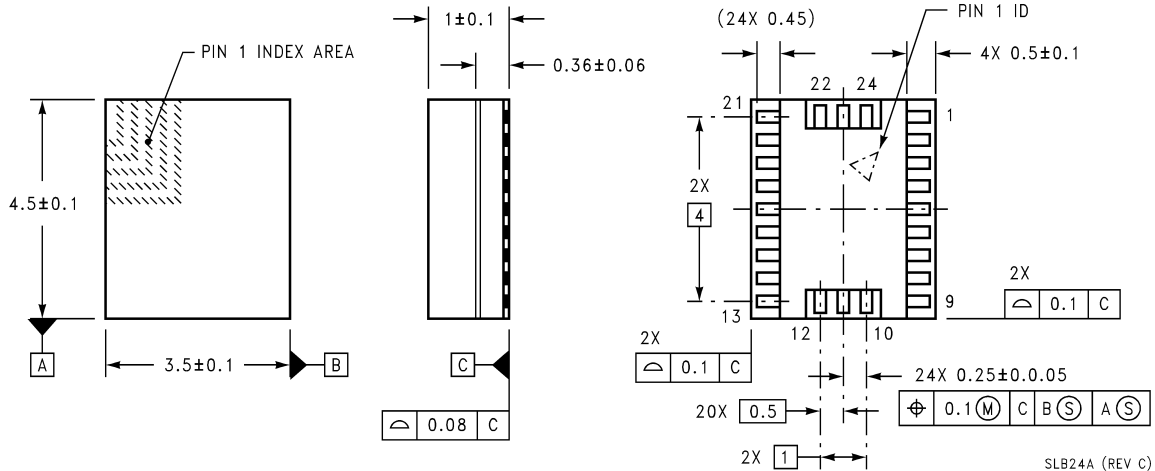


**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



DIMENSIONS ARE IN MILLIMETERS

**RECOMMENDED LAND PATTERN**  
1:1 RATIO WITH PACKAGE SOLDER PADS




SLB24A (REV C)

**24-Pin Chip Scale Package (SLB)**  
**NS Package Number SLB24A**

**LIFE SUPPORT POLICY**

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT AND GENERAL COUNSEL OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

 **National Semiconductor Corporation**  
Americas  
Email: support@nsc.com

www.national.com

**National Semiconductor Europe**  
Fax: +49 (0) 180-530 85 86  
Email: europe.support@nsc.com  
Deutsch Tel: +49 (0) 69 9508 6208  
English Tel: +44 (0) 870 24 0 2171  
Français Tel: +33 (0) 1 41 91 8790

**National Semiconductor Asia Pacific Customer Response Group**  
Tel: 65-2544466  
Fax: 65-2504466  
Email: ap.support@nsc.com

**National Semiconductor Japan Ltd.**  
Tel: 81-3-5639-7560  
Fax: 81-3-5639-7507