MM5321 TV camera sync generator

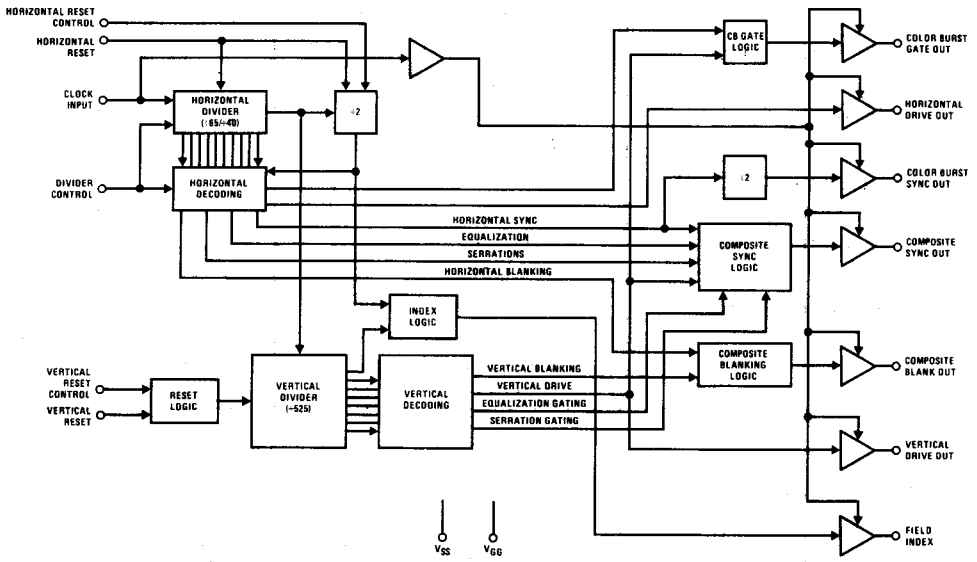
general description

The MM5321 TV camera sync generator is a MOS, P-channel enhancement mode, LSI chip designed to supply the basic sync functions for either color or monochrome 525 line/60 Hz interlaced camera and video recorder applications. Required power supplies are +5V and −12V, or any other combination resulting in V_{SS} − 17V. All inputs and outputs are TTL compatible without the use of external components.

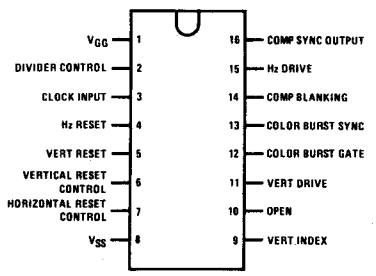
features

- Multi-function gen lock input provides flexible control of multiple camera installations
- 16-lead dual-in-line package
- Conventional +5V, −12V power supplies
- Uses 2.04545 MHz or 1.260 MHz input reference
- Field indexing provided for VTR applications
- Color burst gate and sync allow stable color operation

logic and connection diagrams



Dual-In-Line Package



TOP VIEW

Order Number MM5321N
See Package 19

absolute maximum ratings

Voltage at Any Pin	V_{SS} + 0.3 to V_{SS} − 22
Operating Temperature	0°C to +70°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics

T_A within operating temperature range V_{SS} = 5V ±5%, V_{GG} = −12V ±5%, unless otherwise stated.

	PARAMETER	CONDITIONS	MIN	MAX	UNITS
	Input Levels				
V_{IH}	Logical High Level		V_{SS}−1.5	V_{SS}+0.3	V
V_{IL}	Logical Low Level		V_{SS}−18	V_{SS}−4.2	V
	Input Leakage	V_{IN} = −10V, T_A = 25°C, All Other Pins GND		0.5	μA
	Input Capacitance	V_{IN} = 0V, f = 1 MHz, All Other Pins GND, (Note 1)		6	pF
	Clock Input Leakage	V_{IN} = −10V, T_A = 25°C, All Other Pins GND		0.5	μA
	Clock Input Capacitance	V_{IN} = 0V, f = 1 MHz, All Other Pins GND, (Note 1)		6	pF
	Output Levels				
V_{OH}	Logical High Level	I_{SOURCE} = −0.5 mA	2.4	V_{SS}	V
V_{OL}	Logical Low Level	I_{SINK} = 1.6 mA		0.4	V
		MOS Load	V_{SS}−12.5	V_{SS}−9	V
I_{GG}	Power Supply Current	T_A = 25°C, V_{GG} = −12V, ϕ_{PW} = 235 ns, V_{SS} = 5V, Input Clock Frequency = 2.04545 MHz		36	mA

ac electrical characteristics

T_A within operating temperature range V_{SS} = 5V ±5%, V_{GG} = −12V ±5%, unless otherwise stated.

	PARAMETER	CONDITIONS	MIN	MAX	UNITS
ϕ_{PW}	Input Clock Pulse Width	Input Clock Frequency = 2.04545 MHz, ϕt_r, ϕt_f = 20 ns	190	280	ns
		Input Clock Frequency = 1.26 MHz, ϕt_r = ϕt_f = 20 ns	300	570	ns
	Horizontal Reset Pulse Width	Within 400 ns after the Falling Edge of Master Clock, *(Figure 5)* Rise and Fall Time = 20 ns	500	800	ns
t_{pd}	Output Propagation Delay				
V_{OH}	Logical High Level	Capacitance at the Output = 15 pF		750	ns
V_{OL}	Logical Low Level	*(Figure 5)*		750	ns

Note 1: Capacitance is guaranteed by periodic testing.

functional description

EXTERNAL CONTROL LEVELS

Horizontal Reset occurs for Logic "0." This resets the horizontal counter to a state shown in *Figures 2 and 3.*

Vertical Reset occurs for Logic "0." This resets the vertical counter to a state determined by reset control input as shown below:

VERTICAL RESET CONTROL INPUT	PERMITS THE VERTICAL COUNTER TO RESET TO THE:
V_{IH}, (V_{SS})	0th count
V_{IL}, (V_{GG})	11th count

HORIZONTAL RESET CONTROL INPUT	RESETS THE HORIZONTAL DIVIDER TO:
V_{IH}	Beginning of line
V_{IL}	Center of line

Logic "0" = V_{IL}

Logic "1' = V_{IH}

Divide select input = V_{IL}, (V_{GG}) for master clock frequency of 1.26 MHz.

Divide select input = V_{IH}, (V_{SS}) for master clock frequency of 2.04545 MHz.

INPUTS

The user may select either of two input clock frequencies by properly programming the Divider Control pin. In one case the input frequency is 2.04545 MHz, which is 14.31818 MHz divided by seven. The other is eighty times the horizontal frequency, or 1.26 MHz. The divider control will be programmed by connecting it to V_{IH} (V_{SS}) and V_{IL}, (V_{GG}) respectively.

There are separate Vertical and Horizontal Reset inputs which allow directly resetting the appropriate divider(s) by a control pulse generated by external means. Both horizontal and vertical dividers may be reset simultaneously by connecting the Vertical and Horizontal Reset pins together and driving them with the same reset signal. Actual resetting of the vertical divider is to either of two states, depending upon the state of the Vertical Reset Control input; to zero, or to the fifth vertical serration pulse (eleven 0.5H time intervals from leading edge of Vertical Blanking). Refer to the reset table. The horizontal divider will always be reset to a position which is 8 input clock pulses from the leading edge of the serration gate in the horizontal timing scheme *(Figures 2 and 3)*. The generator is reset to the odd field (field one). The Field Index output pulse occurs once each odd field at the leading edge of Vertical Blanking. It can be used to reset, or "gen-lock," similar sync generator chips by connecting it to their Vertical and Horizontal Reset inputs. The Horizontal Reset Control selects Horizontal Reset to the start or center of a line. For "gen-lock" both Horizontal and Vertical Reset pulses should not exceed 800ns.

OUTPUTS

The generator supplies the following standard output functions: Horizontal Drive Out, Vertical Drive Out, Composite Blanking Out, Composite Sync Out and the Color Burst Gate.

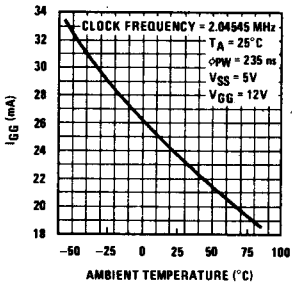
In addition, Field Index and Color Burst Sync outputs are provided. The Field Index identifies the odd field, or field one, by occurring for two clock periods at the leading edge of Vertical Blanking in that field. Thus, its rate is 30 Hz. As described above, it can also be used to "gen-lock" other sync generator chips.

The Color Burst Sync output signal occurs at half the horizontal rate with the same timing as the Color Burst Gate output. It may be used to sync the color burst as it will have the same delay characteristics as the other outputs (including, of course, the Color Burst Gate) – the color burst sync is present during the vertical interval.

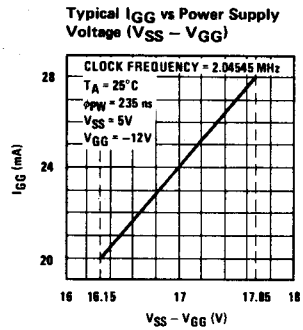
Differences in phasing between outputs are minimized by the use of identical push-pull output buffers clocked by the internal clock.

typical performance characteristics

Typical I_{GG} vs Temperature



Typical I_{GG} vs Power Supply Voltage ($V_{SS} - V_{GG}$)



switching time waveforms

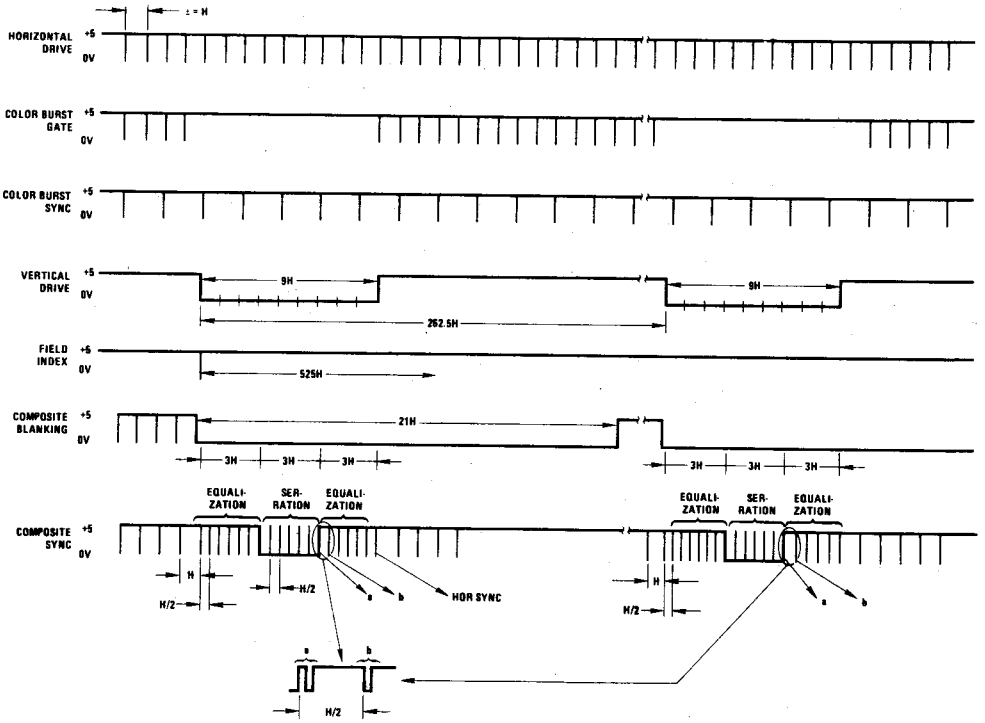


FIGURE 1.

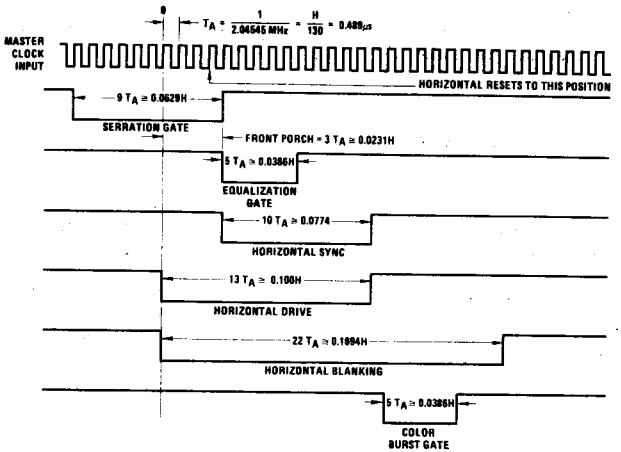


FIGURE 2. Horizontal Timing Master Clock = 2.04545 MHz

switching time waveforms (Continued)

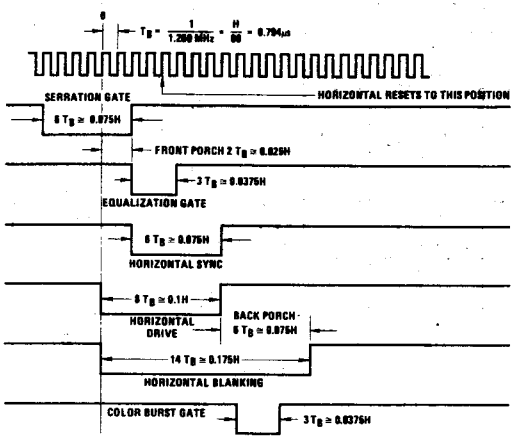


FIGURE 3. Horizontal Timing Master Clock = 1.26 MHz

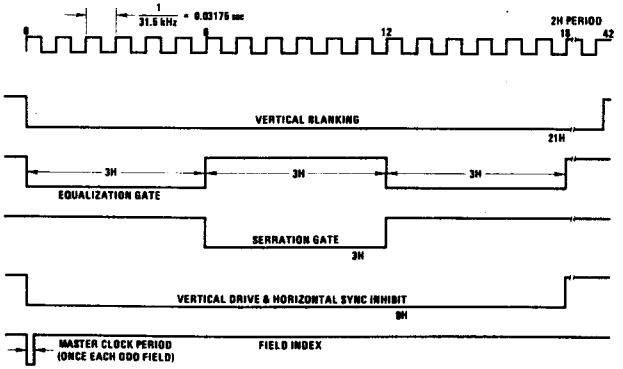


FIGURE 4. Vertical Timing

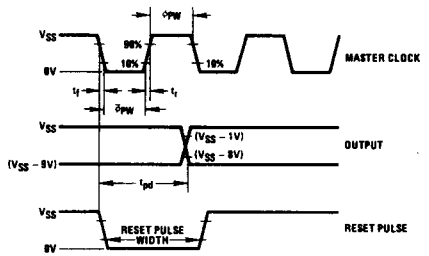


FIGURE 5.

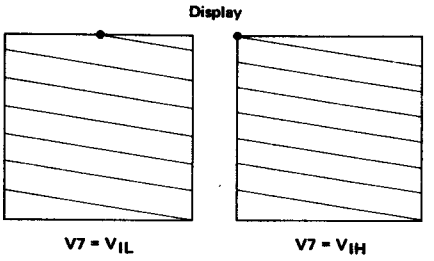
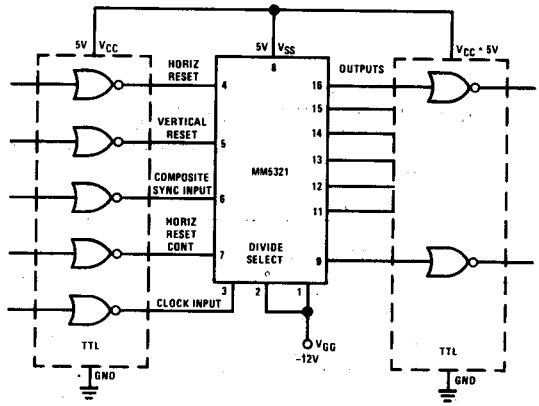


FIGURE 6. Horizontal Reset Characteristics

typical application



TTL Interface