National Semiconductor

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TP3040, TP3040A PCM Monolithic Filter

General Description

The TP3040/TP3040A filter is a monolithic circuit containing both transmit and receive filters specifically designed for PCM CODEC filtering applications in 8 kHz sampled systems.

The filter is manufactured using microCMOS technology and switched capacitor integrators are used to simulate classical LC ladder filters which exhibit low component sensitivity.

TRANSMIT FILTER STAGE

The transmit filter is a fifth order elliptic low pass filter in series with a fourth order Chebyshev high pass filter. It provides a flat response in the passband and rejection of signals below 200 Hz and above 3.4 kHz.

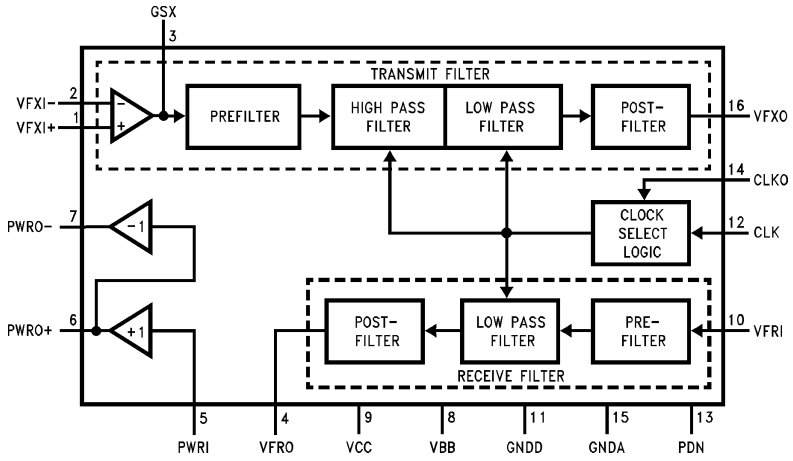
RECEIVE FILTER STAGE

The receive filter is a fifth order elliptic low pass filter designed to reconstruct the voice signal from the decoded/demultiplexed signal which, as a result of the sampling process, is a stair-step signal having the inherent sin x/x frequency response. The receive filter approximates the function required to compensate for the degraded frequency response and restore the flat passband response.

Features

- Designed for D3/D4 and CCITT applications
- +5V, −5V power supplies
- Low power consumption:
  - 45 mW (0 dBm0 into 600Ω)
  - 30 mW (power amps disabled)
- Power down mode: 0.5 mW
- 20 dB gain adjust range
- No external anti-aliasing components
- Sin x/x correction in receive filter
- 50/60 Hz rejection in transmit filter
- TTL and CMOS compatible logic
- All inputs protected against static discharge due to handling

Block Diagram



TL/H/6660–1

FIGURE 1

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Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltages	±7V
Power Dissipation	1 W/Package
Input Voltage	±7V
Voltage at Any Input or Output	V_{CC} + 0.3V to V_{BBV} − 0.3V
Output Short-Circuit Duration	Continuous
Operating Temperature Range	−25°C to +125°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C
ESD Rating to be determined	

DC Electrical Characteristics

Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for V_{CC} = +5.0V ±5%, V_{BB} = −5.0V ±5%; T_A = 0°C to 70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. Typicals specified at V_{CC} = +5.0V, V_{BB} = −5.0V, T_A = 25°C. Clock frequency is 2.048 MHz. Digital interface voltages measured with respect to digital ground, GNDD. Analog voltages measured with respect to analog ground, GNDA.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
POWER DISSIPATION						
I_{CC0}	V_{CC} Standby Current	V_{CC} = 5.25V, V_{BB} = −5.25V, CLK0 and PWRI = −5.25V (Note 6) All other pins at GND (0V) TP3040, TP3040A		50	**100**	µA
I_{BB0}	V_{BB} Standby Current	V_{CC} = 5.25V, V_{BB} = −5.25V, CLK0 and PWRI = −5.25V (Note 6) All other pins at GND (0V) TP3040, TP3040A		50	**100**	µA
I_{CC1}	V_{CC} Operating Current	PWRI = V_{BB}, Power Amp Inactive		3.0	**4.0**	mA
I_{BB1}	V_{BB} Operating Current	PWRI = V_{BB}, Power Amp Inactive		3.0	**4.0**	mA
I_{CC2}	V_{CC} Operating Current	(Note 1)		4.6	**6.4**	mA
I_{BB2}	V_{BB} Operating Current	(Note 1)		4.6	**6.4**	mA
DIGITAL INTERFACE						
I_{INC}	Input Current, CLK	$V_{BB} \le V_{IN} \le V_{CC}$	**−10**		**10**	µA
I_{INP}	Input Current, PDN	$V_{BB} \le V_{IN} \le V_{CC}$	**−100**			µA
I_{IN0}	Input Current, CLK0	$V_{BB} \le V_{IN} \le V_{CC}$ − 0.5V	**−10**		**−0.1**	µA
V_{IL}	Input Low Voltage, CLK, PDN		0		**0.8**	V
V_{IH}	Input High Voltage, CLK, PDN		**2.2**		V_{CC}	V
V_{IL0}	Input Low Voltage, CLK0		V_{BB}		V_{BB}+0.5	V
V_{II0}	Input Intermediate Voltage, CLK0		−0.8		0.8	V
V_{IH0}	Input High Voltage, CLK0		V_{CC}−0.5		V_{CC}	V
TRANSMIT INPUT OP AMP						
$IB_X I$	Input Leakage Current, $VF_X I$	−3.2V ≤ V_{IN} ≤ +3.2V	**−100**		**100**	nA
$RI_X I$	Input Resistance, $VF_X I$	$V_{BB} \le VF_X I \le V_{CC}$	10			MΩ
$VOS_X I$	Input Offset Voltage, $VF_X I$	−2.5V ≤ V_{IN} ≤ +2.5V	**−20**		**20**	mV
V_{CM}	Common-Mode Range, $VF_X I$		**−2.5**		**2.5**	V
CMRR	Common-Mode Rejection Ratio	−2.5V ≤ V_{IN} ≤ 2.5V	**60**			dB
PSRR	Power Supply Rejection of V_{CC} or V_{BB}		**60**			dB
R_{OL}	Open Loop Output Resistance, GS_X			1		kΩ
R_L	Minimum Load Resistance, GS_X		10			kΩ
C_L	Maximum Load Capacitance, GS_X				100	pF
$VO_X I$	Output Voltage Swing, GS_X	$R_L \ge$ 10k	**±2.5**			V
A_{VOL}	Open Loop Voltage Gain, GS_X	$R_L \ge$ 10k	**5,000**			V/V
F_c	Open Loop Unity Gain Bandwidth, GS_X			2		MHz

AC Electrical Characteristics

Unless otherwise specified, $T_A = 25°C$. All parameters are specified for a signal level of 0 dBm0 at 1 kHz. The 0 dBm0 level is assumed to be 1.54 Vrms measured at the output of the transmit or receive filter. Limits printed in **BOLD** characters are guaranteed for $V_{CC} = +5.0V \pm 5\%$, $V_{BB} = -5.0V \pm 5\%$; $T_A = 0°C$ to $70°C$ by correlation with 100% electrical testing at $T_A = 25°C$. All other limits are assured by correlation with other production tests and/or product design and characterization. Typicals specified at $V_{CC} = +5.0V$, $V_{BB} = -5.0V$, $T_A = 25°C$.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
TRANSMIT FILTER (Transmit filter input op amp set to the non-inverting unity gain mode, with $VF_xI = 1.09$ Vrms unless otherwise noted.)						
RL_x	Minimum Load Resistance, VF_xO	$-2.5V < V_{OUT} < 2.5V$ $-3.2V < V_{OUT} < 3.2V$	3 10			kΩ kΩ
CL_x	Load Capacitance, VF_xO				100	pF
RO_x	Output Resistance, VF_xO			1	3	Ω
PSRR1	V_{CC} Power Supply Rejection, VF_xO	f = 1 kHz, $VF_xI+ = 0$ Vrms	**30**			dB
PSRR2	V_{BB} Power Supply Rejection, VF_xO	Same as Above	**35**			dB
GA_x	Absolute Gain	f = 1 kHz (TP3040A) f = 1 kHz (TP3040)	**2.9** **2.875**	3.0 3.0	**3.1** **3.125**	dB dB
GR_x	Gain Relative to GA_x	Below 50 Hz 50 Hz 60 Hz 200 Hz (TP3040A) 200 Hz (TP3040) 300 Hz to 3 kHz (TP3040A) 300 Hz to 3 kHz (TP3040) 3.3 kHz 3.4 kHz 4.0 kHz 4.6 kHz and Above	 **−1.5** **−1.5** **−0.125** **−0.15** **−0.35** **−0.70** 	 −41 −35 −15 	−35 **−35** **−30** **0** **0.05** **0.125** **0.15** **0.03** **−0.1** **−14** **−32**	dB dB dB dB dB dB dB dB dB dB dB
DA_x	Absolute Delay at 1 kHz				250	μs
DD_x	Differential Envelope Delay from 1 kHz to 2.6 kHz				60	μs
DP_x1	Single Frequency Distortion Products				**−48**	dB
DP_x2	Distortion at Maximum Signal Level	0.16 Vrms, 1 kHz Signal Applied to VF_xI+, Gain = 20 dB, $R_L = 10k$			−45	dB
NC_x1	Total C Message Noise at VF_xO	TP3040, TP3040A		2	**5**	dBrnc0
NC_x2	Total C Message Noise at VF_xO	Gain Setting Op Amp at 20 dB, Non-Inverting (Note 3) $T_A = 0°C$ to $70°C$ TP3040, TP3040A		3	**6**	dBrnc0
GA_xT	Temperature Coefficient of 1 kHz Gain			0.0004		dB/°C
GA_xS	Supply Voltage Coefficient of 1 kHz Gain	$V_{CC} = 5.0V \pm 5\%$ $V_{BB} = -5.0V \pm 5\%$		0.01		dB/V
CT_{RX}	Crosstalk, Receive to Transmit $20 \log \frac{VF_xO}{VF_RO}$	Receive Filter Output = 2.2 Vrms $VF_xI+ = 0$ Vrms, f = 0.2 kHz to 3.4 kHz Measure VF_xO			**−70**	dB
GR_xL	Gaintracking Relative to GA_x	Output Level = +3 dBm0 +2 dBm0 to −40 dBm0 −40 dBm0 to −55 dBm0	**−0.1** **−0.05** **−0.1**		**0.1** **0.05** **0.1**	dB dB dB

AC Electrical Characteristics (Continued)

Unless otherwise specified, $T_A = 25°C$. All parameters are specified for a signal level of 0 dBm0 at 1 kHz. The 0 dBm0 level is assumed to be 1.54 Vrms measured at the output of the transmit or receive filter. Limits printed in **BOLD** characters are guaranteed for $V_{CC} = +5.0V \pm 5\%$, $V_{BB} = -5.0V \pm 5\%$; $T_A = 0°C$ to $70°C$ by correlation with 100% electrical testing at $T_A = 25°C$. All other limits are assured by correlation with other production tests and/or product design and characterization. Typicals specified at $V_{CC} = +5.0V$, $V_{BB} = -5.0V$, $T_A = 25°C$.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
RECEIVE FILTER (Unless otherwise noted, the receive filter is preceded by a sin x/x filter with an input signal level of 1.54 Vrms.)						
IB_R	Input Leakage Current, VF_RI	$-3.2V \le V_{IN} \le 3.2V$	**−100**		**100**	nA
RI_R	Input Resistance, VF_RI		10			MΩ
RO_R	Output Resistance, VF_RO			1	3	Ω
CL_R	Load Capacitance, VF_RO				100	pF
RL_R	Load Resistance, VF_RO		10			kΩ
PSRR3	Power Supply Rejection of V_{CC} or V_{BB}, VF_RO	VF_RI Connected to GNDA f = 1 kHz	**35**			dB
VOS_RO	Output DC Offset, VF_RO	VF_RI Connected to GNDA	**−200**		**200**	mV
GA_R	Absolute Gain	f = 1 kHz (TP3040A) f = 1 kHz (TP3040)	**−0.1** **−0.125**	0 0	**0.1** **0.125**	dB dB
GR_R	Gain Relative to Gain at 1 kHz	Below 300 Hz 300 Hz to 3.0 kHz (TP3040A) 300 Hz to 3.0 kHz (TP3040) 3.3 kHz 3.4 kHz 4.0 kHz 4.6 kHz and Above	 **−0.125** **−0.15** **−0.35** **−0.7**		**0.125** **0.125** **0.15** **0.03** **−0.1** **−14** **−32**	dB dB dB dB dB dB dB
DA_R	Absolute Delay at 1 kHz				140	μs
DD_R	Differential Envelope Delay 1 kHz to 2.6 kHz				100	μs
DP_R1	Single Frequency Distortion Products	f = 1 kHz			**−48**	dB
DP_R2	Distortion at Maximum Signal Level	2.2 Vrms Input to Sin x/x Filter, f = 1 kHz, $R_L = 10k$			−45	dB
NC_R	Total C-Message Noise at VF_RO	TP3040, TP3040A		3	**5**	dBrnc0
GA_RT	Temperature Coefficient of 1 kHz Gain			0.0004		dB/°C
GA_RS	Supply Voltage Coefficient of 1 kHz Gain			0.01		dB/V
CT_{XR}	Crosstalk, Transmit to Receive $20 \log \frac{VF_RO}{VF_XO}$	Transmit Filter Output = 2.2 Vrms $VF_RI = 0$ Vrms, f = 0.3 kHz to 3.4 kHz Measure VF_RO			**−70**	dB
GR_RL	Gaintracking Relative to GA_R	Output Level = +3 dBm0 +2 dBm0 to −40 dBm0 −40 dBm0 to −55 dBm0 (Note 5)	**−0.1** **−0.05** **−0.1**		**0.1** **0.05** **0.1**	dB dB dB

AC Electrical Characteristics (Continued)

Unless otherwise specified, $T_A = 25°C$. All parameters are specified for a signal level of 0 dBm0 at 1 kHz. The 0 dBm0 level is assumed to be 1.54 Vrms measured at the output of the transmit or receive filter. Limits printed in **BOLD** characters are guaranteed for $V_{CC} = +5.0V \pm 5\%$, $V_{BB} = -5.0V \pm 5\%$; $T_A = 0°C$ to $70°C$ by correlation with 100% electrical testing at $T_A = 25°C$. All other limits are assured by correlation with other production tests and/or product design and characterization. Typicals specified at $V_{CC} = +5.0V$, $V_{BB} = -5.0V$, $T_A = 25°C$.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
RECEIVE OUTPUT POWER AMPLIFIER						
IBP	Input Leakage Current, PWRI	$-3.2V \le V_{IN} \le 3.2V$	**0.1**		**3**	μA
RIP	Input Resistance, PWRI		10			MΩ
ROP1	Output Resistance, PWRO+, PWRO−	Amplifiers Active		1		Ω
CLP	Load Capacitance, PWRO+, PWRO−				500	pF
GA_p+ GA_p-	Gain, PWRI to PWRO+ Gain, PWRI to PWRO−	$R_L = 600Ω$ Connected Between PWRO+ and PWRO−, Input Level = 0 dBm0 (Note 4)		1 −1		V/V V/V
GR_pL	Gaintracking Relative to 0 dBm0 Output Level, Including Receive Filter	$V = 2.05$ Vrms, $R_L = 600Ω$ (Notes 4, 5) $V = 1.75$ Vrms, $R_L = 300Ω$	**−0.1** −0.1		**0.1** 0.1	dB dB
S/D_p	Signal/Distortion	$V = 2.05$ Vrms, $R_L = 600Ω$ (Notes 4, 5) $V = 1.75$ Vrms, $R_L = 300Ω$			**−45** −45	dB dB
VOSP	Output DC Offset, PWRO+, PWRO−	PWRI Connected to GNDA	**−50**		**50**	mV
PSRR5	Power Supply Rejection of V_{CC} or V_{BB}	PWRI Connected to GNDA	**45**			dB

Note 1: Maximum power consumption will depend on the load impedance connected to the power amplifier. This specification listed assumes 0 dBm is delivered to 600Ω connected from PWRO+ to PWRO−.

Note 2: Voltage input to receive filter at 0V, VF_RO connected to PWRI, 600Ω from PWRO+ to PWRO−. Output measured from PWRO+ to PWRO−.

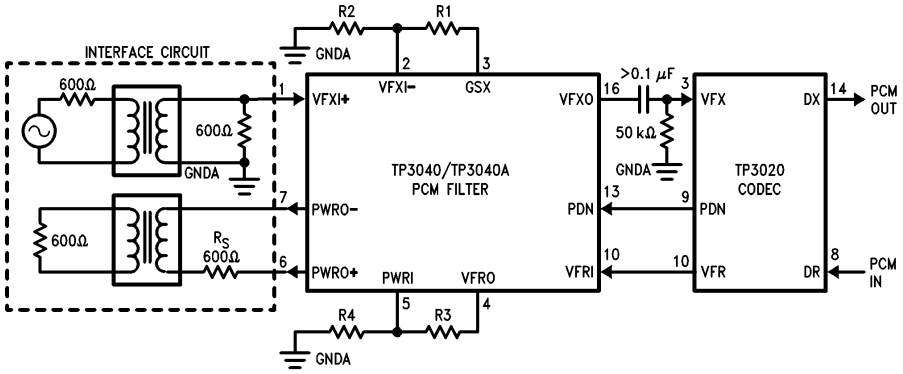
Note 3: The 0 dBm0 level for the filter is assumed to be 1.54 Vrms measured at the output of the XMT or RCV filter.

Note 4: The 0 dBm0 level for the power amplifiers is load dependent. For $R_L = 600Ω$ to GNDA, the 0 dBm0 level is 1.43 Vrms measured at the amplifier output. For $R_L = 300Ω$ the 0 dBm0 level is 1.22 Vrms.

Note 5: VF_RO connected to PWRI, input signal applied to VF_RI.

Note 6: Previous revisions of the datasheet did not clearly indicate this specification requires power amps in powerdown (PWRI = −5.25V).

Typical Application



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Note 1: Transmit voltage gain $= \frac{R1 + R2}{R2} \times \sqrt{2}$ (The filter itself introduces a 3 dB gain), $(R1 + R2 \ge 10k)$

Note 2: Receive gain $= \frac{R4}{R3 + R4}$

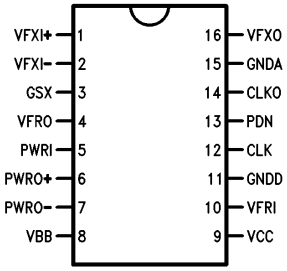
$(R3 + R4 \ge 10k)$

Note: In the configuration shown, the receive filter power amplifiers will drive a 600Ω T to R termination to a maximum signal level of 8.5 dBm. An alternative arrangement, using a transformer winding ratio equivalent to 1.414:1 and 300Ω resistor, R_S, will provide a maximum signal level of 10.1 dBm across a 600Ω termination impedance.

FIGURE 2

Connection Diagrams

Dual-In-Line Package



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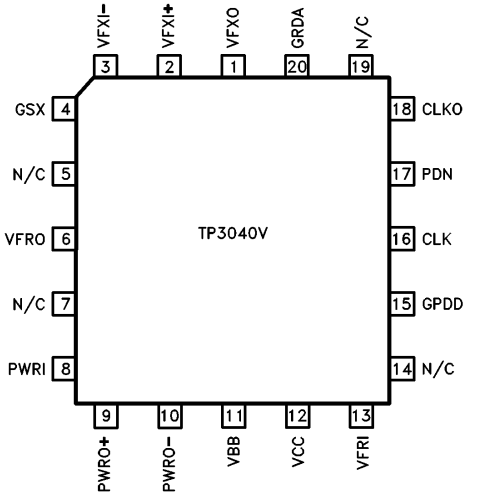
Top View

Order Number TP3040J or TP3040AJ
See NS Package J16A
or
TP3040N or TP3040AN
See NS Package N16A

Plastic Lead Chip Carrier



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Order Number TP3040V or TP3040AV
See NS Package V20A

Description of Pin Functions

Symbol	Function
VF_xI+	The non-inverting input to the transmit filter stage.
VF_xI-	The inverting input to the transmit filter stage.
GS_x	The output used for gain adjustments of the transmit filter.
VF_RO	The low power receive filter output. This pin can directly drive the receive port of an electronic hybrid.
PWRI	The input to the receive filter differential power amplifier.
PWRO+	The non-inverting output of the receive filter power amplifier. This output can directly interface conventional transformer hybrids.
PWRO−	The inverting output of the receive filter power amplifier. This output can be used with PWRO+ to differentially drive a transformer hybrid.
V_{BB}	The negative power supply pin. Recommended input is −5V.
V_{CC}	The positive power supply pin. The recommended input is 5V.
VF_RI	The input pin for the receive filter stage.

Symbol	Function
GNDD	Digital ground input pin. All digital signals are referenced to this pin.
CLK	Master input clock. Input frequency can be selected as 2.048 MHz, 1.544 MHz or 1.536 MHz.
PDN	The input pin used to power down the TP3040/TP3040A during idle periods. Logic 1 (V_{CC}) input voltage causes a power down condition. An internal pull-up is provided.
CLK0	This input pin selects internal counters in accordance with the CLK input clock frequency:

CLK	Connect CLK0 to:
2048 kHz	V_{CC}
1544 kHz	GNDD
1536 kHz	V_{BB}

An internal pull-up is provided.

GNDA	Analog ground input pin. All analog signals are referenced to this pin. Not internally connected to GNDD.
VF_xO	The output of the transmit filter stage.

Functional Description

The TP3040/TP3040A monolithic filter contains four main sections; Transmit Filter, Receive Filter, Receive Filter Power Amplifier, and Frequency Divider/Select Logic (*Figure 1*). A brief description of the circuit operation for each section is provided below.

TRANSMIT FILTER

The input stage of the transmit filter is a CMOS operational amplifier which provides an input resistance of greater than 10 MΩ, a voltage gain of greater than 5,000, low power consumption (less than 3 mW), high power supply rejection, and is capable of driving a 10 kΩ load in parallel with up to 25 pF. The inputs and output of the amplifier are accessible for added flexibility. Non-inverting mode, inverting mode, or differential amplifier mode operation can be implemented with external resistors. It can also be connected to provide a gain of up to 20 dB without degrading the overall filter performance.

The input stage is followed by a prefilter which is a two-pole RC active low pass filter designed to attenuate high frequency noise before the input signal enters the switched-capacitor high pass and low pass filters.

A high pass filter is provided to reject 200 Hz or lower noise which may exist in the signal path. The low pass portion of the switched-capacitor filter provides stopband attenuation which exceeds the D3 and D4 specifications as well as the CCITT G712 recommendations *(Figure 3).*

The output stage of the transmit filter, the postfilter, is also a two-pole RC active low pass filter which attenuates clock frequency noise by at least 40 dB. The output of the transmit filter is capable of driving a ±3.2V peak to peak signal into a 10 kΩ load in parallel with up to 25 pF.

RECEIVE FILTER

The input stage of the receive filter is a prefilter which is similar to the transmit prefilter. The prefilter attenuates high frequency noise that may be present on the receive input signal. A switched capacitor low pass filter follows the prefilter to provide the necessary passband flatness, stopband rejection and sin x/x gain correction. A postfilter which is similar to the transmit postfilter follows the low pass stage. It attenuates clock frequency noise and provides a low output impedance capable of directly driving an electronic subscriber-line-interface circuit *(Figure 3).*

RECEIVE FILTER POWER AMPLIFIERS

Two power amplifiers are also provided to interface to transformer coupled line circuits. These two amplifiers are driven by the output of the receive postfilter through gain setting resistors, R3, R4 (*Figure 2*). The power amplifiers can be deactivated, when not required, by connecting the power amplifier input (pin 5) to the negative power supply V_{BB}. This reduces the total filter power consumption by approximately 10 mW–20 mW depending on output signal amplitude.

POWER DOWN CONTROL

A power down mode is also provided. A logic 1 power down command applied on the PDN pin (pin 13) will reduce the total filter power consumption to less than 1 mW. Connect PDN to GNDD for normal operation.

FREQUENCY DIVIDER AND SELECT LOGIC CIRCUIT

This circuit divides the external clock frequency down to the switching frequency of the low pass and high pass switched capacitor filters. The divider also contains a TTL-CMOS interface circuit which converts the external TTL clock level to the CMOS logic level required for the divider logic. This interface circuit can also be directly driven by CMOS logic. A frequency select circuit is provided to allow the filter to operate with 2.048 MHz, 1.544 MHz or 1.536 MHz clock frequencies. By connecting the frequency select pin CLK0 (pin 14) to V_{CC}, a 2.048 MHz clock input frequency is selected. Digital ground selects 1.544 MHz and V_{BB} selects 1.536 MHz.

Applications Information

GAIN ADJUST

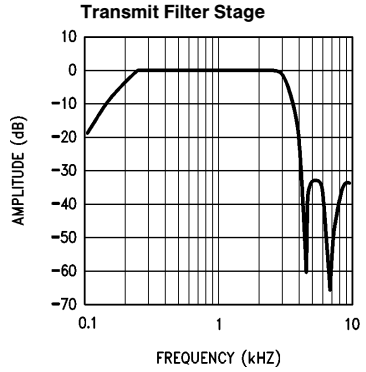
Figure 2 shows the signal path interconnections between the TP3040/TP3040A and the TP3020 signal-channel CODEC. The transmit RC coupling components have been chosen both for minimum passband droop and to present the correct impedance to the CODEC during sampling.

Optimum noise and distortion performance will be obtained from the TP3040/TP3040A filter when operated with system peak overload voltages of ±2.5V to ±3.2V at VF_XO and VF_RO. When interfacing to a PCM CODEC with a peak overload voltage outside this range, further gain or attenuation may be required.

BOARD LAYOUT

Care must be taken in PCB layout to minimize power supply and ground noise. Analog ground (GNDA) of each filter should be connected to digital ground (GNDD) at a single point, which should be bypassed to both power supplies. Further power supply decoupling adjacent to each filter and CODEC is recommended. Ground loops should be avoided, both between GNDA and GNDD and between the GNDA traces of adjacent filters and CODECs.

Typical Performance Characteristics



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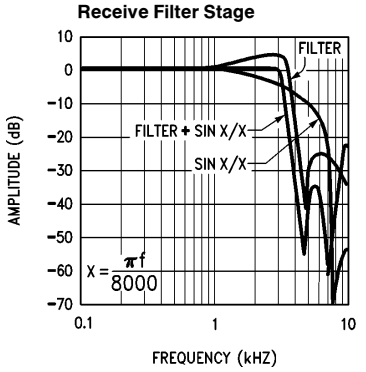

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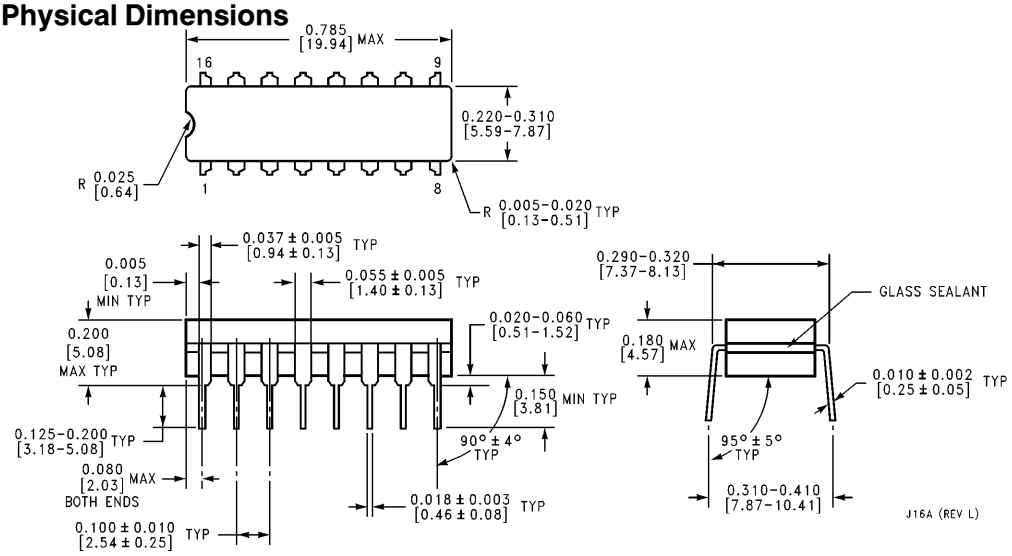
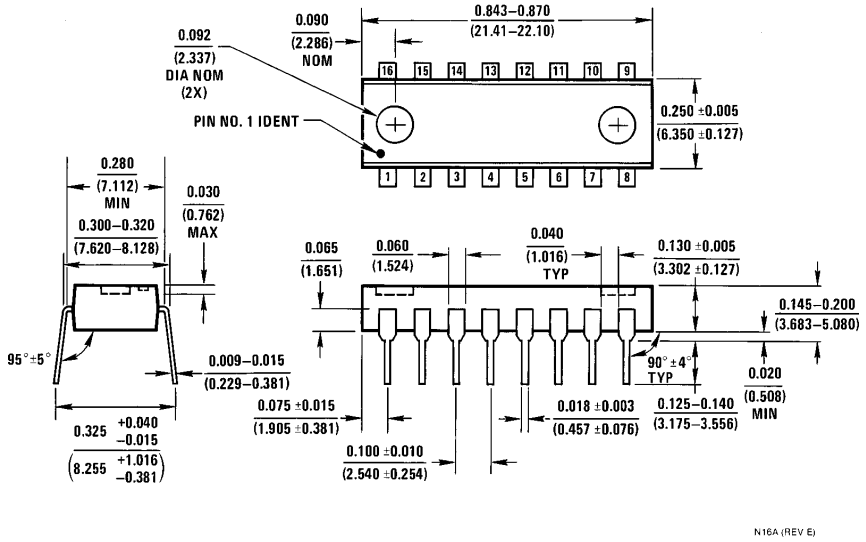
FIGURE 3

Physical Dimensions



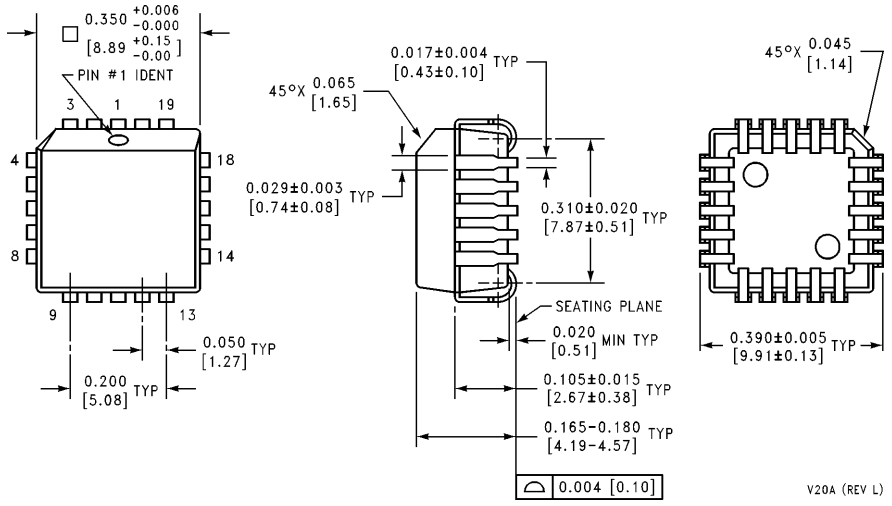
Ceramic Dual-In-Line Package (J)
Order Number TP3040J or TP3040AJ
NS Package Number J16A



Molded Dual-In-Line Package (M)
Order Number TP3040N or TP3040AN
NS Package Number N16A

Physical Dimensions (Continued)

Lit. # 113919



20-Lead Plastic Chip Carrier
Order Number TP3040V or TP3040AV
NS Package Number V20A

LIFE SUPPORT POLICY

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1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

National Semiconductor Corporation
1111 West Bardin Road
Arlington, TX 76017
Tel: 1(800) 272-9959
Fax: 1(800) 737-7018

National Semiconductor Europe
Fax: (+49) 0-180-530 85 86
Email: cnjwge@tevm2.nsc.com
Deutsch Tel: (+49) 0-180-530 85 85
English Tel: (+49) 0-180-532 78 32
Français Tel: (+49) 0-180-532 93 58
Italiano Tel: (+49) 0-180-534 16 80

National Semiconductor Hong Kong Ltd.
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 2737-1600
Fax: (852) 2736-9960

National Semiconductor Japan Ltd.
Tel: 81-043-299-2309
Fax: 81-043-299-2408

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