

OKI Semiconductor

MSM5116165D/DSL

1,048,576-Word × 16-Bit DYNAMIC RAM : FAST PAGE MODE TYPE WITH EDO

DESCRIPTION

The MSM5116165D/DSL is a 1,048,576-word × 16-bit dynamic RAM fabricated in Oki's silicon-gate CMOS technology. The MSM5116165D/DSL achieves high integration, high-speed operation, and low-power consumption because Oki manufactures the device in a quadruple-layer polysilicon/double-layer metal CMOS process. The MSM5116165D/DSL is available in a 42-pin plastic SOJ or 50/44-pin plastic TSOP. The MSM5116165DSL (the self-refresh version) is specially designed for lower-power applications.

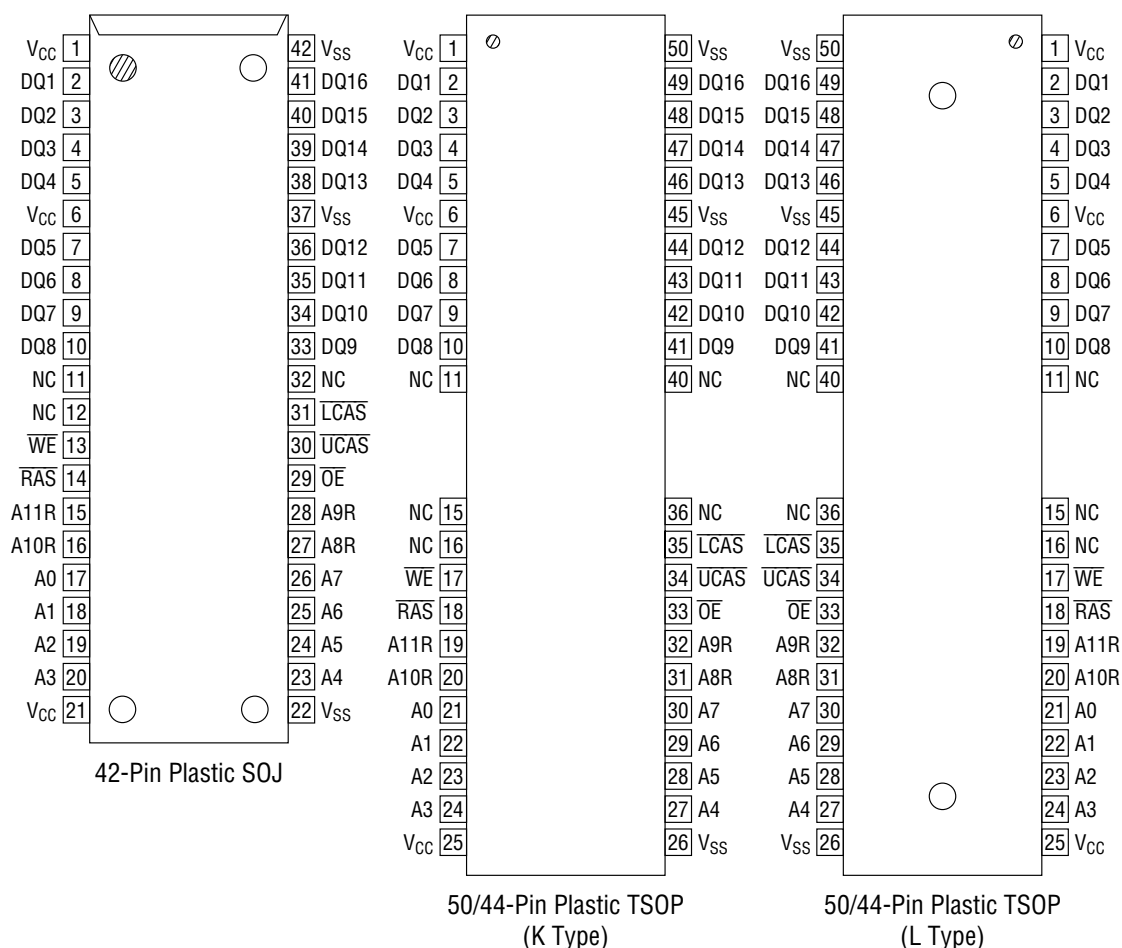
FEATURES

- 1,048,576-word × 16-bit configuration
 - Single 5 V power supply, ±10% tolerance
 - Input : TTL compatible, low input capacitance
 - Output : TTL compatible, 3-state
 - Refresh : 4096 cycles/64 ms, 4096 cycles/128 ms (SL version)
 - Fast page mode with EDO, read modify write capability
 - $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh, hidden refresh, $\overline{\text{RAS}}$ -only refresh capability
 - $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self-refresh capability (SL version)
 - Package options:
 - 42-pin 400 mil plastic SOJ (SOJ42-P-400-1.27) (Product : MSM5116165D/DSL-xxJS)
 - 50/44-pin 400 mil plastic TSOP (TSOPII50/44-P-400-0.80-K) (Product : MSM5116165D/DSL-xxTS-K)
 - (TSOPII50/44-P-400-0.80-L) (Product : MSM5116165D/DSL-xxTS-L)
- xx indicates speed rank.

PRODUCT FAMILY

Family	Access Time (Max.)				Cycle Time (Min.)	Power Dissipation	
	t _{RAC}	t _{AA}	t _{CAC}	t _{OE}		Operating (Max.)	Standby (Max.)
MSM5116165D/DSL-50	50 ns	25 ns	13 ns	13 ns	84 ns	633 mW	5.5 mW/ 1.1 mW (SL version)
MSM5116165D/DSL-60	60 ns	30 ns	15 ns	15 ns	104 ns	578 mW	
MSM5116165D/DSL-70	70 ns	35 ns	20 ns	20 ns	124 ns	523 mW	

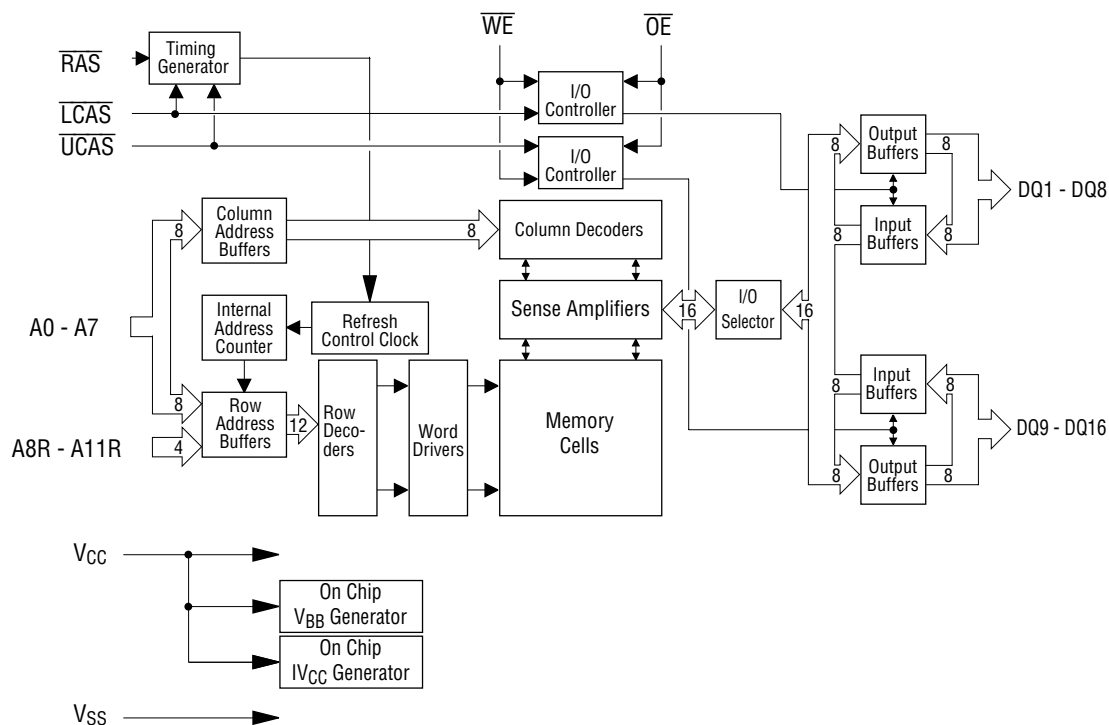
PIN CONFIGURATION (TOP VIEW)



Pin Name	Function
A0 - A7, A8R - A11R	Address Input
RAS	Row Address Strobe
LCAS	Lower Byte Column Address Strobe
UCAS	Upper Byte Column Address Strobe
DQ1 - DQ16	Data Input/Data Output
OE	Output Enable
WE	Write Enable
V _{CC}	Power Supply (5 V)
V _{SS}	Ground (0 V)
NC	No Connection

Note : The same power supply voltage must be provided to every V_{CC} pin, and the same GND voltage level must be provided to every V_{SS} pin.

BLOCK DIAGRAM



FUNCTION TABLE

Input Pin					DQ Pin		Function Mode
RAS	LCAS	UCAS	WE	OE	DQ1 - DQ8	DQ9 - DQ16	
H	*	*	*	*	High-Z	High-Z	Standby
L	H	H	*	*	High-Z	High-Z	Refresh
L	L	H	H	L	D _{OUT}	High-Z	Lower Byte Read
L	H	L	H	L	High-Z	D _{OUT}	Upper Byte Read
L	L	L	H	L	D _{OUT}	D _{OUT}	Word Read
L	L	H	L	H	D _{IN}	Don't Care	Lower Byte Write
L	H	L	L	H	Don't Care	D _{IN}	Upper Byte Write
L	L	L	L	H	D _{IN}	D _{IN}	Word Write
L	L	L	H	H	High-Z	High-Z	—

*: "H" or "L"

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	-0.5 to $V_{CC} + 0.5$	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	-0.5 to 7	V
Short Circuit Output Current	I_{OS}	50	mA
Power Dissipation	P_D^*	1	W
Operating Temperature	T_{opr}	0 to 70	°C
Storage Temperature	T_{stg}	-55 to 150	°C

*: $T_a = 25^{\circ}\text{C}$

Recommended Operating Conditions

($T_a = 0^{\circ}\text{C}$ to 70°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	$V_{CC} + 0.5^{*1}$	V
Input Low Voltage	V_{IL}	-0.5^{*2}	—	0.8	V

Notes : *1. The input voltage is $V_{CC} + 2.0\text{ V}$ when the pulse width is less than 20 ns (the pulse width is with respect to the point at which V_{CC} is applied).

*2. The input voltage is $V_{SS} - 2.0\text{ V}$ when the pulse width is less than 20 ns (the pulse width is with respect to the point at which V_{SS} is applied).

Capacitance

($V_{CC} = 5\text{ V} \pm 10\%$, $T_a = 25^{\circ}\text{C}$, $f = 1\text{ MHz}$)

Parameter	Symbol	Typ.	Max.	Unit
Input Capacitance (A0 - A7, A8R - A11R)	C_{IN1}	—	5	pF
Input Capacitance ($\overline{\text{RAS}}$, $\overline{\text{LCAS}}$, $\overline{\text{UCAS}}$, $\overline{\text{WE}}$, $\overline{\text{OE}}$)	C_{IN2}	—	7	pF
Output Capacitance (DQ1 - DQ16)	$C_{I/O}$	—	7	pF

DC Characteristics

(V_{CC} = 5 V ±10%, T_a = 0°C to 70°C)

Parameter	Symbol	Condition	MSM5116165 D/DSL-50		MSM5116165 D/DSL-60		MSM5116165 D/DSL-70		Unit	Note
			Min.	Max.	Min.	Max.	Min.	Max.		
Output High Voltage	V _{OH}	I _{OH} = -5.0 mA	2.4	V _{CC}	2.4	V _{CC}	2.4	V _{CC}	V	
Output Low Voltage	V _{OL}	I _{OL} = 4.2 mA	0	0.4	0	0.4	0	0.4	V	
Input Leakage Current	I _{LI}	0 V ≤ V _I ≤ 6.5 V; All other pins not under test = 0 V	-10	10	-10	10	-10	10	μA	
Output Leakage Current	I _{LO}	DQ disable 0 V ≤ V _O ≤ V _{CC}	-10	10	-10	10	-10	10	μA	
Average Power Supply Current (Operating)	I _{CC1}	$\overline{\text{RAS}}$, $\overline{\text{CAS}}$ cycling, t _{RC} = Min.	—	90	—	85	—	80	mA	1, 2
Power Supply Current (Standby)	I _{CC2}	$\overline{\text{RAS}}$, $\overline{\text{CAS}}$ = V _{IH}	—	2	—	2	—	2	mA	1
		$\overline{\text{RAS}}$, $\overline{\text{CAS}}$	—	1	—	1	—	1	μA	1, 5
		≥ V _{CC} - 0.2 V	—	200	—	200	—	200	μA	1, 5
Average Power Supply Current ($\overline{\text{RAS}}$ -only Refresh)	I _{CC3}	$\overline{\text{RAS}}$ cycling, $\overline{\text{CAS}}$ = V _{IH} , t _{RC} = Min.	—	90	—	85	—	80	mA	1, 2
Power Supply Current (Standby)	I _{CC5}	$\overline{\text{RAS}}$ = V _{IH} , $\overline{\text{CAS}}$ = V _{IL} , DQ = enable	—	5	—	5	—	5	mA	1
Average Power Supply Current ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh)	I _{CC6}	$\overline{\text{RAS}}$ cycling, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$	—	90	—	85	—	80	mA	1, 2
Average Power Supply Current (Fast Page Mode)	I _{CC7}	$\overline{\text{RAS}}$ = V _{IL} , $\overline{\text{CAS}}$ cycling, t _{HPC} = Min.	—	115	—	105	—	95	mA	1, 3
Average Power Supply Current (Battery Backup)	I _{CC10}	t _{RC} = 125 μs, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$, t _{RAS} ≤ 1 μs	—	400	—	400	—	400	μA	1, 4, 5
Average Power Supply Current ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Self-Refresh)	I _{CCS}	$\overline{\text{RAS}}$ ≤ 0.2 V, $\overline{\text{CAS}}$ ≤ 0.2 V	—	300	—	300	—	300	μA	1, 5

- Notes :
1. I_{CC} Max. is specified as I_{CC} for output open condition.
 2. The address can be changed once or less while $\overline{\text{RAS}}$ = V_{IL}.
 3. The address can be changed once or less while $\overline{\text{CAS}}$ = V_{IH}.
 4. V_{CC} - 0.2 V ≤ V_{IH} ≤ V_{CC} + 0.5 V, -0.5 V ≤ V_{IL} ≤ 0.2 V.
 5. SL version.

AC Characteristics (1/2)

(V_{CC} = 5 V ±10%, T_a = 0°C to 70°C) Note 1, 2, 3

Parameter	Symbol	MSM5116165 D/DSL-50		MSM5116165 D/DSL-60		MSM5116165 D/DSL-70		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Random Read or Write Cycle Time	t _{RC}	84	—	104	—	124	—	ns	
Read Modify Write Cycle Time	t _{RWC}	131	—	155	—	185	—	ns	
Fast Page Mode Cycle Time	t _{HPC}	20	—	25	—	30	—	ns	
Fast Page Mode Read Modify Write Cycle Time	t _{HPRWC}	58	—	68	—	78	—	ns	
Access Time from $\overline{\text{RAS}}$	t _{RAC}	—	50	—	60	—	70	ns	4, 5, 6
Access Time from $\overline{\text{CAS}}$	t _{CAC}	—	13	—	15	—	20	ns	4, 5
Access Time from Column Address	t _{AA}	—	25	—	30	—	35	ns	4, 6
Access Time from $\overline{\text{CAS}}$ Precharge	t _{CPA}	—	30	—	35	—	40	ns	4, 13
Access Time from $\overline{\text{OE}}$	t _{OEa}	—	13	—	15	—	20	ns	4
Output Low Impedance Time from $\overline{\text{CAS}}$	t _{CLZ}	0	—	0	—	0	—	ns	4
Data Output Hold After $\overline{\text{CAS}}$ Low	t _{DOH}	5	—	5	—	5	—	ns	
$\overline{\text{CAS}}$ to Data Output Buffer Turn-off Delay Time	t _{CEZ}	0	13	0	15	0	20	ns	7, 8
$\overline{\text{RAS}}$ to Data Output Buffer Turn-off Delay Time	t _{REZ}	0	13	0	15	0	20	ns	7, 8
$\overline{\text{OE}}$ to Data Output Buffer Turn-off Delay Time	t _{OEZ}	0	13	0	15	0	20	ns	7
$\overline{\text{WE}}$ to Data Output Buffer Turn-off Delay Time	t _{WEZ}	0	13	0	15	0	20	ns	7
Transition Time	t _T	1	50	1	50	1	50	ns	3
Refresh Period	t _{REF}	—	64	—	64	—	64	ms	
Refresh Period (SL version)	t _{REF}	—	128	—	128	—	128	ms	16
$\overline{\text{RAS}}$ Precharge Time	t _{RP}	30	—	40	—	50	—	ns	
$\overline{\text{RAS}}$ Pulse Width	t _{RAS}	50	10,000	60	10,000	70	10,000	ns	
$\overline{\text{RAS}}$ Pulse Width (Fast Page Mode with EDO)	t _{RASP}	50	100,000	60	100,000	70	100,000	ns	
$\overline{\text{RAS}}$ Hold Time	t _{RSH}	7	—	10	—	13	—	ns	
$\overline{\text{RAS}}$ Hold Time referenced to $\overline{\text{OE}}$	t _{ROH}	7	—	10	—	13	—	ns	
$\overline{\text{CAS}}$ Precharge Time (Fast Page Mode with EDO)	t _{CP}	7	—	10	—	10	—	ns	15
$\overline{\text{CAS}}$ Pulse Width	t _{CAS}	7	10,000	10	10,000	13	10,000	ns	
$\overline{\text{CAS}}$ Hold Time	t _{CSH}	35	—	40	—	45	—	ns	
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	t _{CRP}	5	—	5	—	5	—	ns	13
$\overline{\text{RAS}}$ Hold Time from $\overline{\text{CAS}}$ Precharge	t _{RHCP}	30	—	35	—	40	—	ns	13
$\overline{\text{OE}}$ Hold Time from $\overline{\text{CAS}}$ (DQ Disable)	t _{CHO}	5	—	5	—	5	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	t _{RCD}	11	37	14	45	14	50	ns	5
$\overline{\text{RAS}}$ to Column Address Delay Time	t _{RAD}	9	25	12	30	12	35	ns	6
Row Address Set-up Time	t _{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t _{RAH}	7	—	10	—	10	—	ns	
Column Address Set-up Time	t _{ASC}	0	—	0	—	0	—	ns	12
Column Address Hold Time	t _{CAH}	7	—	10	—	13	—	ns	12
Column Address to $\overline{\text{RAS}}$ Lead Time	t _{RAL}	25	—	30	—	35	—	ns	

AC Characteristics (2/2)

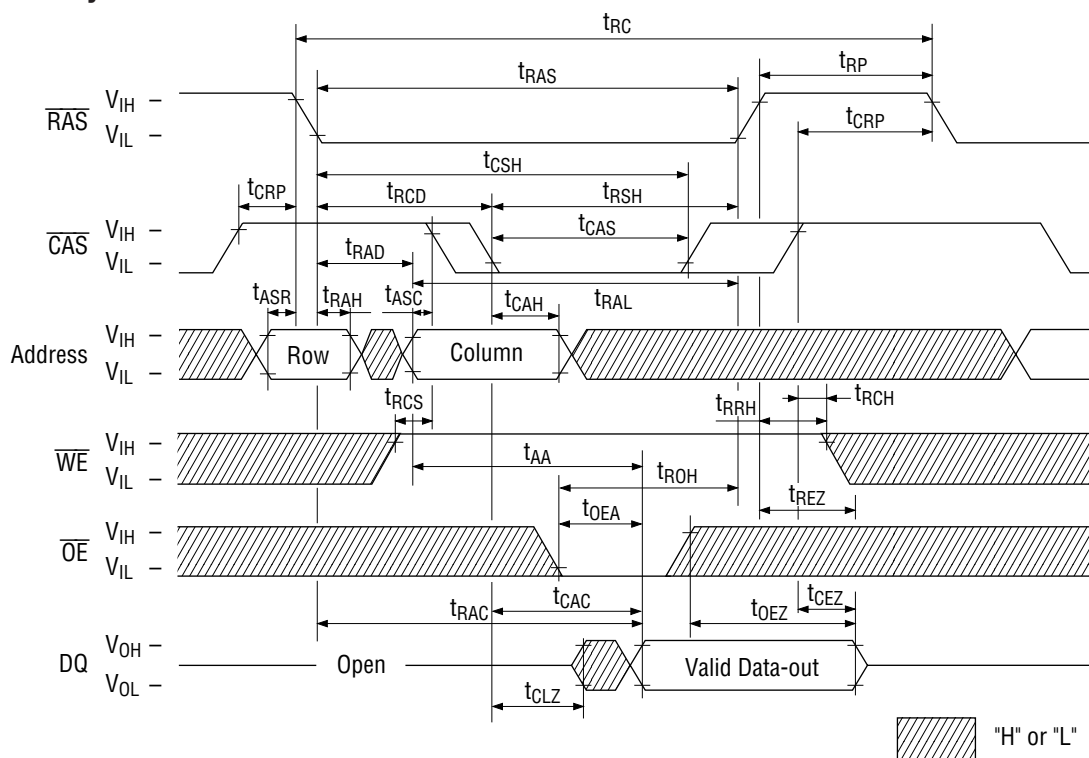
(V_{CC} = 5 V ±10%, T_a = 0°C to 70°C) Note 1, 2, 3

Parameter	Symbol	MSM5116165 D/DSL-50		MSM5116165 D/DSL-60		MSM5116165 D/DSL-70		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Read Command Set-up Time	t _{RCS}	0	—	0	—	0	—	ns	12
Read Command Hold Time	t _{RCH}	0	—	0	—	0	—	ns	9, 12
Read Command Hold Time referenced to $\overline{\text{RAS}}$	t _{RRH}	0	—	0	—	0	—	ns	9
Write Command Set-up Time	t _{WCS}	0	—	0	—	0	—	ns	10, 12
Write Command Hold Time	t _{WCH}	7	—	10	—	13	—	ns	12
Write Command Pulse Width	t _{WP}	7	—	10	—	10	—	ns	
$\overline{\text{WE}}$ Pulse Width (DQ Disable)	t _{WPE}	7	—	10	—	10	—	ns	
$\overline{\text{OE}}$ Command Hold Time	t _{OEh}	7	—	10	—	13	—	ns	
$\overline{\text{OE}}$ Precharge Time	t _{OEP}	7	—	10	—	10	—	ns	
$\overline{\text{OE}}$ Command Hold Time	t _{OCH}	7	—	10	—	10	—	ns	
Write Command to $\overline{\text{RAS}}$ Lead Time	t _{RWL}	7	—	10	—	13	—	ns	
Write Command to $\overline{\text{CAS}}$ Lead Time	t _{CWL}	7	—	10	—	13	—	ns	14
Data-in Set-up Time	t _{DS}	0	—	0	—	0	—	ns	11, 12
Data-in Hold Time	t _{DH}	7	—	10	—	13	—	ns	11, 12
$\overline{\text{OE}}$ to Data-in Delay Time	t _{OED}	13	—	15	—	20	—	ns	
$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay Time	t _{CWD}	30	—	34	—	44	—	ns	10
Column Address to $\overline{\text{WE}}$ Delay Time	t _{AWD}	42	—	49	—	59	—	ns	10
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Delay Time	t _{RWD}	67	—	79	—	94	—	ns	10
$\overline{\text{CAS}}$ Precharge $\overline{\text{WE}}$ Delay Time	t _{CPWD}	47	—	54	—	64	—	ns	10
$\overline{\text{CAS}}$ Active Delay Time from $\overline{\text{RAS}}$ Precharge	t _{RPC}	5	—	5	—	5	—	ns	12
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Set-up Time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$)	t _{CSR}	5	—	5	—	5	—	ns	12
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Hold Time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$)	t _{CHR}	10	—	10	—	10	—	ns	13
$\overline{\text{RAS}}$ Pulse Width ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Self-Refresh)	t _{RASS}	100	—	100	—	100	—	μs	16
$\overline{\text{RAS}}$ Precharge Time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Self-Refresh)	t _{RPS}	90	—	110	—	130	—	ns	16
$\overline{\text{CAS}}$ Hold Time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Self-Refresh)	t _{CHS}	-50	—	-50	—	-50	—	ns	16

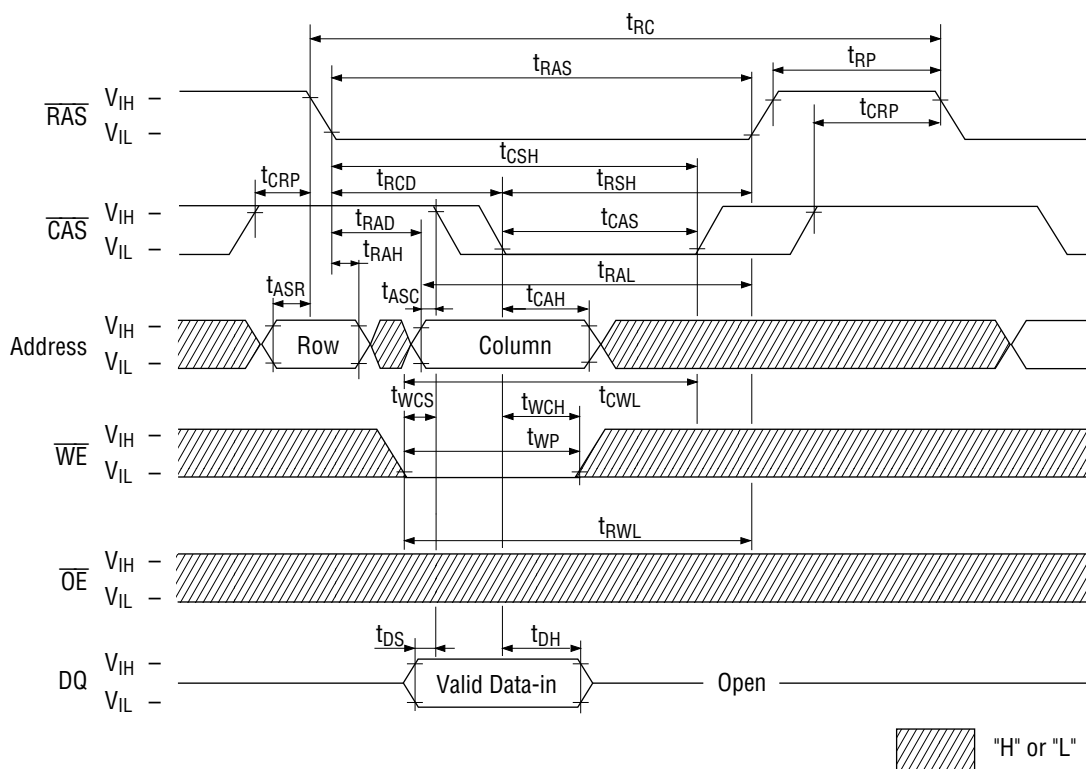
- Notes:
1. A start-up delay of 200 μ s is required after power-up, followed by a minimum of eight initialization cycles ($\overline{\text{RAS}}$ -only refresh or $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh) before proper device operation is achieved.
 2. The AC characteristics assume $t_T = 2$ ns.
 3. V_{IH} (Min.) and V_{IL} (Max.) are reference levels for measuring input timing signals. Transition times (t_T) are measured between V_{IH} and V_{IL} .
 4. This parameter is measured with a load circuit equivalent to 2 TTL loads and 100 pF.
 5. Operation within the t_{RCD} (Max.) limit ensures that t_{RAC} (Max.) can be met. t_{RCD} (Max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (Max.) limit, then the access time is controlled by t_{CAC} .
 6. Operation within the t_{RAD} (Max.) limit ensures that t_{RAC} (Max.) can be met. t_{RAD} (Max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (Max.) limit, then the access time is controlled by t_{AA} .
 7. t_{CEZ} (Max.), t_{REZ} (Max.), t_{WEZ} (Max.) and t_{OEZ} (Max.) define the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.
 8. t_{CEZ} and t_{REZ} must be satisfied for open circuit condition.
 9. t_{RCH} or t_{RRH} must be satisfied for a read cycle.
 10. t_{WCS} , t_{CWD} , t_{RWD} , t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (Min.), then the cycle is an early write cycle and the data out will remain open circuit (high impedance) throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (Min.), $t_{RWD} \geq t_{RWD}$ (Min.), $t_{AWD} \geq t_{AWD}$ (Min.) and $t_{CPWD} \geq t_{CPWD}$ (Min.), then the cycle is a read modify write cycle and data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, then the condition of the data out (at access time) is indeterminate.
 11. These parameters are referenced to the $\overline{\text{UCAS}}$ and $\overline{\text{LCAS}}$, leading edges in an early write cycle, and to the $\overline{\text{WE}}$ leading edge in an $\overline{\text{OE}}$ control write cycle, or a read modify write cycle.
 12. These parameters are determined by the falling edge of either $\overline{\text{UCAS}}$ or $\overline{\text{LCAS}}$, whichever is earlier.
 13. These parameters are determined by the rising edge of either $\overline{\text{UCAS}}$ or $\overline{\text{LCAS}}$, whichever is later.
 14. t_{CWL} should be satisfied by both $\overline{\text{UCAS}}$ and $\overline{\text{LCAS}}$.
 15. t_{CP} is determined by the time both $\overline{\text{UCAS}}$ and $\overline{\text{LCAS}}$ are high.
 16. Only SL version.

TIMING WAVEFORM

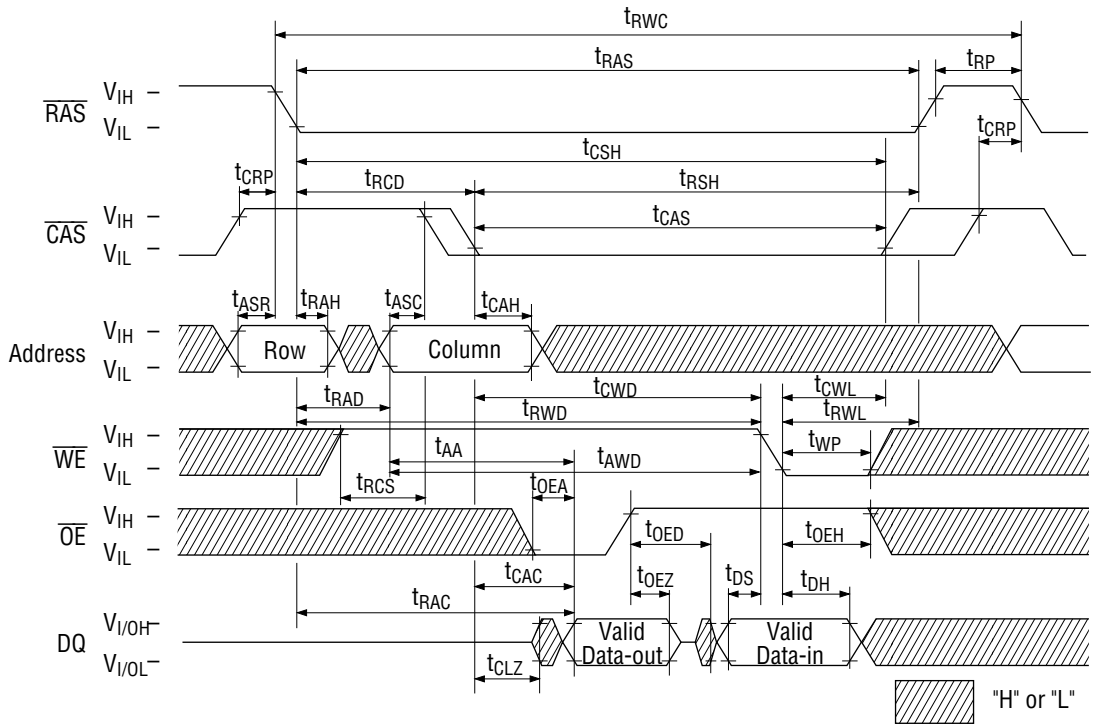
Read Cycle



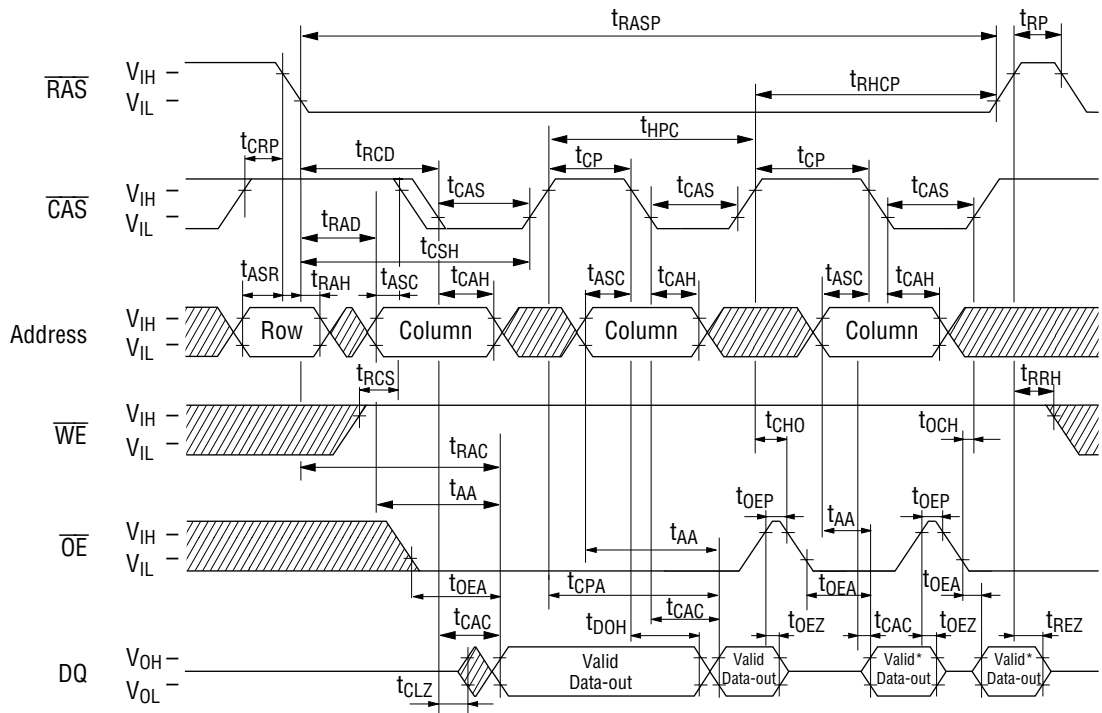
Write Cycle (Early Write)



Read Modify Write Cycle

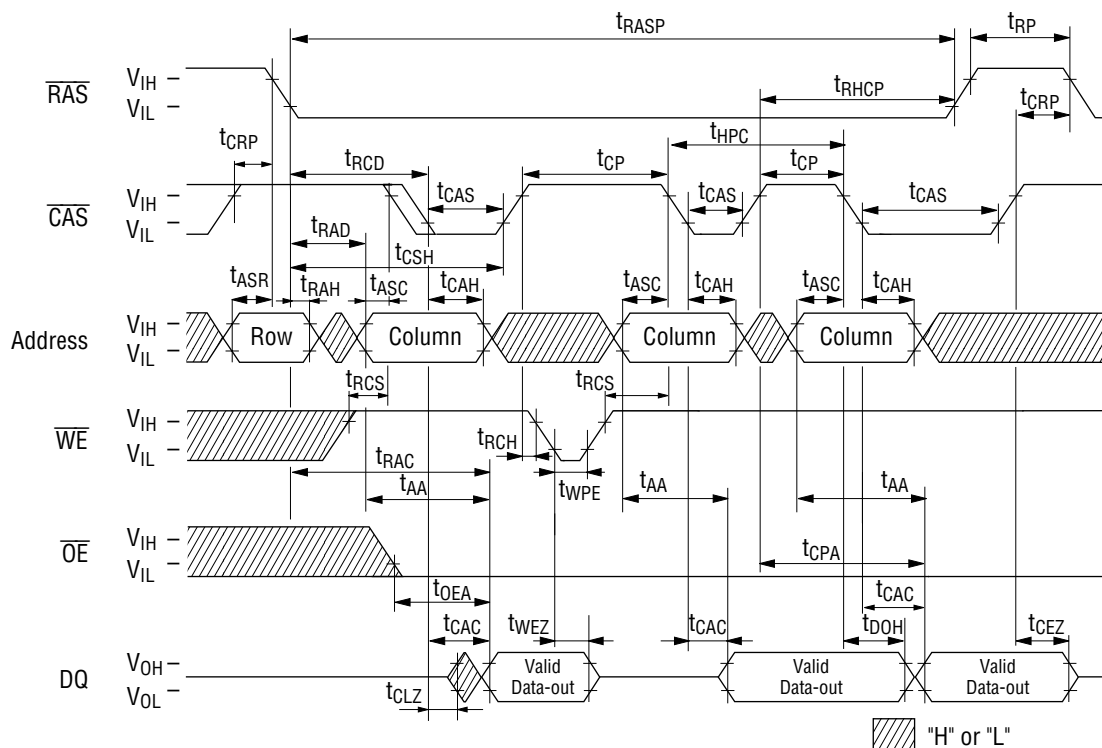


Fast Page Mode Read Cycle (Part-1)



* : Same Data, "H" or "L"

Fast Page Mode Read Cycle (Part-2)



"H" or "L"

The diagram illustrates the timing relationships for a 2D array DRAM. It shows the signals RAS, CAS, Address, WE, OE, and DQ over time. The timing parameters are defined as follows:

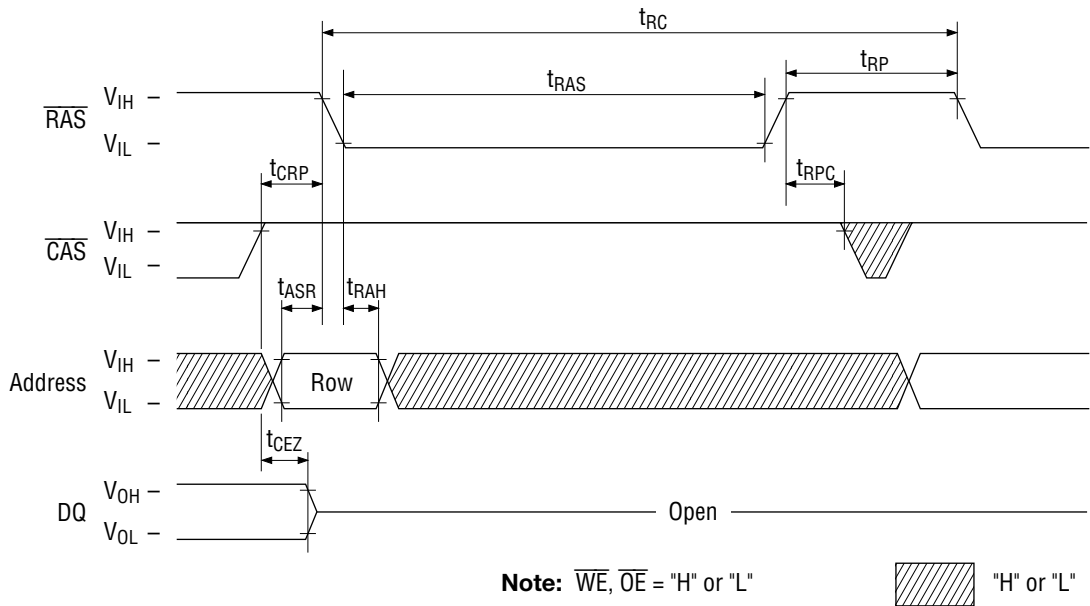
- t_{RAS} : RAS pulse width
- t_{RCD} : RAS to CAS delay
- t_{CAS} : CAS pulse width
- t_{CP} : CAS to Precharge delay
- t_{HPC} : Precharge to High Power Control delay
- t_{CRP} : RAS to Precharge delay
- t_{RAD} : RAS to Array Delay
- t_{CSH} : CAS to High Power Control delay
- t_{ASR} : Address to RAS delay
- t_{RAH} : RAS to Array Delay
- t_{ASC} : Address to CAS delay
- t_{CAH} : CAS to Array Delay
- t_{WCS} : WE to CAS delay
- t_{WCH} : WE to High Power Control delay
- t_{DS} : Data Setup time
- t_{DH} : Data Hold time
- t_{RP} : Precharge to RAS delay

The diagram also shows the valid data-in periods for the DQ signal, which are defined by t_{DS} and t_{DH} . The signals WE, OE, and DQ are shown as shaded areas, indicating they are "H" or "L".

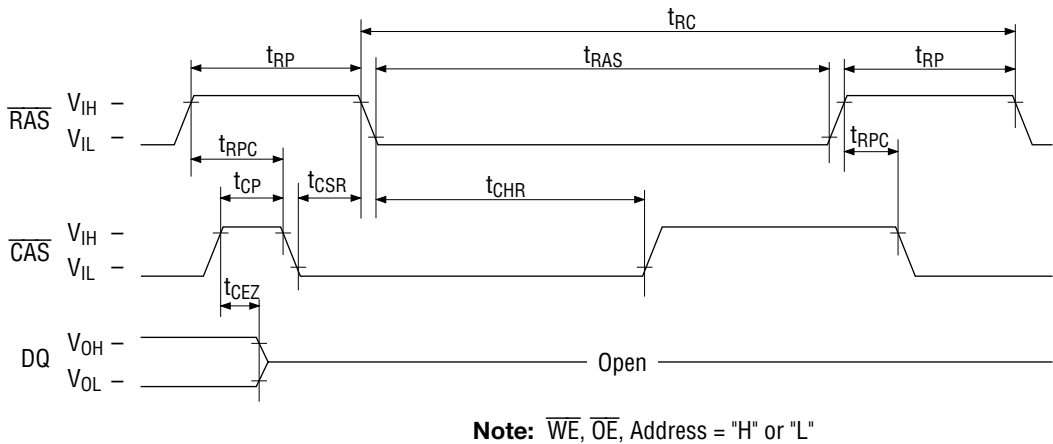
The diagram illustrates the timing relationships for a memory device. The signals shown are RAS, CAS, Address, WE, OE, and DQ. The timing parameters are defined as follows:

- t_{RAS} : RAS pulse width
- t_{RWD} : RAS to WE delay
- t_{CRP} : RAS to CAS setup
- t_{RCD} : RAS to CAS delay
- t_{CP} : CAS to WE delay
- t_{CPWD} : CAS to WE pulse width
- t_{CPA} : CAS to WE setup
- t_{CAH} : CAS to WE hold
- t_{CWL} : CAS to WE delay
- t_{ASC} : CAS to WE delay
- t_{CAH} : CAS to WE hold
- t_{RWL} : RAS to WE delay
- t_{ASR} : Address to WE delay
- t_{RAH} : Address to WE delay
- t_{ASC} : Address to WE delay
- t_{CAH} : Address to WE hold
- t_{RCS} : RAS to WE delay
- t_{AWD} : Address to WE delay
- t_{RCS} : RAS to WE delay
- t_{CWD} : CAS to WE delay
- t_{AA} : Address to WE delay
- t_{DS} : Data to WE delay
- t_{WP} : Data to WE delay
- t_{OE} : OE pulse width
- t_{OEZ} : OE to WE delay
- t_{OEH} : OE to WE delay
- t_{ODH} : OE to WE delay
- t_{CAC} : OE to WE delay
- t_{CLZ} : OE to WE delay

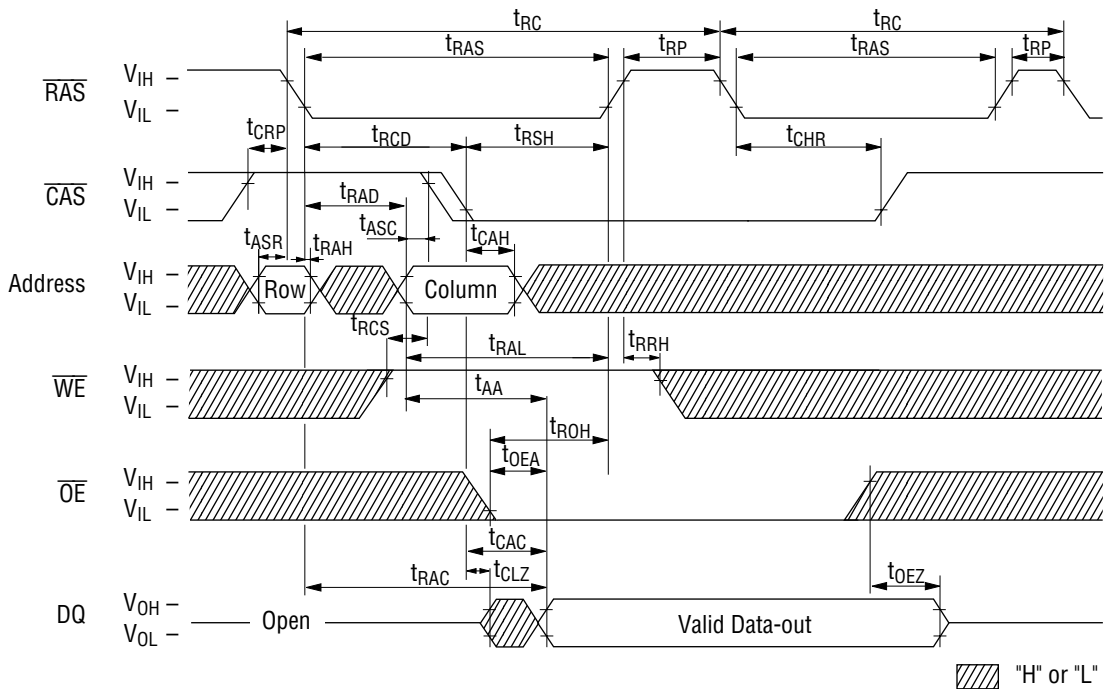
RAS-Only Refresh Cycle



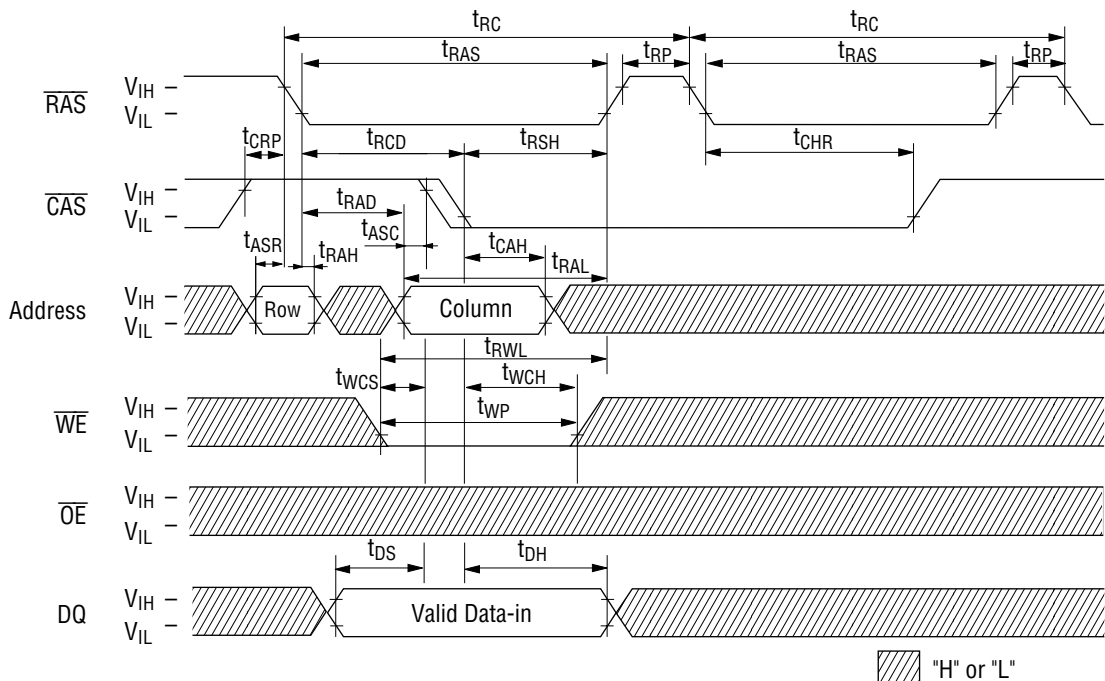
CAS before RAS Refresh Cycle



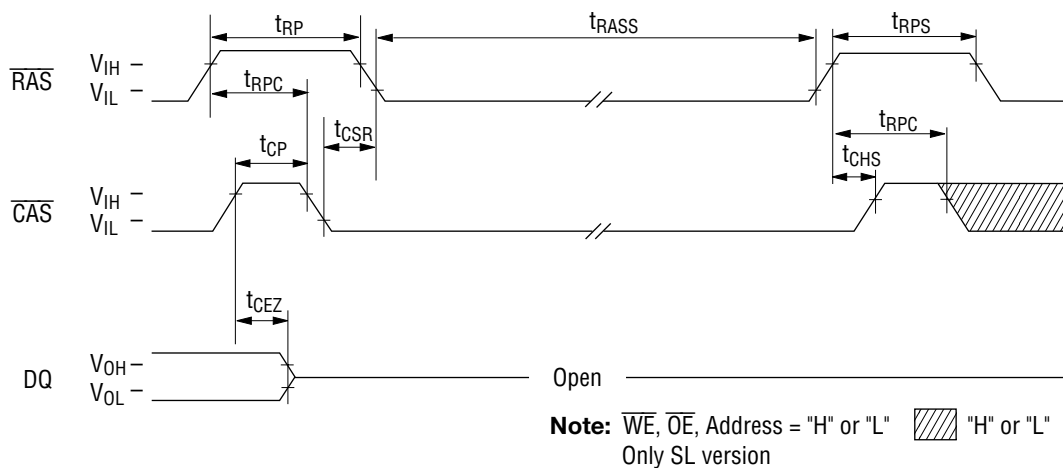
Hidden Refresh Read Cycle



Hidden Refresh Write Cycle

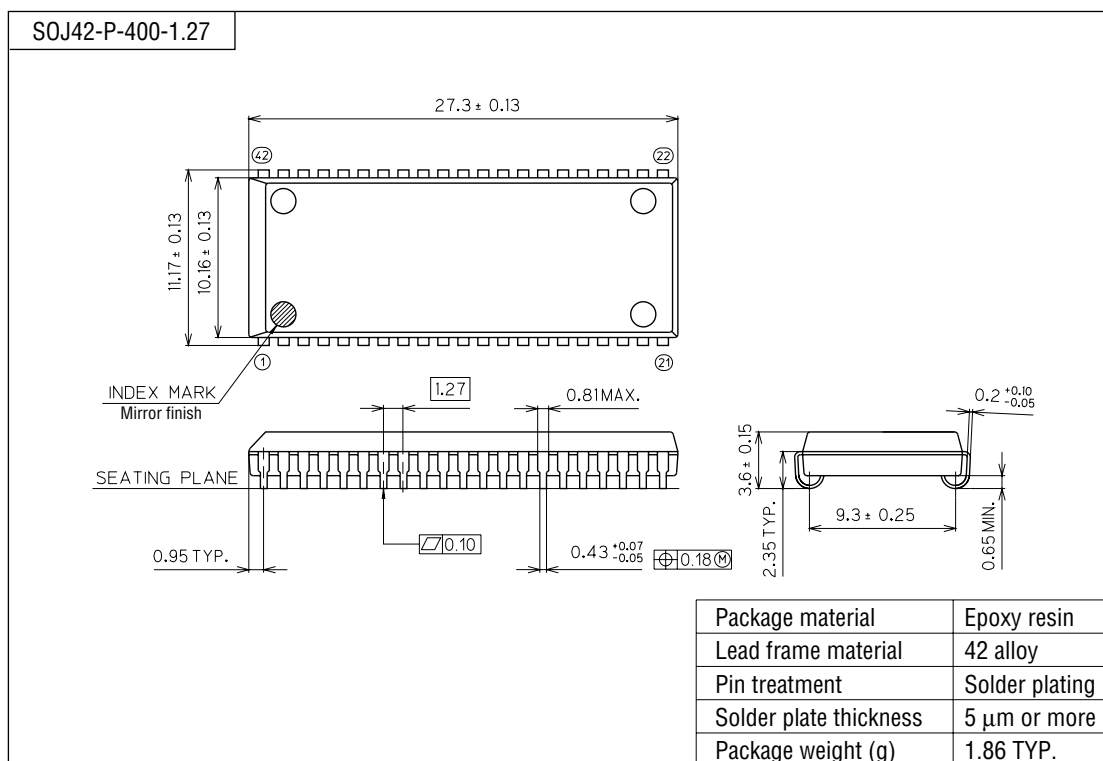


$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Self-Refresh Cycle



PACKAGE DIMENSIONS

(Unit : mm)

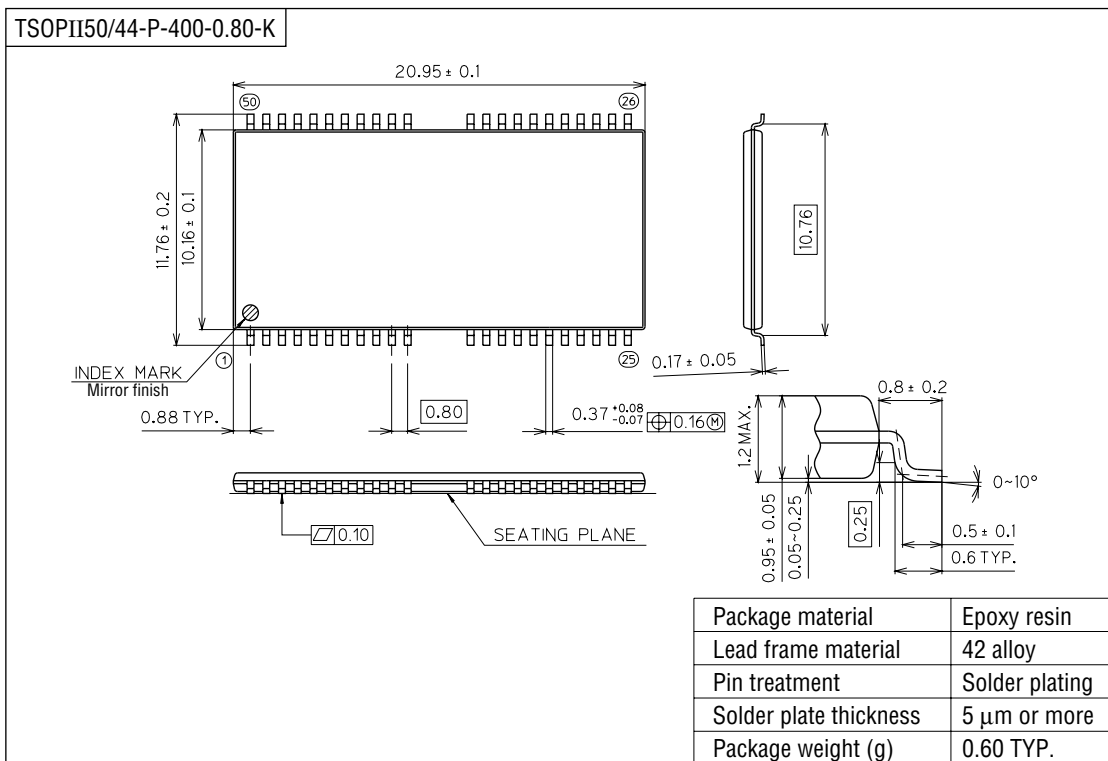


Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.

Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

(Unit : mm)



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