OKI Semiconductor

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MSM80C85AHRS/GS/JS

8-Bit CMOS MICROPROCESSOR

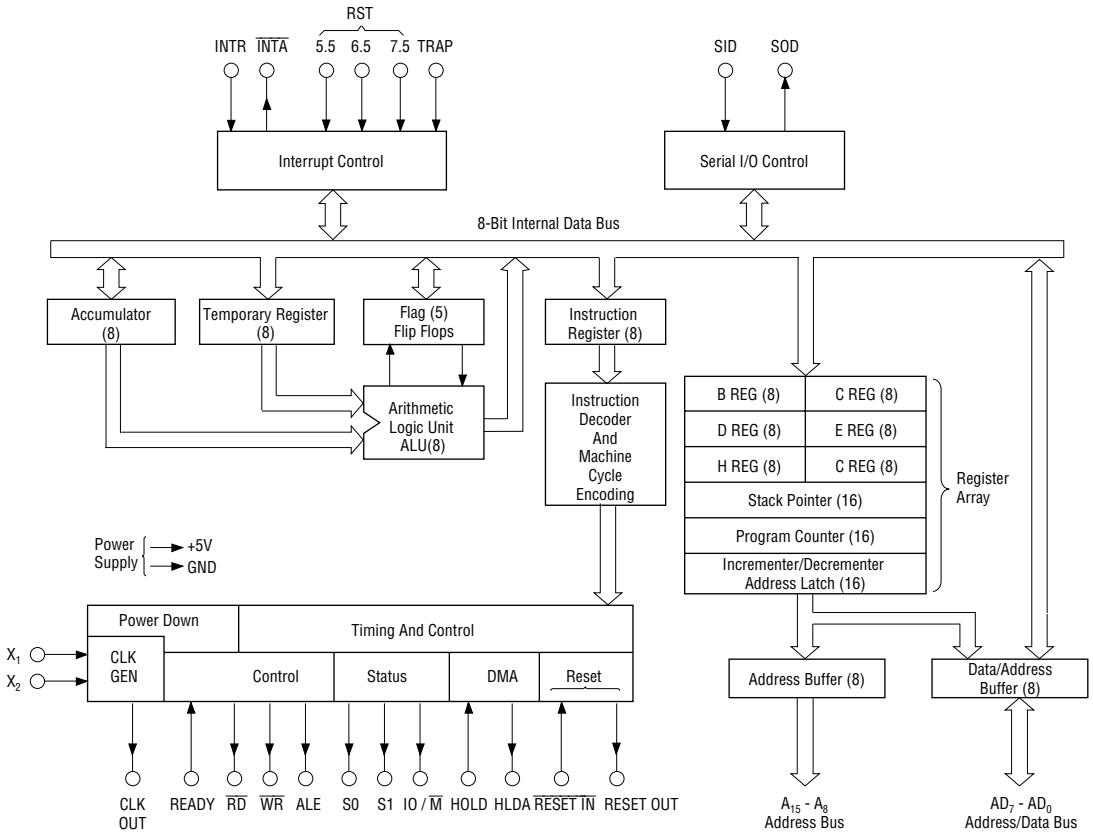
GENRAL DESCRIPTION

The MSM80C85AH is a complete 8-bit parallel; central processor implemented in silicon gate C-MOS technology and compatible with MSM80C85A.
It is designed with higher processing speed (max.5 MHz) and lower power consumption compared with MSM80C85A and power down mode is provided, thereby offering a high level of system integration.
The MSM80C85AH uses a multiplexed address/data bus. The address is split between the 8-bit address bus and the 8-bit data bus. The on-chip address latch : of a MSM81C55-5 memory product allows a direct interface with the MSM80C85AH.

FEATURES

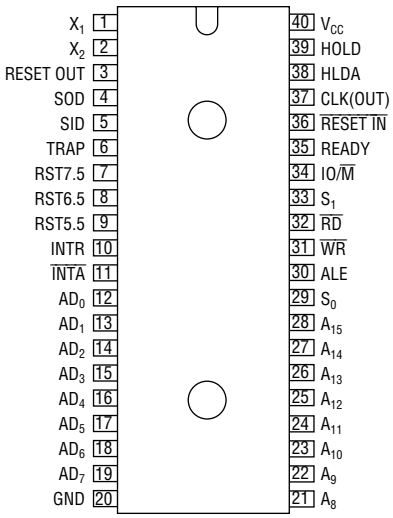
- Power down mode (HALT-HOLD)
- Low Power Dissipation: 50mW(Typ)
- Single + 3 to + 6 V Power Supply
- –40 to + 85°C, Operating Temperature
- Compatible with MSM80C85A
- 0.8 µs instruction Cycle (V_{CC} = 5V)
- On-Chip Clock Generator (with External Crystal)
- On-Chip System Controller; Advanced Cycle Status Information Available for Large System Control
- Bug operation in MSM80C85AH is fixed
- Four Vectored interrupt (One is non-maskable) Plus the 8080A-compatible interrupt.
- Serial, In/Serial Out Port
- Decimal, Binary and Double Precision Arithmetic
- Addressing Capability to 64K Bytes of Memory
- TTL Compatible
- 40-pin Plastic DIP(DIP40-P-600-2.54): (Product name: MSM80C85AHRS)
- 44-pin Plastic QFJ(QFJ44-P-S650-1.27): (Product name: MSM80C85AHJS)
- 44-pin Plastic QFP(QFP44-P-910-0.80-2K): (Product name: MSM80C85AHGS-2K)

FUNCTIONAL BLOCK DIAGRAM

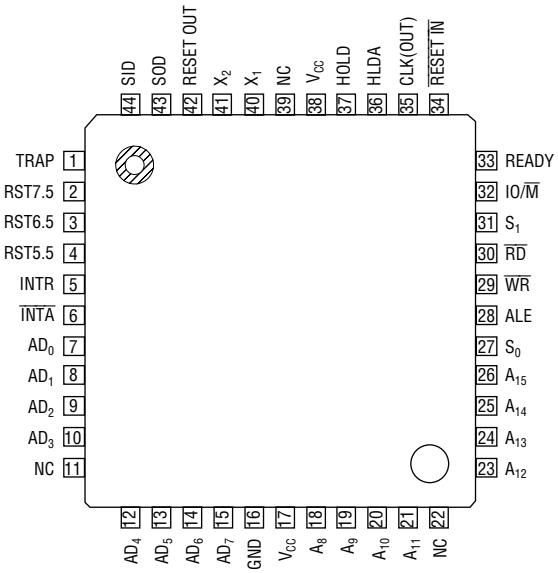


PIN CONFIGURATION (TOP VIEW)

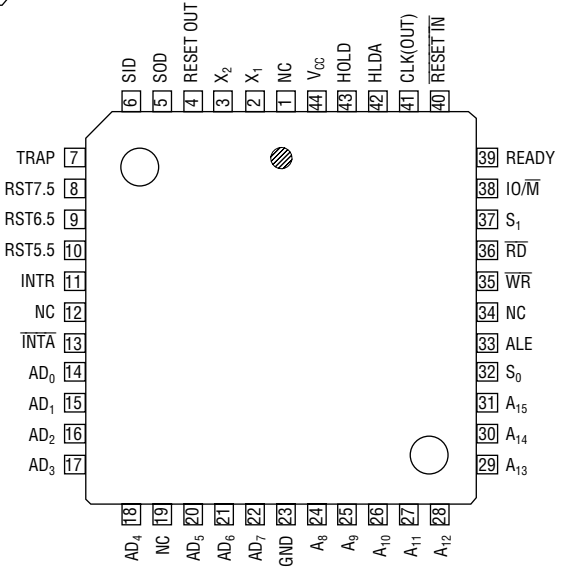
40 pin Plastic DIP



44 pin Plastic QFP



44 pin Plastic QFJ



MSM80C85AH FUNCTIONAL PIN DEFINITION

The following describes the function of each pin:

Symbol	Function
A_8 - A_{15} (Output, 3-state)	Address Bus: The most significant 8-bits of the memory address or the 8-bits of the I/O address, 3-stated during Hold and Halt modes and during RESET.
A_0 - A_7 (Input/Output) 3-state	Multiplexed Address/Data Bus: Lower 8-bits of the memory address (or I/O address) appear on the bus during the first clock cycle (T state) of a machine cycle. It then becomes the data bus during the second and third clock cycles.
ALE (Output)	Address Latch Enable: It occurs during the first clock state of a machine cycle and enables address to get latched into the on-chip latch peripherals. The falling edge of ALE is set to guarantee setup and hold times for the address information. The falling edge ALE can also be used to strobe the status information ALE is never 3-state.
S_0 , S_1 , IO/$\overline{M}$ (Output)	Machine cycle status: IO/$\overline{M}$ S_1 S_0 States 0 0 1 Memory write 0 1 0 Memory read 1 0 1 I/O write 1 1 0 I/O read 0 1 1 Opcode fetch IO/$\overline{M}$ S_1 S_0 States 1 1 1 Interrupt Acknowledge . 0 0 Halt = 3-state . × × Hold (high impedance) . × × Reset × = unspecified S_1 can be used as an advanced R/W status. IO/$\overline{M}$, S_0 and S_1 become valid at the beginning of a machine cycle and remain stable throughout the cycle. The falling edge of ALE may be used to latch the state of these lines.
$\overline{RD}$ (Output, 3-state)	READ control: A low level on $\overline{RD}$ indicates the selected memory or I/O device is to be read that the Data Bus is available for the data transfer, 3-stated during Hold and Halt modes and during RESET.
$\overline{WR}$ (Output, 3-state)	WRITE control: A low level on $\overline{WR}$ indicates the data on the Data Bus is to be written into the selected memory or I/O location. Data is set up at the trailing edge of $\overline{WR}$, 3-stated during Hold and Halt modes and during RESET.
READY (Input)	If READY is high during a read or write cycle, it indicates that the memory or peripheral is ready to send or receive data. If READY is low, the cpu will wait an integral number of clock cycles for READY to go high before completing the read or write cycle READY must conform to specified setup and hold times.
HOLD (Input)	HOLD indicates that another master is requesting the use of the address and data buses. The cpu, upon receiving the hold request, will relinquish the use of the bus as soon as the completion of the current bus transfer. Internal processing can continue. The processor can regain the bus only after the HOLD is removed. When the HOLD is acknowledged, the Address, Data, $\overline{RD}$, $\overline{WR}$, and IO/$\overline{M}$ lines are 3-stated. And status of power down is controlled by HOLD.
HLDA (Output)	HOLD ACKNOWLEDGE: Indicates that the cpu has received the HOLD request and that it will relinquish the bus in the next clock cycle. HLDA goes low after the Hold request is removed. The cpu takes the bus one half clock cycle after HLDA goes low.
INTR (Output)	INTERRUPT REQUEST: Is used as a general purpose interrupt. It is sampled on during the next to the last clock cycle of an instruction and during Hold and Halt states. If it is active, the Program Counter (PC) will be inhibited from incrementing and an $\overline{INTA}$ will be issued. During this cycle a RESTART or CALL instruction can be inserted to jump to the interrupt service routine. The INTR is enabled and disabled by software. It is disabled by Reset and immediately after an interrupt is accepted. Power down mode is reset by INTR.
$\overline{INTA}$ (Output)	INTERRUPT ACKNOWLEDGE: Is used instead of (and has the same timing as) $\overline{RD}$ during the instruction cycle after an INTR is accepted.
RST 5.5 RST 6.5 RST 7.5 (Input)	RESTART INTERRUPTS: These three inputs have the same timing as INTR except they cause an internal RESTART to be automatically inserted. The priority of these interrupts is ordered as shown in Table 1. These interrupts have a higher priority than INTR. In addition, they may be individually masked out using the SIM instruction. Power down mode is reset by these interrupts.
TRAP (Input)	Trap interrupt is a nonmaskable RESTART interrupt. It is recognized at the same timing as INTR or RST 5.5 - 7.5. It is unaffected by any mask or Interrupt Disable. It has the highest priority of any interrupt. (See Table 1.) Power down mode is reset by input of TRAP.

Symbol	Function
$\overline{\text{RESET IN}}$ (Input)	Sets the Program Counter to zero and resets the Interrupt Enable and HLDA flip-flops and release power down mode. The data and address buses and the control lines are 3-stated during RESET and because of the asynchronous nature of $\overline{\text{RESET IN}}$, the processor's internal registers and flags may be altered by RESET with unpredictable results. $\overline{\text{RESET IN}}$ is a Schmitt-triggered input, allowing connection to an R-C network for power-on RESET delay. The cpu is held in the reset condition as long as $\overline{\text{RESET IN}}$ is applied.
RESET OUT (Output)	Indicated cpu is being reset. Can be used as a system reset. The signal is synchronized to the processor clock and lasts an integral number of clock periods.
X_1, X_2 (Input)	X_1 and X_2 are connected to a crystal to drive the internal clock generator. X_1 can also be an external clock input from a logic gate. The input frequency is divided by 2 to give the processor's internal operating frequency.
CLK (Output)	Clock Output for use as a system clock. The period of CLK is twice the X_1, X_2 input period.
SID (Input)	Serial input data line. The data on this line is loaded into accumulator bit 7 whenever a RIM instruction is executed.
SOD (Output)	Serial output data line. The output SOD is set or reset as specified by the SIM instruction.
V_{CC}	+ 5 Volt supply
GND	Ground Reference.

Table 1 Interrupt Priority, Restart Address, and Sensitivity

Name	Priority	Address Branched To (1) When Interrupt Occurs	Type Trigger
TRAP	1	24H	Rising edge and high level unit sampled.
RST 7.5	2	3CH	Rising edge (latched).
RST 6.5	3	34H	High level unitl sampled.
RST 5.5	4	2CH	High level until sampled.
INTR	5	(2)	High level until sampled.

Notes: (1) The processor pushes the PC on the stack before branching to the indicated address.
(2) The address branched to depends on the instruction provided to the cpu when the interrupt is acknowledged.

FUNCTIONAL DESCRIPTION

The MSM80C85AH is a complete 8-bit parallel central processor. It is designed with silicon gate C-MOS technology and requires a single +5 volt supply. Its basic clock speed is 5 MHz, thus improving on the present MSM80C85A's performance with higher system speed and power down mode. Also it is designed to fit into a minimum system of two IC's: The CPU (MSM80C85AH), and a RAM/IO (MSM81C55-5)

The MSM80C85AH has twelve addressable 8-bit register pairs. Six others can be used interchangeably as 8-bit registers or 16-bit register pairs. The MSM80C85AH register set is as follows:

Mnemonic	Register	Contents
ACC or A	Accumulator	8-bits
PC	Program Counter	16-bit address
BC, DE, HL	General-Purpose Registers; data pointer (HL)	8-bit × 6 or 16-bits × 3
SP	Stack Pointer	16-bit address
Flags or F	Flag Register	5 flags (8-bit space)

The MSM80C85AH uses a multiplexed Data Bus. The address is spilt between the higher 8-bit Address Bus and the lower 8-bit Address/Data Bus. During the first T state (clock cycle) of a machine cycle the low order address is sent out on the Address/Data Bus. These lower 8-bits may be latched externally by the Address Latch Enable signal (ALE). During the rest of the machine cycle the data bus is used for mamory or I/O data.

The MSM80C85AH provides $\overline{RD}$, $\overline{WR}$, S_0, S_1, and IO/$\overline{M}$ signals for bus control. An Interrupt Acknowledge signal ($\overline{INTA}$) is also provided. Hold and all Interrupts are synchronized with the processor's internal clock. The MSM80C85AH also provides Serial Input Data (SID) and Serial Output Data (SOD) lines for a simple serial interface.
In addition to these features, the MSM80C85AH has three maskable, vector interrupt pins, one nonmaskable TRAP interrupt and power down mode with HALT and HOLD.

INTERRUPT AND SERIAL I/O

The MSM80C85AH has 5 interrupt inputs: INTR, RST 5.5 RST 6.5, RST 7.5, and TRAP. INTR is identical in function to the 8080A INT. Each of the three RESTART inputs, 5.5, 6.5, and 7.5, has a programmable mask. TRAP is also a RESTART interrupt but it is nonmaskable.

The three maskable interrupts cause the internal execution of RESTART (saving the program counter in the stack branching to the RESTART address) it the interrupts are enable and if the interrupt mask is not set. The nonmaskable TRAP causes the internal execution of a RESTART vector independent of the state of the interrupt enable or masks. (See Table 1.)

There are two different types of inputs in the restart interrupt. RST 5.5 and RST 6.5 are high level-sensitive like INTR (and INT on the 8080A) and are recognized with the same timing as INTR. RST 7.5 is rising edge-sensitive.

For RST 7.5, only a pulse is required to set an internal flip-flop which generates the internal interrupt request. The RST 7.5 request flip-flop remains set until the request is serviced. Then it is reset automatically, This flip-flop may also be reset by using the SIM instruction or by issuing a $\overline{\text{RESET IN}}$ to the MSM80C85AH. The RST 7.5 internal flip-flop will be set by a pulse on the RST 7.5 pin even when the RST 7.5 interrupt is masked out.

The interrupts are arranged in a flixed priority that determines which interrupt is to be recognized if more than one is pending, as follows: TRAP-highest priority, RST 7.5, RST 6.5, RST 5.5, INTR-lowest priority. This priority scheme does not take into account the priority of a routine that was started by a higher priority interrupt. RST 5.5 can interrupt an RST 7.5 routine if the interrupt are re-enabled before the end of the RST 7.5 routine.

The TRAP interrupt is useful for catastrophic evens such as power failure or bus error. The TRAP input is recognized just as any other interrupt but has the highest priority. It is not affected by any flag or mask. The TRAP input is both edge and level sensitive. The TRAP input must go high and remain high until it is acknowledged. It will not be recognized again until it goes low, then high again. This avoids any false triggering due to noise or logic glitches. Figure 3 illustrates the TRAP interrupt request circuitry within the MSM80C85AH. Note that the servicing of any interrupt (TRAP, RST 7.5, RST 6.5, RST 5.5,INTR) disables all future interrupts (except TRAPs) until an El instruction is executed.

The TRAP interrupt is special in that it disables interrupts, but preserves the previous interrupt enable status. Performing the first RIM instruction following a TRAP interrupt allows you to determine whether interrupts were enabled or disabled prior to the TRAP. All subsequent RIM instructions provide current interrupt enable status. Performing a RIM instruction following INTR or RST 5.5-7.5 will provide current interrupt Enable status, revealing that Interrupts are disabled.

The serial I/O system is also controlled by the RIM and SIM instructions. SID is read by RIM, and SIM sets the SOD data.

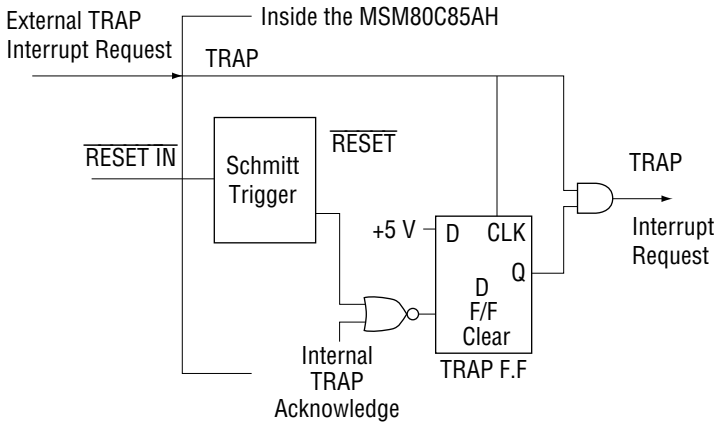


Figure 3 Trap and $\overline{\text{RESET IN}}$ Circuit

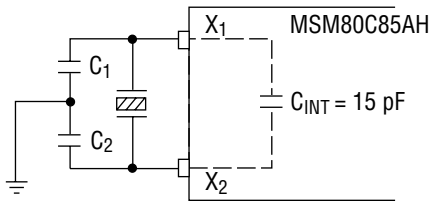
DRIVING THE X_1 AND X_2 INPUTS

You may drive the clock inputs of the MSM80C85AH with a crystal, or an external clock source. The driving frequency must be at least 1 MHz, and must be twice the desired internal clock frequency; hence, the MSM80C85AH is operated with a 6 MHz crystal (for 3 MHz clock). If a crystal is used, it must have the following characteristics:

Parallel resonance at twice the clock frequency desired
C_L (load capacitance) ≤ 30 pF
C_S (shunt capacitance) ≤ 7 pF
R_S (equivalent shunt resistance) ≤ 75 ohms
Drive level: 10 mW
Frequency tolerance: ±0.05% (suggested)

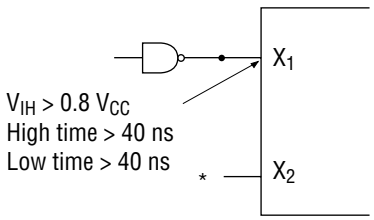
Note the use of the capacitors between X_1, X_2 and ground. These capacitors are required to assure oscillator startup at the correct frequency.
Figure 4 shows the recommended clock driver circuits. Note in B that a pull-up resistor is required to assure that the high level voltage of the input is at least 4 V.
For driving frequencies up to and including 6 MHz you may supply the driving signal to X, and leave X_2 open-circuited (Figure 4B). To prevent self-oscillation of the MSM80C85AH, be sure that X_2 is not coupled back to X_1 through the driving circuit.

A. Quartz Crystal Clock Driver



33 pF Capacitor required for crystal frequency 10 to 6.25 MHz
50 pF Capacitor required for crystal frequency 6.25 to 4 MHz
100 pF Capacitor required for crystal frequency <4 MHz

B. 1 - 10 MHz Input Frequency External Clock Drive Circuit



* X_2 Left Floating

Note: Since the constant values may vary depending on oscillator, consult the manufacturer of the oscillator used when designing a circuit.

Figure 4 Clock Driver Circuits

BASIC SYSTEM TIMING

The MSM80C85AH has a multiplexed Data Bus. ALE is used as a strobe to sample the lower 8-bits of address on the Data Bus. Figure 5 shows an instruction fetch, memory read and I/O write cycle (as would occur during processing of the OUT instruction). Note that during the I/O write and read cycle that the I/O port address is copied on both the upper and lower half of the address.

There are seven possible types of machine cycles. Which of these seven takes place is defined by the status of the three status lines ($IO/\overline{M}$, S_1, S_0) and the three control signals ($\overline{RD}$, $\overline{WR}$,and $\overline{INTA}$). (See Table 2.) The status line can be used as advanced controls (for device selection, for example), since they become active at the T_1 state, at the outset of each machine cycle. Control lines $\overline{RD}$ and $\overline{WR}$ become active later, at the time when the transfer of data is to take place, so are used as command lines.

A machine cycle normally consists of three T states, with the exception of OPCODE FETCH, which normally has either four or six T states (unless WAIT or HOLD states are forced by the receipt of $\overline{READY}$ or HOLD inputs). Any T state must be one of ten possible states, shown in Table 3.

Table 2 MSM80C85AH Machine Cycle Chart

Machine Cycle		Status			Control		
		$IO/\overline{M}$	S_1	S_0	$\overline{RD}$	$\overline{WR}$	$\overline{INTA}$
Opcode Fetch	(OF)	0	1	1	0	1	1
Memory Read	(MR)	0	1	0	0	1	1
Memory Write	(MW)	0	0	1	1	0	1
I/O Read	(IOR)	1	1	0	0	1	1
I/O Write	(IOW)	1	0	1	1	0	1
Acknowledge of INTR	(INA)	1	1	1	1	1	0
Bus Idle	(BI): DAD	0	1	0	1	1	1
	ACK. OF RST, TRAP	1	1	1	1	1	1
	HALT	TS	0	0	TS	TS	1

Table 3 MSM80C85AH Machine State Chart

Machine State	Status & Buses				Control		
	S_1, S_0	IO/$\overline{M}$	$A_8 - A_{15}$	$AD_0 - AD_7$	$\overline{RD}$, $\overline{WR}$	$\overline{INTA}$	$\overline{ALE}$
T_1	×	×	×	×	1	1	1 (1)
T_2	×	×	×	×	×	×	0
T_{WAIT}	×	×	×	×	×	×	0
T_3	×	×	×	×	×	×	0
T_4	1	0 (2)	×	TS	1	1	0
T_5	1	0 (2)	×	TS	1	1	0
T_6	1	0 (2)	×	TS	1	1	0
T_{RESET}	×	TS	TS	TS	TS	1	0
T_{HALT}	0	TS	TS	TS	TS	1	0
T_{HOLD}	×	TS	TS	TS	TS	1	0

0 = Logic "0"
1 = Logic "1"
TS = High Impedance
× = Unspecified

Notes: (1) ALE not generated during 2nd and 3rd machine cycles of DAD instruction.
(2) IO/$\overline{M}$ = 1 during T_4 - T_6 of INA machine cycle.

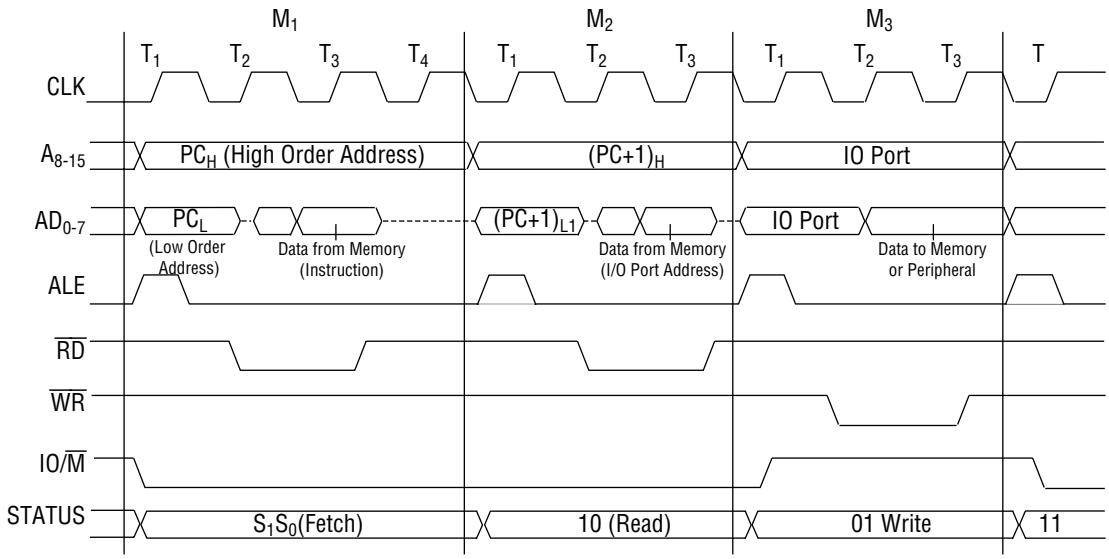


Figure 5 MSM80C85AH Basic System Timing

POWER DOWN Mode

The MSM80C85AH is compatible with the MSM80C85A in function and POWER DOWN mode. This reduces power consumption further.
There are two methods available for starting this POWER DOWN mode. One is through software control by using the HALT command and the other is under hardware control by using the pin HOLD. This mode is released by the HOLD, RESET, and interrupt pins (TRAP, RST7.5, RST6.5 RST5.5, or INTR). (See Table 4.)

Since the sequence of HALT, HOLD, RESET, and INTERRUPT is compatible with MSM80C85A, every the POWER DOWN mode can be used with no special attention.

Table 4 POWER DOWN Mode Releasing Method

Start by means of Halt command	Released by using pins RESET and INTERRUPT (not by pin HOLD)
Start by means of HOLD pin	Released by using RESET and HOLD pins (not by interrupt pins)

(1) Start by means of HALT command (See Figures 6 and 7.)

The POWER DOWN mode can be started by executing the HALT command.
At this time, the system is put into the HOLD status and therefore the POWER DOWN mode cannot be released even when the HOLD is released later.
In this case, the POWER DOWN mode can be released by means of the RESET or interrupt.

(2) Start by means of HOLD pin (See Figure 8.)

During the execution of commands other than the HALT, the POWER DOWN mode is started when the system is put into HOLD status by means of the HOLD pin.
Since no interrupt works during the execution of the HOLD, the POWER DOWN mode cannot be released by means of interrupt pins. In this case, the POWER DOWN mode can be released either by means of the RESET pin or by releasing the HOLD status by means of HOLD pin.

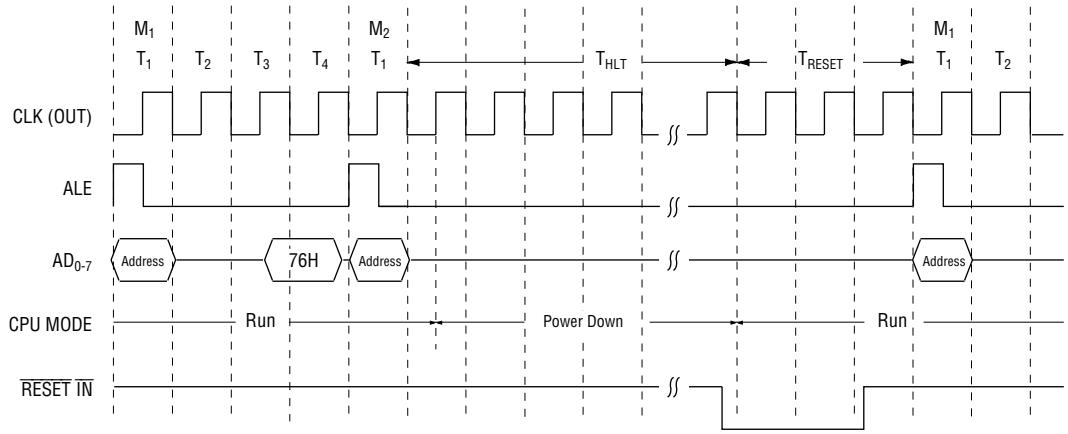


Figure 6 Started by HALT and Released by $\overline{\text{RESET IN}}$

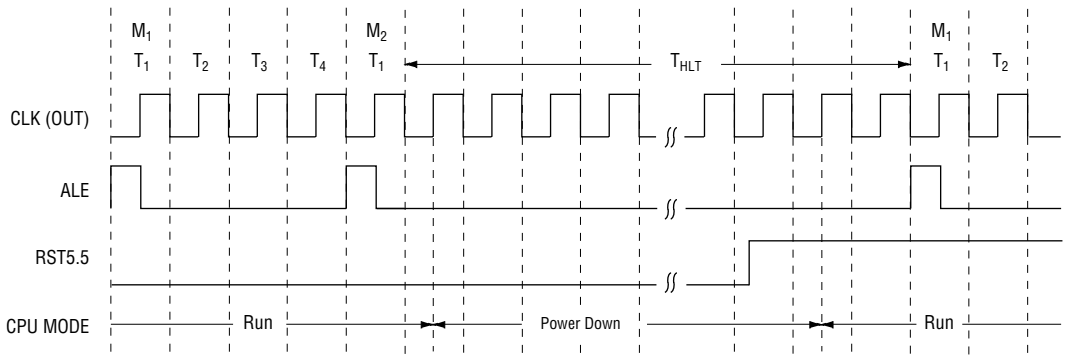


Figure 7 Started by HALT and Released by RST5.5

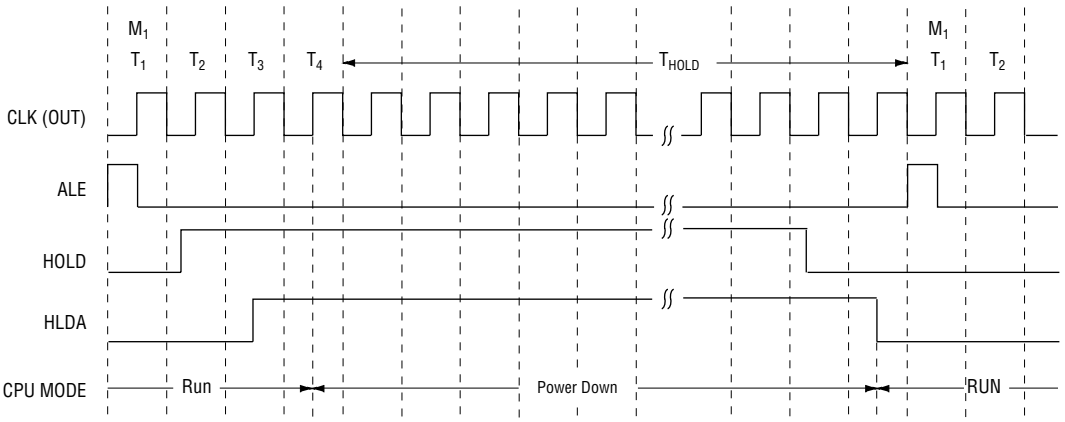


Figure 8 Started and Released by HOLD

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Limits			Units
			MSM80C85AHRS	MSM80C85AHGS	MSM80C85AHJS	
Power Supply Voltage	V_{CC}	With respect to GND	–0.5 - 7			V
Input Voltage	V_{IN}		–0.5 - V_{CC} +0.5			V
Output Voltage	V_{OUT}		–0.5 - V_{CC} +0.5			V
Storage Temperature	T_{STG}	—	–55 - +150			°C
Power Dissipation	P_D	Ta = 25°C	1.0	0.7	1.0	W

OPERATING RANGE

Parameter	Symbol	Limits	Unit
Power Supply Voltage	V_{CC}	3 - 6	V
Operating Temperature	T_{OP}	–40 - +85	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{CC}	4.5	5	5.5	V
Operating Temperature	T_{OP}	–40	+25	+85	°C
"L" Input Voltage	V_{IL}	–0.3	—	+0.8	V
"H" Output Voltage	V_{IH}	2.2	—	V_{CC} +0.3	V
"L" $\overline{\text{RESET IN}}$ Input Voltage	V_{ILR}	–0.3	—	+0.8	V
"H" $\overline{\text{RESET IN}}$ Input Voltage	V_{IHR}	3.0	—	V_{CC} +0.3	V

DC CHARACTERISTICS

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
"L" Output Voltage	V_{OL}	I_{OL} = 2.5 mA	V_{CC} = 4.5 V - 5.5 V, Ta = –40°C - +85°C	—	—	0.4	V
"H" Output Voltage	V_{OH}	I_{OH} = –2.5 mA		3.0	—	—	V
		I_{OH} = –100 µA		V_{CC} - 0.4	—	—	V
Input Leak Current	I_{LI}	$0 \le V_{IN} \le V_{CC}$		–10	—	10	µA
Output Leak Current	I_{LO}	$0 \le V_{OUT} \le V_{CC}$		–10	—	10	µA
Operating Supply Current	I_{CC}	T_{cyc} = 200 ns, C_L = 0 pF at reset		—	10	20	mA
		T_{cyc} = 200 ns, C_L = 0 pF at power down mode		—	5	10	mA

AC CHARACTERISTICS

(Ta = –40°C ~ 85°C, V_{CC} = 4.5 V ~ 5.5 V)

Parameter	Symbol	Condition	Min.	Max.	Unit
CLY Cycle Period	t_{CYC}		200	2000	ns
CLY Low Time	t_1		40	—	ns
CLY High Time	t_2		70	—	ns
CLY Rise and Fall Time	t_r, t_f		—	30	ns
X_1 Rising to CLK Rising	t_{XKR}		25	120	ns
X1 Rising to CKK Falling	t_{XKF}		30	150	ns
$A_{8\sim15}$ Valid to Leading Edge of Control (1)	t_{AC}		115	—	ns
$AD_{0\sim7}$ Valid to Leading Edge of Control	t_{ACL}		115	—	ns
$AD_{0\sim15}$ Valid Data in	t_{AD}		—	350	ns
Address Float After Leading Edge of $\overline{RD}$ $\overline{INTA}$	t_{AFR}		—	0	ns
$A_{8\sim15}$ Valid Before Trailing Edge of ALE (1)	t_{AL}		50	—	ns
$AD_{0\sim7}$ Valid Before Trailing Edge of ALE	t_{ALL}		50	—	ns
READY Valid from Address Valid	t_{ARY}		—	100	ns
Address ($A_{8\sim15}$) Valid After Control	t_{CA}		60	—	ns
Width of Control Law ($\overline{RD}$, $\overline{WR}$, $\overline{INTA}$)	t_{CC}		230	—	ns
Trailing Edge of Control to Leading Edges of ALE	t_{CL}		25	—	ns
Data Valid to Trailing Edge of $\overline{WR}$	t_{DW}		230	—	ns
HLDA to Bus Enable	t_{HABE}		—	150	ns
Bus Float After HLDA	t_{HABF}	t_{CYC}=200 ns	—	150	ns
HLDA Valid to Trailing Edge of CLK	t_{HACK}	CL=150 pF	40	—	ns
HOLD Hold Time	t_{HDH}		0	—	ns
HOLD Step Up Time to Trailing Edge of CLK	t_{HDS}		120	—	ns
INTR Hold Time	t_{INH}		0	—	ns
INTR, RST and TRAP Setup Time to Falling Edge of CLK	t_{INS}		150	—	ns
Address Hold Time After ALE	t_{LA}		50	—	ns
Trailing Edge of ALE to Leading Edge of Control	t_{LC}		60	—	ns
ALE Low During CLK High	t_{LCK}		50	—	ns
ALE to Valid Data During Read	t_{LDR}		—	270	ns
ALE to Valid Data During Write	t_{LDW}		—	140	ns
ALE Width	t_{LL}		80	—	ns
ALE to READY Stable	t_{LRY}		—	30	ns
Trailing Edge of $\overline{RD}$ to Re-enabling of Address	t_{RAE}		90	—	ns
RD (or INTA) to Valid Data	t_{RD}		—	150	ns
Control Trailing Edge to Leading Edge of Next Control	t_{RV}		220	—	ns
Data Hold Time After $\overline{RD}$ $\overline{INTA}$ (7)	t_{RDH}		0	—	ns
READY Hold Time	t_{RYH}		0	—	ns
READY Setup Time to Leading Edge of CLK	t_{RYS}		100	—	ns
Data Valid After Trailing Edge of $\overline{WR}$	t_{WD}		60	—	ns
LEADING Edge of $\overline{WR}$ to Data Vaild	t_{WDL}		—	20	ns

Notes: (1) A_8 - A_{15} address Specs apply to IO/$\overline{M}$, S_0 and S_1.
(2) Test condition: t_{CYC}=200 ns C_L=150 pF
(3) For all output timing where C_L=150 pF use the following correction factors:
25 pF $\leq C_L <$ 150 pF : –0.10ns/pF
150 pF $< C_L \leq$ 200 pF : +0.30ns/pF
(4) Output timings are measured with purely capacitive load.
(5) All timings are measured to output voltage V_L=0.8 V, V_H=2.2 V, and 1.5 V with 10 ns rise and fall time on inputs.
(6) To calculate timing specifications at other values of t_{CYC} use Table 7.
(7) Data hold time is guaranteed under all loading conditions.

Input Waveform for A.C. Tests:

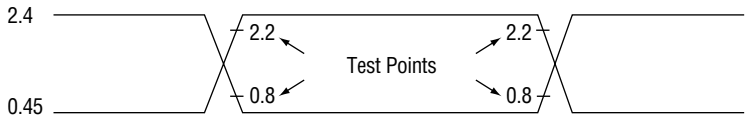


Table 7 Bus Timing Specification as a T_{CYC} Dependent

(Ta = -40°C - +85°C, V_{CC} = 4.5 V - 5.5 V, C_L = 150 pF)

	MSM80C85AH		
t_{AL}	—	(1/2)T - 50	Min
t_{LA}	—	(1/2)T - 50	Min
t_{LL}	—	(1/2)T - 20	Min
t_{LCK}	—	(1/2)T - 50	Min
t_{LC}	—	(1/2)T - 40	Min
t_{AD}	—	(5/2+N)T - 150	Max
t_{RD}	—	(3/2+N)T - 150	Max
t_{RAE}	—	(1/2)T - 10	Min
t_{CA}	—	(1/2)T - 40	Min
t_{DW}	—	(3/2+N)T -70	Min
t_{WD}	—	(1/2)T - 40	Min
t_{CC}	—	(3/2+N)T - 70	Min
t_{CL}	—	(1/2)T - 75	Min
t_{ARY}	—	(3/2)T - 200	Max
t_{HACK}	—	(1/2)T - 60	Min
t_{HABF}	—	(1/2)T + 50	Max
t_{HABE}	—	(1/2)T + 50	Max
t_{AC}	—	(2/2)T - 85	Min
t_1	—	(1/2)T - 60	Min
t_2	—	(1/2)T - 30	Min
t_{RV}	—	(3/2)T - 80	Min
t_{LDR}	—	(2+N)T -130	Max

Note: N is equal to the total WAIT states.
T = t_{CYC}

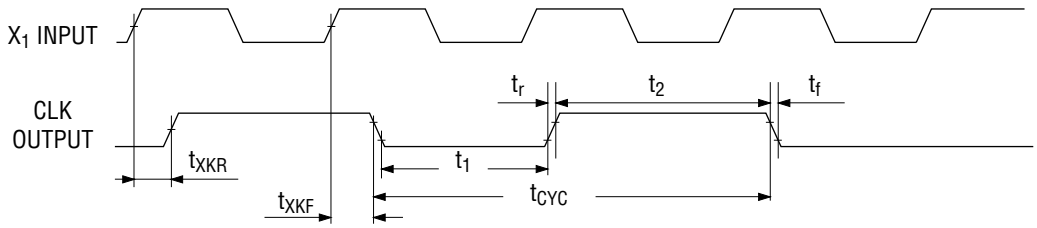
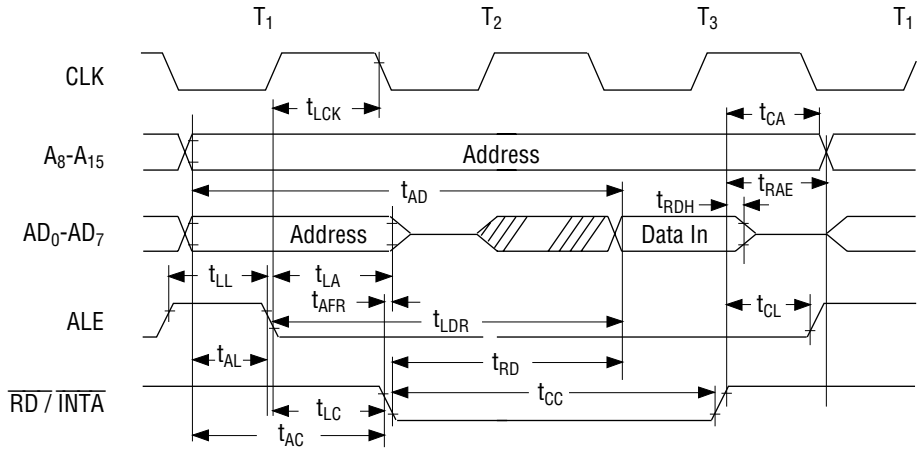
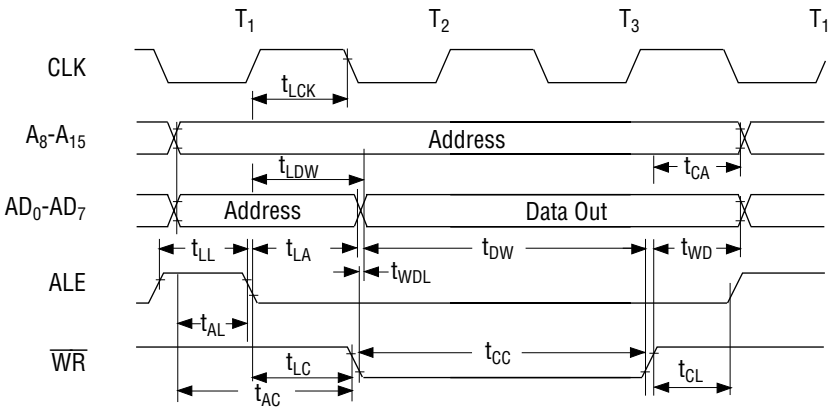


Figure 6 Clock Timing Waveform

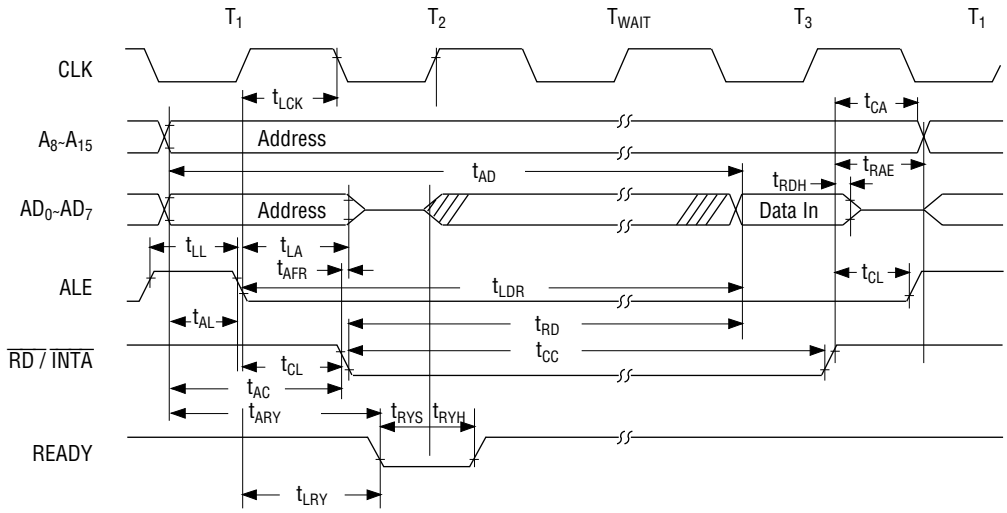
READ OPERATION



WRITE OPERATION



Read operation with Wait Cycle (Typical)–
same READY timing applies to WRITE operation



Note: READY must remain stable during setup and hold times.

Figure 7 MSM80C85AH Bus Timing, With and Without Wait

HOLD OPERATION

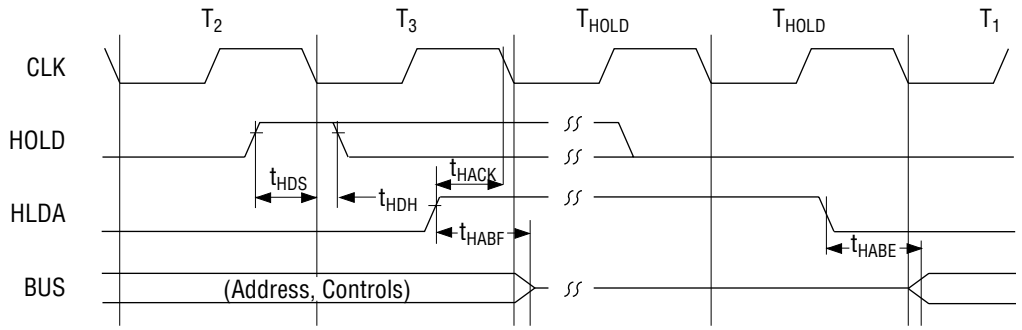
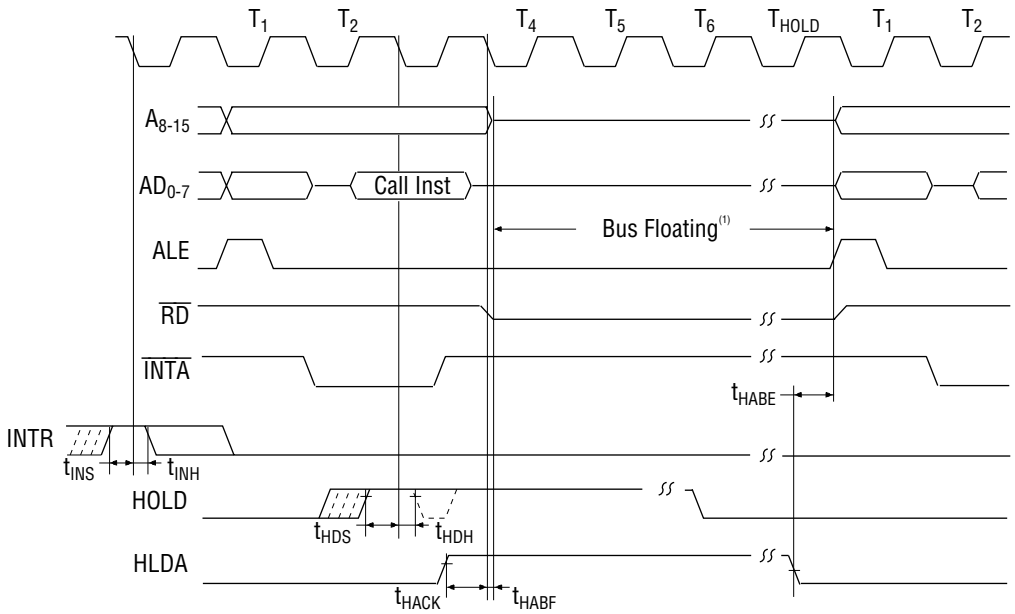


Figure 8 MSM80C85AH Hold Timing



NOTE: (1) IO/$\overline{M}$ is also floating during this time.

Figure 9 MSM80C85AH Interrupt and Hold Timing

Table 8 Instruction Set Summary

Mnemonic	Description	Instruction Code (1) D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Clock (2) Cycles
MOVE, LOAD, AND STORE										
MOVr1 r2	Move register to register	0	1	D	D	D	S	S	S	4
MOV M r	Move register to memory	0	1	1	1	0	S	S	S	7
MOV r M	Move memory to register	0	1	D	D	D	1	1	0	7
MVI r	Move immediate register	0	0	D	D	D	1	1	0	7
MVI M	Move immediate memory	0	0	1	1	0	1	1	0	10
LXI B	Load immediate register Pair B & C	0	0	0	0	0	0	0	1	10
LXI D	Load immediate register Pair D & E	0	0	0	1	0	0	0	1	10
LXI H	Load immediate register Pair H & L	0	0	1	0	0	0	0	1	10
LXI SP	Load immediate stack pointer	0	0	1	1	0	0	0	1	10
STAX B	Store A indirect	0	0	0	0	0	0	1	0	7
STAX D	Store A indirect	0	0	0	1	0	0	1	0	7
LDAX B	Load A indirect	0	0	0	0	1	0	1	0	7
LDAX D	Load A indirect	0	0	0	1	1	0	1	0	7
STA	Store A direct	0	0	1	1	0	0	1	0	13
LDA	Load A direct	0	0	1	1	1	0	1	0	13
SHLD	Store H & L direct	0	0	1	0	0	0	1	0	16
LHLD	Load H & L direct	0	0	1	0	1	0	1	0	16
XCHG	Exchange D & E H & L registers	1	1	1	0	1	0	1	1	4
STACK OPS										
PUSH B	Push register Pair B & C on stack	1	1	0	0	0	1	0	1	12
PUSH D	Push register Pair D & E on stack	1	1	0	1	0	1	0	1	12
PUSH H	Push register Pair H & L on stack	1	1	1	0	0	1	0	1	12
PUSH PSW	Push A and Flags on stack	1	1	1	1	0	1	0	1	12
POP B	Pop register Pair B & C off stack	1	1	0	0	0	0	0	1	10
POP D	Pop register Pair D & E off stack	1	1	0	1	0	0	0	1	10
POP H	Pop register Pair H & L off stack	1	1	1	0	0	0	0	1	10
POP PSW	Pop A and Flags off stack	1	1	1	1	0	0	0	1	10
XTHL	Exchange top of stack H & L	1	1	1	0	0	0	1	1	16
SPHL	H & L to stack pointer	1	1	1	1	1	0	0	1	6
JUMP										
JMP	Jump unconditional	1	1	0	0	0	0	1	1	10
JC	Jump on carry	1	1	0	1	1	0	1	0	7/10
JNC	Jump on no carry	1	1	0	1	0	0	1	0	7/10
JZ	Jump on zero	1	1	0	0	1	0	1	0	7/10
JNZ	Jump on no zero	1	1	0	0	0	0	1	0	7/10
JP	Jump on positive	1	1	1	1	0	0	1	0	7/10
JM	Jump on minus	1	1	1	1	1	0	1	0	7/10
JPE	Jump on parity even	1	1	1	0	1	0	1	0	7/10
JPO	Jump on parity odd	1	1	1	0	0	0	1	0	7/10
PCHL	H & L to program counter	1	1	1	0	1	0	0	1	6
CALL										
CALL	Call unconditional	1	1	0	0	1	1	0	1	18
CC	Call on carry	1	1	0	1	1	1	0	0	9/18
CNC	Call on no carry	1	1	0	1	0	1	0	0	9/18
CZ	Call on zero	1	1	0	0	1	1	0	0	9/18
CNZ	Call on no zero	1	1	0	0	0	1	0	0	9/18
CP	Call on positive	1	1	1	1	0	1	0	0	9/18
CM	Call on minus	1	1	1	1	1	1	0	0	9/18
CPE	Call on parity even	1	1	1	0	1	1	0	0	9/18
CPO	Call on parity odd	1	1	1	0	0	1	0	0	9/18

Table 8 Instruction Set Summary cont'd

Mnemonic	Description	Instruction Code (1) D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Clock (2) Cycles
RETURN										
RET	Return	1	1	0	0	1	0	0	1	10
RC	Return on carry	1	1	0	1	1	0	0	0	6/12
RNC	Return on no carry	1	1	0	1	0	0	0	0	6/12
RZ	Return on zero	1	1	0	0	1	0	0	0	6/12
RNZ	Return on no zero	1	1	0	0	0	0	0	0	6/12
RP	Return on positive	1	1	1	1	0	0	0	0	6/12
RM	Return on minus	1	1	1	1	1	0	0	0	6/12
RPE	Return on parity even	1	1	1	0	1	0	0	0	6/12
RPO	Return on parity odd	1	1	1	0	0	0	0	0	6/12
RESTART										
RST	Restart	1	1	A	A	A	1	1	1	12
INPUT/OUTPUT										
IN	Input	1	1	0	1	1	0	1	1	10
OUT	Output	1	1	0	1	0	0	1	1	10
INCREMENT AND DECREMENT										
INR r	Increment register	0	0	D	D	D	1	0	0	4
DCR r	Decrement register	0	0	D	D	D	1	0	1	4
INR M	Increment memory	0	0	1	1	0	1	0	0	10
DCR M	Decrement memory	0	0	1	1	0	1	0	1	10
INX B	Increment B & C registers	0	0	0	0	0	0	1	1	6
INX D	Increment D & E registers	0	0	0	1	0	0	1	1	6
INX H	Increment H & L registers	0	0	1	0	0	0	1	1	6
INX SP	Increment stack pointer	0	0	1	1	0	0	1	1	6
DCX B	Decrement B & C	0	0	0	0	1	0	1	1	6
DCX D	Decrement D & E	0	0	0	1	1	0	1	1	6
DCX H	Decrement H & L	0	0	1	0	1	0	1	1	6
DCX SP	Decrement stack pointer	0	0	1	1	1	0	1	1	6
ADD										
ADD r	Add register to A	1	0	0	0	0	S	S	S	4
ADC r	Add register to A with carry	1	0	0	0	1	S	S	S	4
ADD M	Add memory to A	1	0	0	0	0	1	1	0	7
ADC M	Add memory to A with carry	1	0	0	0	1	1	1	0	7
ADI	Add immediate to A	1	1	0	0	0	1	1	0	7
ACI	Add immediate to A with carry	1	1	0	0	1	1	1	0	7
DAD B	Add B & C to H & L	0	0	0	0	1	0	0	1	10
DAD D	Add D & E to H & L	0	0	0	1	1	0	0	1	10
DAD H	Add H & L to H & L	0	0	1	0	1	0	0	1	10
DAD SP	Add stack pointer to H & L	0	0	1	1	1	0	0	1	10
SUBTRACT										
SUB r	Subtract register from A	1	0	0	1	0	S	S	S	4
SBB r	Subtract register from A with borrow	1	0	0	1	1	S	S	S	4
SUB M	Subtract memory from A	1	0	0	1	0	1	1	0	7
SBB M	Subtract memory from A with borrow	1	0	0	1	1	1	1	0	7
SUI	Subtract immediate from A	1	1	0	1	0	1	1	0	7
SBI	Subtract immediate from A with borrow	1	1	0	1	1	1	1	0	7

Table 8 Instruction Set Summary cont'd

Mnemonic	Description	Instruction Code (1) D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Clock (2) Cycles
LOGICAL										
ANA r	Add register with A	1	0	1	0	0	S	S	S	4
XRA r	Exclusive Or register with A	1	0	1	0	1	S	S	S	4
ORA r	Or register with A	1	0	1	1	0	S	S	S	4
CMP r	Compare register with A	1	0	1	1	1	S	S	S	4
ANA M	And memory with A	1	0	1	0	0	1	1	0	7
XRA M	Exclusive Or Memory with A	1	0	1	0	1	1	1	0	7
ORA M	Or memory with A	1	0	1	1	0	1	1	0	7
CMP M	Compare memory with A	1	0	1	1	1	1	1	0	7
ANI	And immediate with A	1	1	1	0	0	1	1	0	7
XRI	Exclusive Or immediate with A	1	1	1	0	1	1	1	0	7
ORI	Or immediate with A	1	1	1	1	0	1	1	0	7
CPI	Compare immediate with A	1	1	1	1	1	1	1	0	7
ROTATE										
RLC	Rotate A left	0	0	0	0	0	1	1	1	4
RRC	Rotate A right	0	0	0	0	1	1	1	1	4
RAL	Rotate A left through carry	0	0	0	1	0	1	1	1	4
RAR	Rotate A right through carry	0	0	0	1	1	1	1	1	4
SPECIALS										
CMA	Complement A	0	0	1	0	1	1	1	1	4
STC	Set carry	0	0	1	1	0	1	1	1	4
CMC	Complement carry	0	0	1	1	1	1	1	1	4
DAA	Decimal adjust A	0	0	1	0	0	1	1	1	4
CONTROL										
EI	Enable Interrupts	1	1	1	1	1	0	1	1	4
DI	Disable Interrupts	1	1	1	1	0	0	1	1	4
NOP	No-operation	0	0	0	0	0	0	0	0	4
HLT	Halt (Power down)	0	1	1	1	0	1	1	0	5
RIM	Read Interrupt Mask	0	0	1	0	0	0	0	0	4
SIM	Set Interrupt Mask	0	0	1	1	0	0	0	0	4

Notes: (1) DDD or SSS. B 000. C 001. D 010. E 011. H 100. L 101. Memory 110. A 111.
(2) Two possible cycle times, (6/12) indicate instruction cycles dependent on condition flags.

Precautions for operation

(1) When the oscillation circuit is to be used, keep the RES input low until the oscillation is sufficiently stabilized after power is turned on.
(2) When power is turned on, the output level (SOD etc.) is unknown before the equipment is reset.
(3) Bug of MSM80C85A–2 at power down has fixed.
(4) Because Spike Noise would be output on HLDA, RESET OUT and CLK pins, depending on the customers condition of usage; please take into account this issue at System Board design.

SUPPLEMENTARY EXPLANATION

(1) SIM instruction: The execution of the SIM instruction uses the contents of the accumulator to mask MSM80C85AH'S interrupts.

Accumulator Setting Value

Bit 7	6	5	4	3	2	1	0
—	—	—	R7.5	MSE	M7.5	M6.5	M5.5

R7.5 (Reset interrupt 7.5 Flip-flop): When this bit is set to 1, the edge detecting flip-flop of RST 7.5 interrupt is reset.
MSE (Mask Set Enable): When this bit is set to 1, the interrupt mask bits are valid.
M7.5 (Mask RST7.5): When this bit is set to 1 and MSE bit is set to 1, RST7.5 interrupt is masked.
M6.5 (Mask RST6.5): When this bit is set to 1 and MSE bit is set to 1, RST6.5 interrupt is masked.
M5.5 (Mask RST5.5): When this bit is set to 1 and MSE bit is set to 1, RST 5.5 interrupt is masked.

(2) RIM instruction: When the contents of the accumulator are read out after RIM instruction has been executed, MSM80C85AH interrupt status can be known.

Accumulator Reading Value

Bit 7	6	5	4	3	2	1	0
—	17.5	16.5	15.5	IE	M7.5	M6.5	M5.5

17.5 (Pending RST7.5): When RST7.5 interrupt is pending, "1" is read out.
16.5 (Pending RST6.5): When RST6.5 interrupt is pending, "1" is read out.
15.5 (Pending RST5.5): When RST5.5 interrupt is pending, "1" is read out.
IE (Interrupt Enable Flag): When interrupt is Enable, "1" is read out.
M7.5 (Mask RST7.5): When RST7.5 interrupt is masked, "1" is read out.
M6.5 (Mask RST6.5): When RST6.5 interrupt is masked, "1" is read out.
M5.5 (Mask RST5.5): When RST5.5 interrupt is masked ,"1" is read out.

NOTICE ON REPLACING LOW-SPEED DEVICES WITH HIGH-SPEED DEVICES

The conventional low speed devices are replaced by high-speed devices as shown below.
When you want to replace your low speed devices with high-speed devices, read the replacement notice given on the next pages.

High-speed device (New)	Low-speed device (Old)	Remarks
M80C85AH	M80C85A/M80C85A-2	8bit MPU
M80C86A-10	M80C86A/M80C86A-2	16bit MPU
M80C88A-10	M80C88A/M80C88A-2	8bit MPU
M82C84A-2	M82C84A/M82C84A-5	Clock generator
M81C55-5	M81C55	RAM.I/O, timer
M82C37B-5	M82C37A/M82C37A-5	DMA controller
M82C51A-2	M82C51A	USART
M82C53-2	M82C53-5	Timer
M82C55A-2	M82C55A-5	PPI

Differences between MSM80C85AH and MSM80C85A/MSM80C85A-2

1) Manufacturing Process

Item	MSM80C85A	MSM80C85A-2	MSM80C85AH
Manufacturing Process	3μSi-CMOS	2.5μSi-CMOS	2μSi-CMOS

2) Functions

Item	MSM80C85A	MSM80C85A-2	MSM80C85AH
Power-down Function	Not provided	Provided (but may malfunction when HOLD is used)	Provided (The malfunction has been removed.)
Address output during T4 to T6 cycles	Undefined (compatible with Intel devices)	Not fixed	The contents of data in T3 cycle are retained (for low power consumption).

3) Electrical Characteristics
3-1) Operating Conditions

Parameter	Symbol	MSM80C85A	MSM80C85A-2	MSM80C85AH
Power Supply Voltage	V_{CC}	4 to 6 V	3 to 6 V	3 to 6 V

3-2) DC Characteristics

Parameter	Symbol	MSM80C85A	MSM80C85A-2	MSM80C85AH
''L''Level Output Voltage	V_{OL}	0.45 V maximum (+2 mA)	0.45 V maximum (+2 mA)	0.40 V maximum (+2.5 mA)
''H''Level Output Voltage	V_{OH}	2.4 V minimum (-400 μA)	2.4 V minimum (-400 μA)	3.0 V maximum (-2.5 mA)
''H''Level Output Voltage	V_{OH}	4.2 V minimum (-40 μA)	4.2 V minimum (-40 μA)	V_{CC}-0.2 V minimum (-100 μA)
Supply Current (at RES)	I_{CC}	22 mA maximum (@3 MHz)	20 mA maximum (@5 MHz)	20 mA maximum (@5 MHz)
Supply Current (in PD)	I_{CC}	None	7 mA maximum (@5 MHz)	10 mA maximum (@5 MHz)

Notes: "at RES" means "at reset time" and "in PD" means "in power down mode".

As shown above, the V_{OL} and V_{OH} ranges the MSM80C85AH contain those of the MSM80C85A/MSM80C85A-2. Although the supply current range (at a power failure) of the MSM80C85AH does not contain that of the MSM80C85A-2, this does not affect the actual use of the MSM80C85AH.

3-3) AC Characteristics

The AC characteristics (5 MHz) of the MSM80C85AH satisfy that (3 MHz) of the MSM80C85A. The MSM80C85AH also satisfies that (5MHz) of the MSM80C85A.

AC Charasteristics

Symbol		MSM80C85A	MSM80C85A-2	MSM80C85AH
t_{CYC}	Min	*320 ns*	200 ns	200 ns
t_1	Min	*80 ns*	40 ns	40 ns
t_2	Min	*120 ns*	70 ns	70 ns
t_{XKR}	Min	*30 ns*	25 ns	25 ns
t_{AC}	Max	*270 ns*	115 ns	115 ns
t_{ACL}	Min	*240 ns*	115 ns	115 ns
t_{AD}	Max	*575 ns*	330 ns	350 ns
t_{AL}	Min	*115 ns*	50 ns	50 ns
t_{ALL}	Min	*90 ns*	50 ns	50 ns
t_{ARY}	Max	*220 ns*	100 ns	100 ns
t_{CA}	Min	*120 ns*	60 ns	60 ns
t_{CC}	Min	*400 ns*	230 ns	230 ns
t_{CL}	Min	*50 ns*	25 ns	25 ns
t_{DW}	Min	*420 ns*	230 ns	230 ns
t_{HABE}	Min	*210 ns*	150 ns	150 ns
t_{HABF}	Max	*210 ns*	150 ns	150 ns
t_{HACK}	Min	*110 ns*	40 ns	40 ns
t_{HDS}	Min	*170 ns*	120 ns	120 ns
t_{INS}	Min	*160 ns*	150 ns	150 ns
t_{LA}	Min	*100 ns*	50 ns	50 ns
t_{LC}	Min	*130 ns*	60 ns	60 ns
t_{LCK}	Min	*100 ns*	50 ns	50 ns
t_{LDR}	Max	*460 ns*	250 ns	270 ns
t_{LDW}	Max	*200 ns*	140 ns	140 ns
t_{LL}	Min	*140 ns*	80 ns	80 ns
t_{LRY}	Max	*110 ns*	30 ns	30 ns
t_{RAE}	Min	*150 ns*	90 ns	90 ns
t_{RD}	Max	*300 ns*	150 ns	150 ns
t_{RV}	Min	*400 ns*	220 ns	220 ns
t_{WD}	Min	*100 ns*	60 ns	60 ns
t_{WDL}	Max	*40 ns*	20 ns	20 ns

Notes: The italicized or underlined values indicate that they are different from those of the MSM80C85AH.

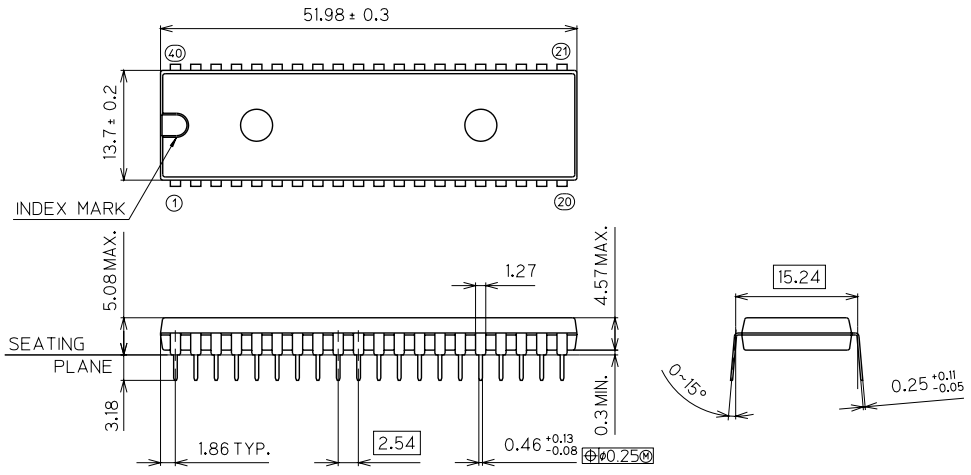
4) Other notes

1) As the MSM80C85AH employs the 2 µ process, its noise characteristics may be a little different from those of the MSM80C85A. When devices are replaced for upgrading, it is recommended to perform noise evaluation. Especially, HLDA, RESOUT, and CLKOUT pins must be evaluated.
2) The MSM80C85AH basically satisfies the characteristics of the MSM80C85A-2 and the MSM80C85A, but their timings are a little different, Therefore, when critical timing is required in designing, it is recommended to evaluate operating margins at various temperatures and voltages.

PACKAGE DIMENSIONS

(Unit : mm)

DIP40-P-600-2.54



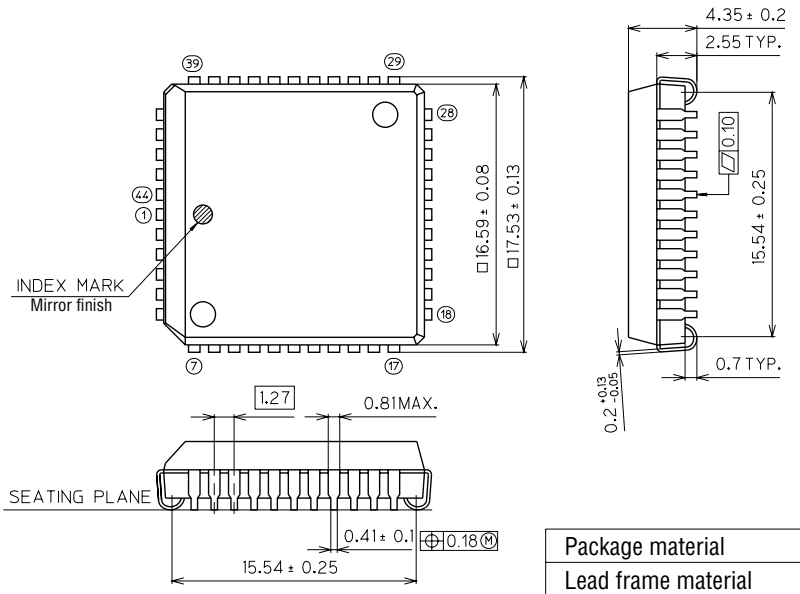
Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	6.10 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

(Unit : mm)

QFJ44-P-S650-1.27



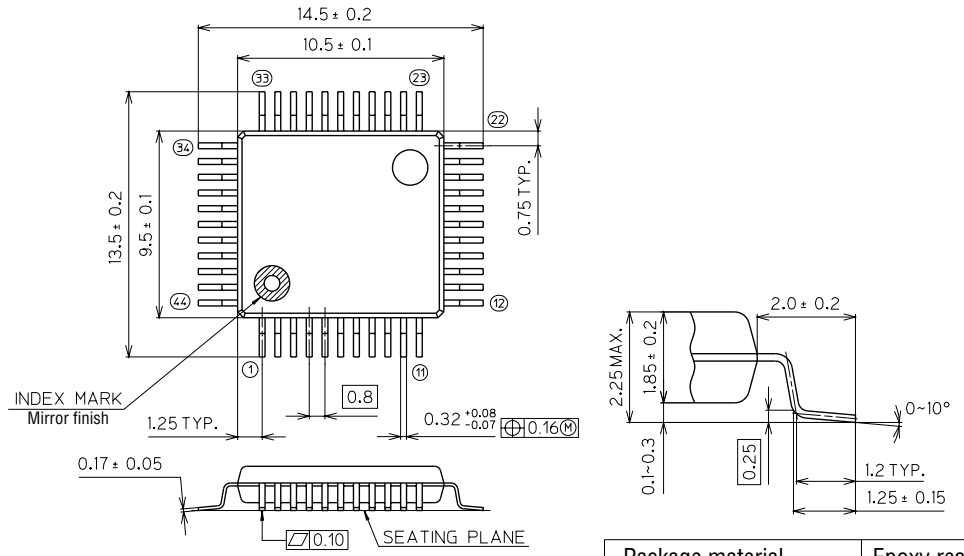
Package material	Epoxy resin
Lead frame material	Cu alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	2.00 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

(Unit : mm)

QFP44-P-910-0.80-2K



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	0.41 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).