

SINGLE-CHANNEL
6N135, 6N136
HCPL-2503
HCPL-4502

DUAL-CHANNEL
HCPL-2530
HCPL-2531

DESCRIPTION

The HCPL-4502/HCPL-2503, 6N135/6 and HCPL-2530/HCPL-2531 optocouplers consist of an AlGaAs LED optically coupled to a high speed photodetector transistor.

A separate connection for the bias of the photodiode improves the speed by several orders of magnitude over conventional phototransistor optocouplers by reducing the base-collector capacitance of the input transistor.

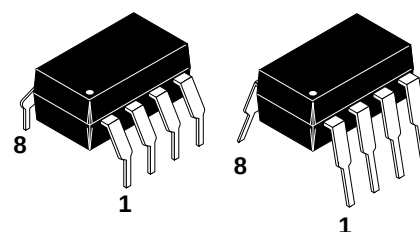
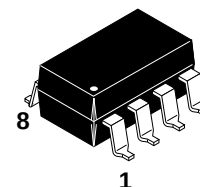
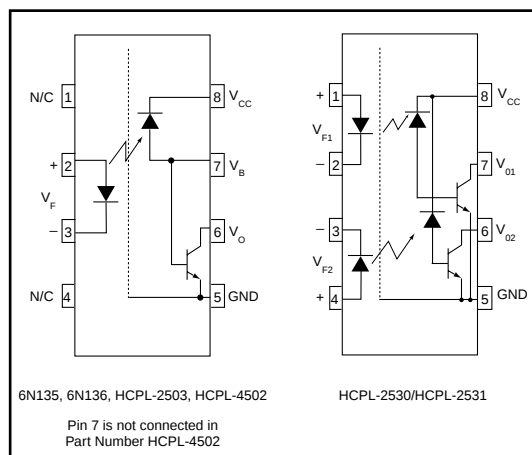
An internal noise shield provides superior common mode rejection of 10kV/μs. An improved package allows superior insulation permitting a 480 V working voltage compared to industry standard of 220 V.

FEATURES

- High speed-1 Mbit/s
- Superior CMR-10 kV/μs
- Dual-Channel
HCPL-2530/HCPL-2531
- Double working voltage-480V RMS
- CTR guaranteed 0-70°C
- U.L. recognized (File # E90700)

APPLICATIONS

- Line receivers
- Pulse transformer replacement
- Output interface to CMOS-LSTTL-TTL
- Wide bandwidth analog coupling



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise specified)

Parameter	Symbol	Value	Units
Storage Temperature	T _{STG}	-55 to +125	°C
Operating Temperature	T _{OPR}	-55 to +100	°C
Lead Solder Temperature	T _{SOL}	260 for 10 sec	°C
EMITTER			
DC/Average Forward Input Current Each Channel (Note 1)	I _F (avg)	25	mA
Peak Forward Input Current (50% duty cycle, 1 ms P.W.) Each Channel (Note 2)	I _F (pk)	50	mA
Peak Transient Input Current - (≤ 1 μs P.W., 300 pps) Each Channel	I _F (trans)	1.0	A
Reverse Input Voltage Each Channel	V _R	5	V
Input Power Dissipation (6N135/6N136 and HCPL-2503/4502) Each Channel (Note 3)	P _D	100	mW
		45	
DETECTOR			
Average Output Current Each Channel	I _O (avg)	8	mA
Peak Output Current Each Channel	I _O (pk)	16	mA
Emitter-Base Reverse Voltage (6N135, 6N136 and HCPL-2503 only)	V _{EBR}	5	V
Supply Voltage	V _{CC}	-0.5 to 30	V
Output Voltage	V _O	-0.5 to 20	V
Base Current (6N135, 6N136 and HCPL-2503 only)	I _B	5	mA
Output power (6N135, 6N136, HCPL-2503, HCPL-4502) (Note 4)	P _D	100	mW
dissipation (HCPL-2530, HCPL-2531) Each Channel		35	mW

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ELECTRICAL CHARACTERISTICS ($T_A = 0$ to 70°C Unless otherwise specified)

INDIVIDUAL COMPONENT CHARACTERISTICS

Parameter	Test Conditions	Symbol	Device	Min	Typ**	Max	Unit
EMITTER							
	($I_F = 16\text{ mA}$, $T_A = 25^\circ\text{C}$)	V_F			1.45	1.7	V
Input Forward Voltage	($I_F = 16\text{ mA}$)					1.8	
Input Reverse Breakdown Voltage	($I_R = 10\text{ }\mu\text{A}$)	B_{VR}		5.0			V
Temperature coefficient of forward voltage	($I_F = 16\text{ mA}$)	$(\Delta V_F / \Delta T_A)$			-1.6		mV/ $^\circ\text{C}$
DETECTOR							
Logic high output current	($I_F = 0\text{ mA}$, $V_O = V_{CC} = 5.5\text{ V}$) ($T_A = 25^\circ\text{C}$)	I_{OH}	All		0.001	0.5	μA
	($I_F = 0\text{ mA}$, $V_O = V_{CC} = 15\text{ V}$) ($T_A = 25^\circ\text{C}$)		6N135 6N136 HCPL-4502 HCPL-2503		0.005	1	
	($I_F = 0\text{ mA}$, $V_O = V_{CC} = 15\text{ V}$)		All			50	
Logic low supply current	($I_F = 16\text{ mA}$, $V_O = \text{Open}$) ($V_{CC} = 15\text{ V}$)	I_{CCL}	6N135 6N136 HCPL-4502 HCPL-2503		120	200	μA
	($I_{F1} = I_{F2} = 16\text{ mA}$, $V_O = \text{Open}$) ($V_{CC} = 15\text{ V}$)		HCPL-2530 HCPL-2531		200	400	
Logic high supply current	($I_F = 0\text{ mA}$, $V_O = \text{Open}$, $V_{CC} = 15\text{ V}$) ($T_A = 25^\circ\text{C}$)	I_{CCH}	6N135 6N136 HCPL-4502 HCPL-2503			1	μA
	($I_F = 0\text{ mA}$, $V_O = \text{Open}$) ($V_{CC} = 15\text{ V}$)		6N135 6N136 HCPL-4502 HCPL-2503			2	
	($I_F = 0\text{ mA}$, $V_O = \text{Open}$) ($V_{CC} = 15\text{ V}$)		HCPL-2530 HCPL-2531		0.02	4	

** All typicals at $T_A = 25^\circ\text{C}$

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TRANSFER CHARACTERISTICS (T_A = 0 to 70°C Unless otherwise specified)

Parameter	Test Conditions	Symbol	Device	Min	Typ**	Max	Unit
COUPLED	Current transfer ratio (Note 5)	CTR	6N135 HCPL-2530	7	18	50	%
			6N136 HCPL-4502 HCPL-2531	19	27	50	%
			HCPL-2503	12	27		%
			6N135 HCPL-2530	5	21		%
			6N136 HCPL-4502 HCPL-2531	15	30		%
			HCPL-2503	9	30		%
Logic low output voltage output voltage	(I _F = 16 mA, I _O = 1.1 mA) (V _{CC} = 4.5 V, T _A =25°C)	V _{OL}	6N135 HCPL-2530		0.18 0.18	0.4 0.5	V
			6N136 HCPL-4502 HCPL-2503		0.25	0.4	
			HCPL-2531		0.25	0.5	
			6N135 HCPL-2530			0.5	
			6N136 HCPL-4502 HCPL-2503 HCPL-2531			0.5	

** All typicals at T_A = 25°C

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SWITCHING CHARACTERISTICS ($T_A = 0$ to 70°C unless otherwise specified., $V_{CC} = 5\text{ V}$)

Parameter	Test Conditions	Symbol	Device	Min	Typ**	Max	Unit
Propagation delay time to logic low	$T_A = 25^\circ\text{C}$, ($R_L = 4.1\text{ k}\Omega$, $I_F = 16\text{ mA}$) (Note 6) (Fig. 7)	T_{PHL}	6N135 HCPL-2530		0.45	1.5	μs
	$(R_L = 1.9\text{ k}\Omega$, $I_F = 16\text{ mA}$) (Note 7) (Fig. 7) $T_A = 25^\circ\text{C}$		6N136 HCPL-4502 HCPL-2503 HCPL-2531		0.45	0.8	μs
	$(R_L = 4.1\text{ k}\Omega$, $I_F = 16\text{ mA}$) (Note 6) (Fig. 7)		6N135 HCPL-2530			2.0	μs
	$(R_L = 1.9\text{ k}\Omega$, $I_F = 16\text{ mA}$) (Note 7) (Fig. 7)		6N136 HCPL-4502 HCPL-2503 HCPL-2531			1.0	μs
Propagation delay time to logic high	$T_A = 25^\circ\text{C}$, ($R_L = 4.1\text{ k}\Omega$, $I_F = 16\text{ mA}$) (Note 6) (Fig. 7)	T_{PLH}	6N135 HCPL-2530		0.5	1.5	μs
	$(R_L = 1.9\text{ k}\Omega$, $I_F = 16\text{ mA}$) (Note 7) (Fig. 7) $T_A = 25^\circ\text{C}$		6N136 HCPL-4502 HCPL-2503 HCPL-2531		0.3	0.8	μs
	$(R_L = 4.1\text{ k}\Omega$, $I_F = 16\text{ mA}$) (Note 6) (Fig. 7)		6N135 HCPL-2530			2.0	μs
	$(R_L = 1.9\text{ k}\Omega$, $I_F = 16\text{ mA}$) (Note 7) (Fig. 7)		6N136 HCPL-4502 HCPL-2503 HCPL-2531			1.0	μs
Common mode transient immunity at logic high	$(I_F = 0\text{ mA}$, $V_{CM} = 10\text{ V}_{P-P}$, $R_L = 4.1\text{ k}\Omega$) (Note 8) (Fig. 8) $T_A = 25^\circ\text{C}$	$ CM_H $	6N135 HCPL-2530		10,000		$\text{V}/\mu\text{s}$
	$(I_F = 0\text{ mA}$, $V_{CM} = 10\text{ V}_{P-P}$) $T_A = 25^\circ\text{C}$, ($R_L = 1.9\text{ k}\Omega$) (Note 8) (Fig. 8)		6N136 HCPL-4502 HCPL-2503 HCPL-2531		10,000		$\text{V}/\mu\text{s}$
Common mode transient immunity at logic low	$(I_F = 16\text{ mA}$, $V_{CM} = 10\text{ V}_{P-P}$, $R_L = 4.1\text{ k}\Omega$) (Note 8) (Fig. 8) $T_A = 25^\circ\text{C}$	$ CM_L $	6N135 HCPL-2530		10,000		$\text{V}/\mu\text{s}$
	$(I_F = 16\text{ mA}$, $V_{CM} = 10\text{ V}_{P-P}$) ($R_L = 1.9\text{ k}\Omega$) (Note 8) (Fig. 8)		6N136 HCPL-4502 HCPL-2503 HCPL-2531		10,000		$\text{V}/\mu\text{s}$

** All typicals at $T_A = 25^\circ\text{C}$

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ISOLATION CHARACTERISTICS (T_A = 0 to 70°C Unless otherwise specified)

Characteristics	Test Conditions	Symbol	Min	Typ**	Max	Unit
Input-output insulation leakage current	(Relative humidity = 45%) (T _A = 25°C, t = 5 s) (V _{I-O} = 3000 VDC) (Note 9)	I _{I-O}			1.0	μA
Withstand insulation test voltage	(RH ≤ 50%, T _A = 25°C) (Note 9) (t = 1 min.)	V _{ISO}	2500			V _{RMS}
Resistance (input to output)	(Note 9) (V _{I-O} = 500 VDC)	R _{I-O}		10 ¹²		Ω
Capacitance (input to output)	(Note 9) (f = 1 MHz)	C _{I-O}		0.6		pF
DC Current gain	(I _O = 3 mA, V _O = 5 V)	HFE		150		
Input-Input Insulation leakage current	(RH ≤ 45%, V _{I-I} = 500 VDC) (Note 10) t = 5 s, (HCPL-2530/2531 only)	I _{I-I}		0.005		μA
Input-Input Resistance	(V _{I-I} = 500 VDC) (Note 10) (HCPL-2530/2531 only)	R _{I-I}		10 ¹¹		Ω
Input-Input Capacitance	(f = 1 MHz) (Note 10) (HCPL-2530/2531 only)	C _{I-I}		0.03		pF

** All typicals at T_A = 25°C

NOTES

- Derate linearly above 70°C free-air temperature at a rate of 0.8 mA/°C.
- Derate linearly above 70°C free-air temperature at a rate of 1.6 mA/°C.
- Derate linearly above 70°C free-air temperature at a rate of 0.9 mW/°C.
- Derate linearly above 70°C free-air temperature at a rate of 2.0 mW/°C.
- Current Transfer Ratio is defined as a ratio of output collector current, I_O, to the forward LED input current, I_F, times 100%.
- The 4.1 kΩ load represents 1 LSTTL unit load of 0.36 mA and 6.1kΩ pull-up resistor.
- The 1.9 kΩ load represents 1 TTL unit load of 1.6 mA and 5.6 kΩ pull-up resistor.
- Common mode transient immunity in logic high level is the maximum tolerable (positive) dV_{cm}/dt on the leading edge of the common mode pulse signal V_{CM}, to assure that the output will remain in a logic high state (i.e., V_O > 2.0 V). Common mode transient immunity in logic low level is the maximum tolerable (negative) dV_{cm}/dt on the trailing edge of the common mode pulse signal, V_{CM}, to assure that the output will remain in a logic low state (i.e., V_O < 0.8 V).
- Device is considered a two terminal device: Pins 1, 2, 3 and 4 are shorted together and Pins 5, 6, 7 and 8 are shorted together.
- Measured between pins 1 and 2 shorted together, and pins 3 and 4 shorted together.

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Fig. 1 Normalized CTR vs. Forward Current

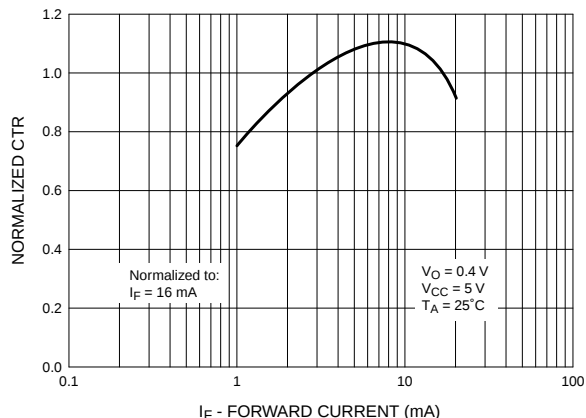


Fig. 2 Normalized CTR vs. Temperature

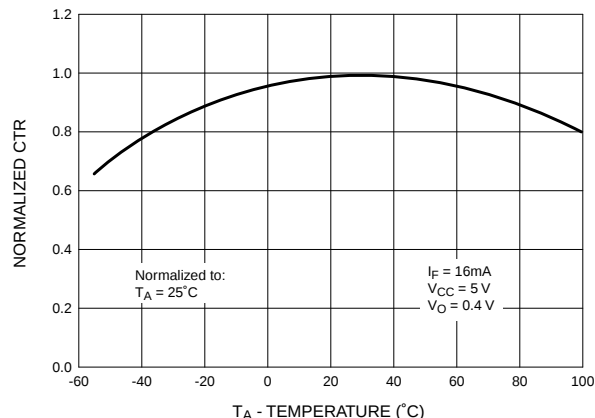


Fig. 3 Output Current vs. Output Voltage

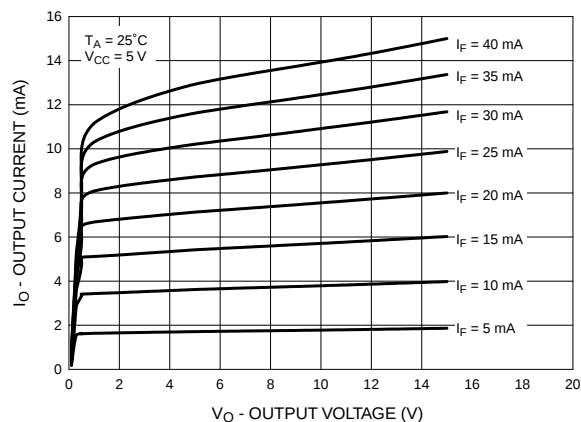


Fig. 4 Logic High Output Current vs. Temperature

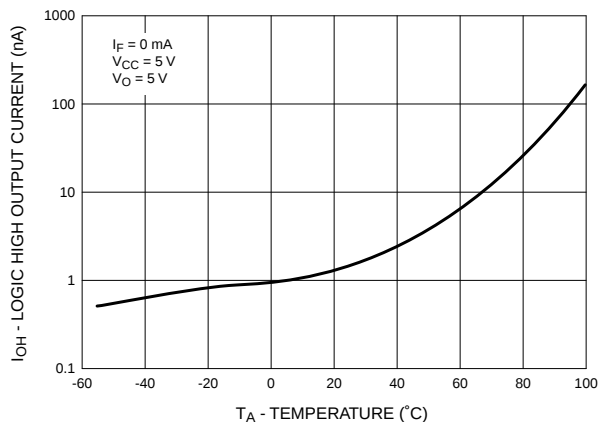


Fig. 5 Propagation Delay vs. Temperature

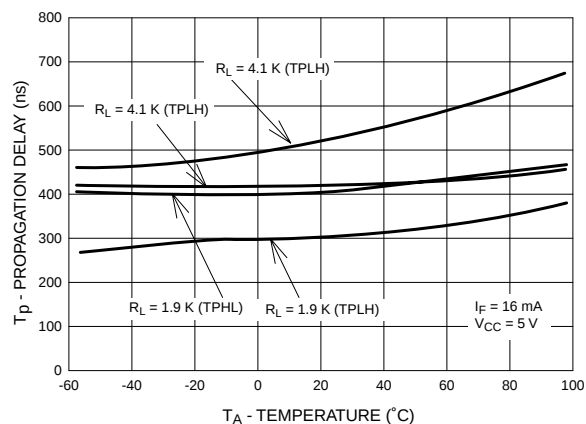
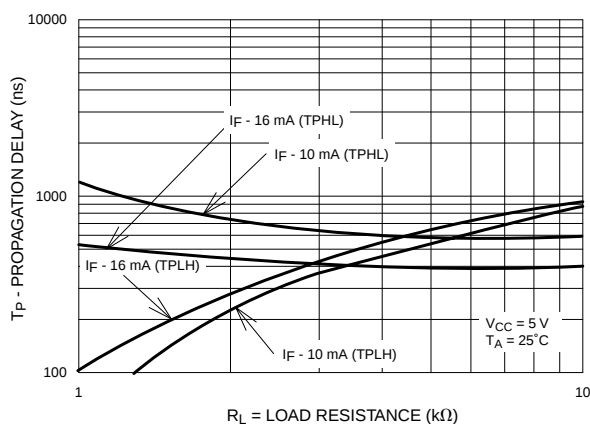
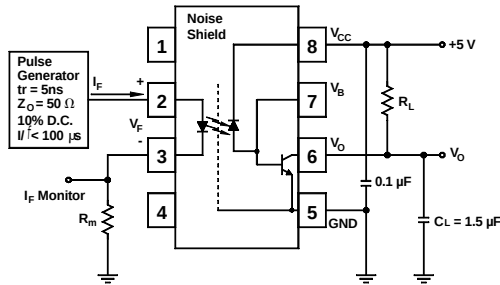


Fig. 6 Propagation Delay vs. Load Resistance

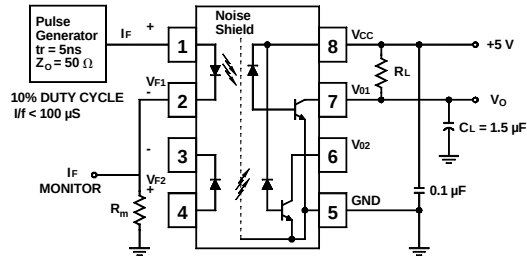


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Test Circuit for 6N135, 6N136, HCPL-2503 and HCPL-4502



Test Circuit for HCPL-2530 and HCPL-2531

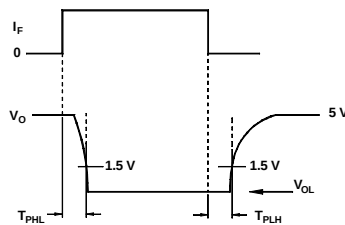
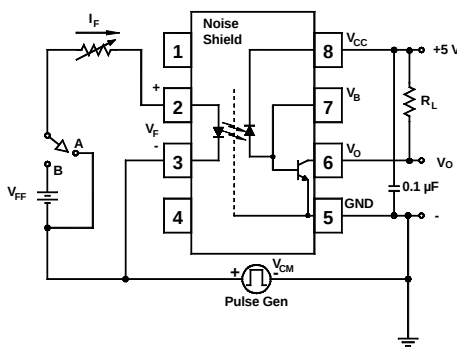
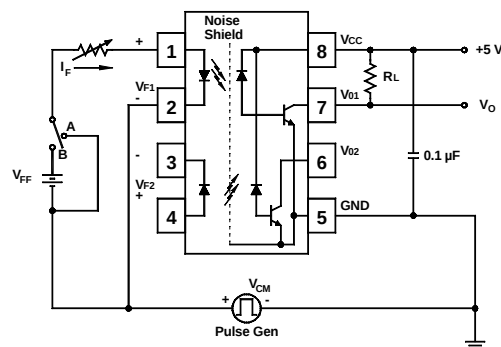


Fig. 7 Switching Time Test Circuit



Test Circuit for 6N135, 6N136, HCPL-2503 and HCPL-4502



Test Circuit for HCPL-2530 and HCPL-2531

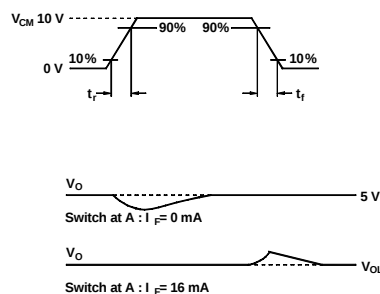
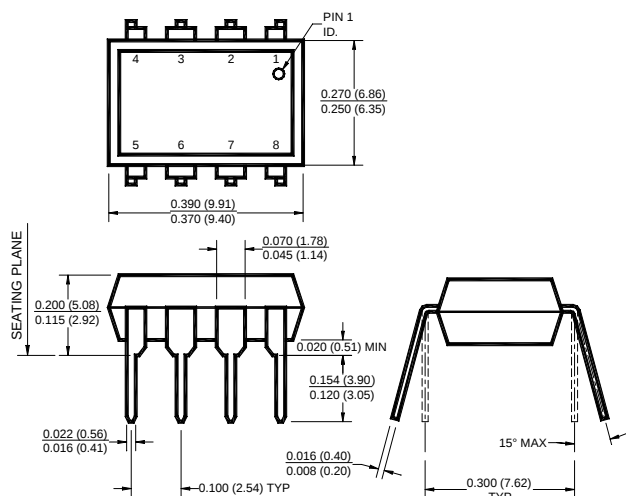


Fig. 8 Common Mode Immunity Test Circuit

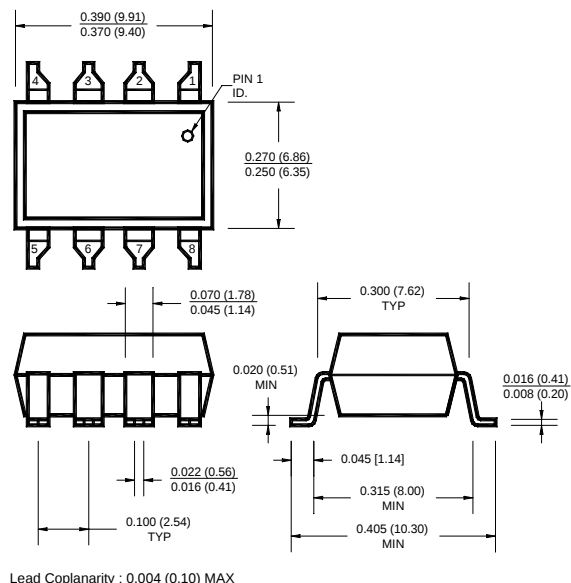
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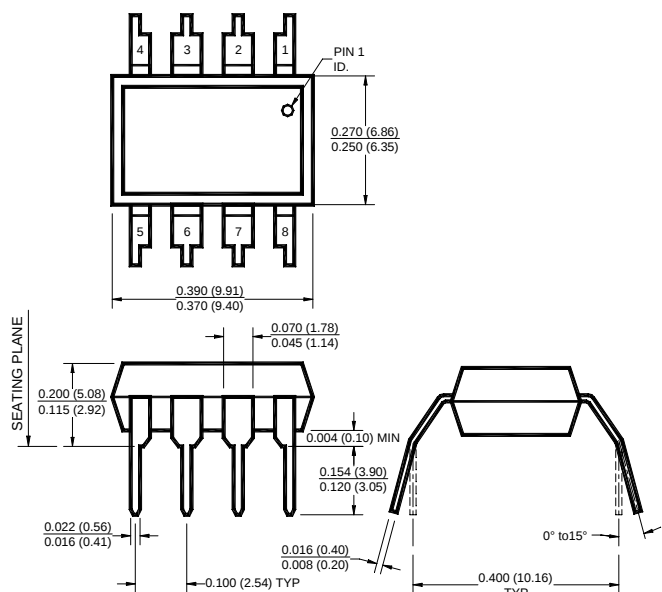
Package Dimensions (Through Hole)



Package Dimensions (Surface Mount)



Package Dimensions (0.4" Lead Spacing)



NOTE

All dimensions are in inches (millimeters)

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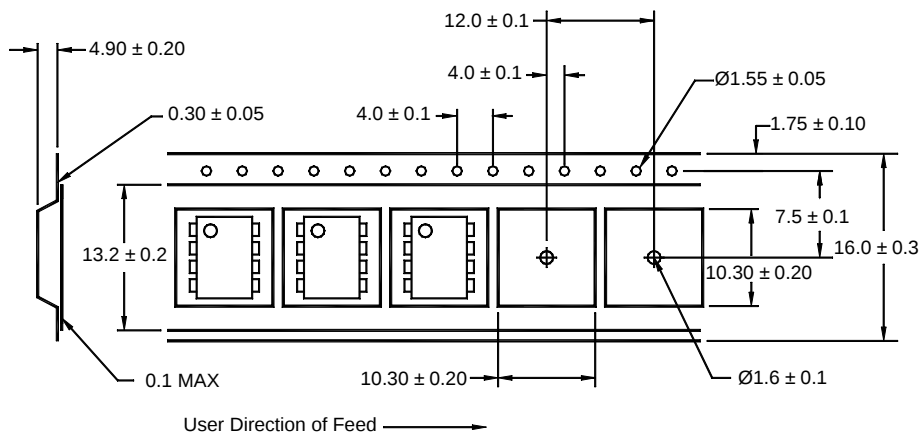
ORDERING INFORMATION

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Option	Order Entry Identifier	Description
R2	.R2	Opto Plus Reliability Conditioning
S	.S	Surface Mount Lead Bend
SD	.SD	Surface Mount; Tape and reel
SDL	.SDL	Surface Mount; Tape and reel
W	.W	0.4" Lead Spacing

QT Carrier Tape Specifications ("D" Taping Orientation)



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