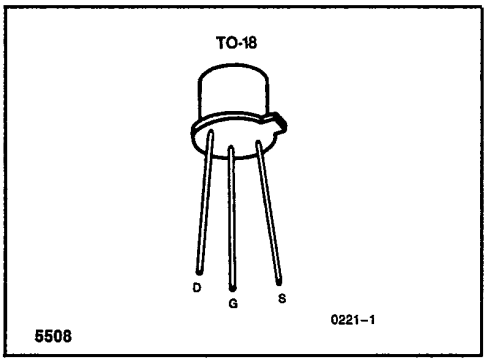
T-37-25

2N5018, 2N5019
P-Channel JFET Switch

FEATURES
- Low Insertion Loss
- No Offset or Error Voltages Generated By Closed Switch
- Purely Resistive

APPLICATIONS
- Analog Switches
- Commutators
- Choppers

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS
(T_A = 25°C unless otherwise noted)

Gate-Drain or Gate-Source Voltage 30V
Gate Current 50mA
Storage Temperature Range ..... −65°C to +200°C
Operating Temperature Range ..... −55°C to +200°C
Lead Temperature (Soldering, 10sec) ..... +300°C
Power Dissipation 500mW
Derate above 25°C ..... 3mW/°C

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

ORDERING INFORMATION*

TO-18
2N5018
2N5019

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions		2N5018		2N5019		Units
				Min	Max	Min	Max	
BV_{GSS}	Gate-Source Breakdown Voltage	I_G = 1μA, V_{DS} = 0		30		30		V
I_{GSS}	Gate Reverse Current	V_{GS} = 15V, V_{DS} = 0			2		2	nA
$I_{D(off)}$	Drain Cutoff Current	V_{DS} = −15V, V_{GS} = 12V (2N5018) V_{GS} = 7V (2N5019)			−10		−10	nA
			T_A = 150°C		−10		−10	μA
I_{DGO}	Drain Reverse Current	V_{DG} = −15V, I_S = 0			−2		−2	nA
			T_A = 150°C		−3		−3	μA
$V_{GS(off)}$	Gate-Source Cutoff Voltage	V_{DS} = −15V, I_D = −1μA			10		5	V
I_{DSS}	Saturation Drain Current	V_{DS} = −20V, V_{GS} = 0		−10		−5		mA
$V_{DS(on)}$	Drain-Source ON Voltage	V_{GS} = 0, I_D = −6mA (2N5018), I_D = −3mA (2N5019)			−0.5		−0.5	V
$r_{ds(on)}$	Static Drain-Source ON Resistance	I_D = −1mA, V_{GS} = 0			75		150	Ω
$r_{ds(on)}$	Drain-Source ON Resistance	I_D = 0, V_{GS} = 0	f = 1kHz		75		150	Ω
C_{iss}	Common-Source Input Capacitance (Note 1)	V_{DS} = −15V, V_{GS} = 0	f = 1MHz		45		45	pF
C_{rss}	Common-Source Reserve Transfer Capacitance (Note 1)	V_{DS} = 0, V_{GS} = 12V (2N5018), V_{GS} = 7V (2N5019)			10		10	pF

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NOTE: All typical values have been characterized but are not tested.

2N5018, 2N5019

INTERSIL

T-37-25

ELECTRICAL CHARACTERISTICS (Continued)(T_A = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions				2N5018		2N5019		Units
						Min	Max	Min	Max	
$t_{d(on)}$	Turn-ON Delay Time (Note 1)	V_{DD} = −6V, $V_{GS(on)}$ = 0					15		15	ns
t_r	Rise Time (Note 1)		$V_{GS(off)}$	$I_{D(on)}$	R_L		20		75	
$t_{d(off)}$	Turn-off Delay Time (Note 1)	2N5018	12V	−6mA	910Ω		15		25	
t_f	Fall Time (Note 1)	2N5019	7V	−3mA	1.8kΩ		50		100	

NOTES: 1. For design reference only, not 100% tested.

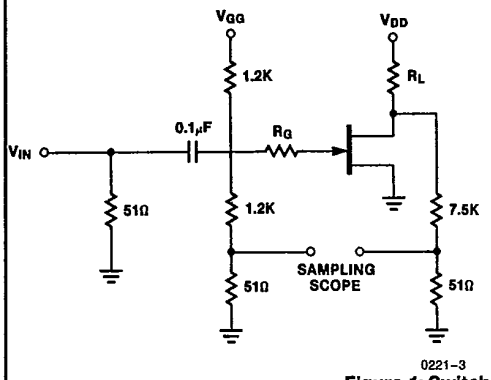

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Figure 1: Switching Time Text Circuit

INPUT PULSE
RISE TIME < 1ns
FALL TIME < 1ns
PULSE WIDTH 100ns
REPLETION RATE 1MHz

SAMPLING SCOPE
RISE TIME 0.4ns
INPUT RESISTANCE 10MΩ
INPUT CAPACITANCE 1.5pF

NOTE: All typical values have been characterized but are not tested.