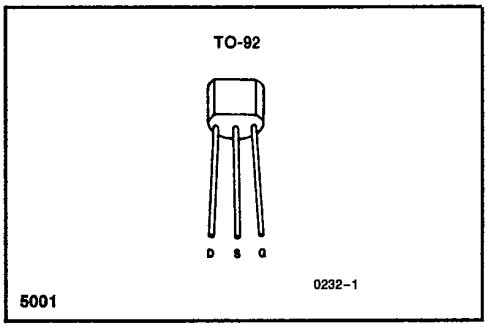
T-35-25

2N5638-2N5640

2N5638-2N5640
N-Channel JFET Switch

FEATURES
- Economy Packaging
- Fast Switching
- Low Drain-Source 'ON' Resistance

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS
(T_A = 25°C unless otherwise specified)

Drain-Source Voltage	30V
Drain-Gate Voltage	30V
Source-Gate Voltage	30V
Forward Gate Current	10mA
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−55°C to +135°C
Lead Temperature (Soldering, 10sec)	+300°C
Power Dissipation	310mW
Derate above 25°C	2.82mW/°C

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

ORDERING INFORMATION

TO-92
2N5638
2N5639
2N5640

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	2N5638		2N5639		2N5640		Units
			Min	Max	Min	Max	Min	Max	
BV_{GSS}	Gate Reverse Breakdown Voltage	I_G = −10μA, V_{DS} = 0	−30		−30		−30		V
I_{GSS}	Gate Reverse Current	V_{GS} = −15V, V_{DS} = 0		−1.0		−1.0		−1.0	nA
		T_A = 100°C		−1.0		−1.0		−1.0	μA
$I_{D(off)}$	Drain Cutoff Current	V_{DS} = 15V, V_{GS} = −12V (2N5638), V_{GS} = −8V (2N5639), V_{GS} = −6V (2N5640)		1.0		1.0		1.0	nA
		T_A = 100°C		1.0		1.0		1.0	μA
I_{DSS}	Saturation Drain Current	V_{DS} = 20V, V_{GS} = 0 (Note 1)	50		25		5.0		mA
$V_{DS(on)}$	Drain-Source ON Voltage	V_{GS} = 0, I_D = 12mA (2N5638), I_D = 6mA (2N5639), I_D = 3mA (2N5640)		0.5		0.5		0.5	V
$r_{DS(on)}$	Static Drain-Source ON Resistance	I_D = 1mA, V_{GS} = 0		30		60		100	Ω
$r_{ds(on)}$	Drain-Source ON Resistance	V_{GS} = 0, I_D = 0, f = 1kHz		30		60		100	Ω
C_{iss}	Common-Source Input Capacitance (Note 2)	V_{GS} = −12V, V_{DS} = 0, f = 1MHz		10		10		10	pF
C_{rss}	Common-Source Reverse Transfer Capacitance (Note 2)			4.0		4.0		4.0	pF
$t_{d(on)}$	Turn-On Delay Time (Note 2)	V_{DD} = 10V, $V_{GS(on)}$ = 0, $V_{GS(off)}$ = −10V, R_G = 50Ω (Note 2)		4.0		6.0		8.0	ns
t_r	Rise Time (Note 2)	$I_{D(on)}$ = 12mA (2N5638)		5.0		8.0		10	ns
t_d	Turn-OFF Delay Time (Note 2)	$I_{D(on)}$ = 6mA (2N5639)		5.0		10		15	ns
t_f	Fall Time (Note 2)	$I_{D(on)}$ = 3mA (2N5640)		10		20		30	ns

NOTES: 1. Pulse test; PW ≤ 300μs, duty cycle ≤ 3.0%.
2. For design reference only, not 100% tested.

NOTE: All typical values have been characterized but are not tested.

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INTERSIL

T-35-25

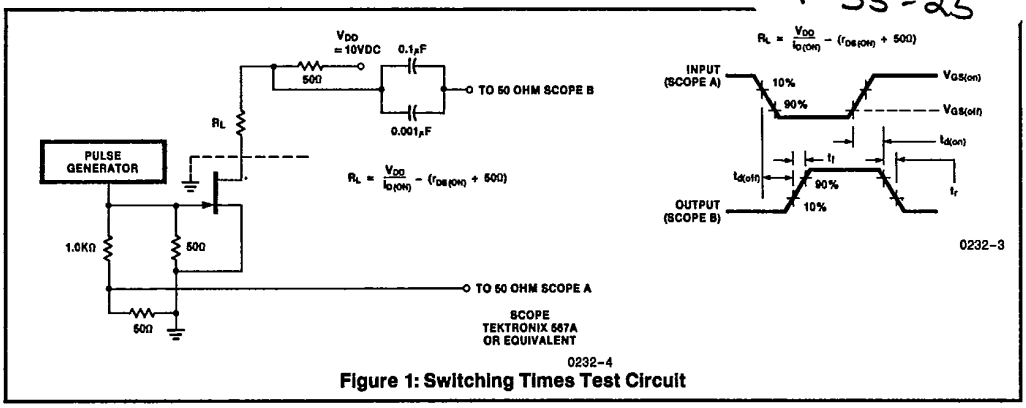

Figure 1: Switching Times Test Circuit

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NOTE: All typical values have been characterized but are not tested.