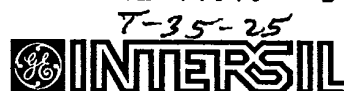


3875081 G E SOLID STATE

01E 11019 D

3N170, 3N171

N-Channel Enhancement Mode MOSFET Switch

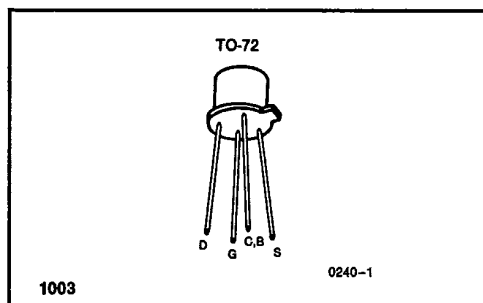


3N170, 3N171

FEATURES

- Low Switching Voltages
- Fast Switching Times
- Low Drain-Source Resistance
- Low Reverse Transfer Capacitance

PIN CONFIGURATION



ORDERING INFORMATION

TO-72
3N170
3N171

HANDLING PRECAUTIONS

MOS field-effect transistors have extremely high input resistance and can be damaged by the accumulation of excess static charge. To avoid possible damage to the device while wiring, testing, or in actual operation, follow the procedures outlined below.

1. To avoid the build-up of static charge, the leads of the devices should remain shorted together with a metal ring except when being tested or used.
2. Avoid unnecessary handling. Pick up devices by the case instead of the leads.
3. Do not insert or remove devices from circuits with the power on as transient voltages may cause permanent damage to the devices.

ABSOLUTE MAXIMUM RATINGS

($T_A = 25^\circ\text{C}$ unless otherwise noted)

Drain-Gate Voltage	$\pm 35\text{V}$
Drain-Source Voltage	25V
Gate-Source Voltage	$\pm 35\text{V}$
Drain Current	30mA
Storage Temperature Range	-65°C to $+200^\circ\text{C}$
Operating Temperature Range	-55°C to $+150^\circ\text{C}$
Lead Temperature (Soldering, 10sec)	$+300^\circ\text{C}$
Power Dissipation	300mW
Derate above 25°C	$2.4\text{mW}/^\circ\text{C}$

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted) Substrate connected to source.

Symbol	Parameter	Test Conditions	Limits		Units
			Min	Max	
BV_{DSS}	Drain-Source Breakdown Voltage	$I_D = 10\mu\text{A}$, $V_{GS} = 0$	25		V
I_{GSS}	Gate Leakage Current	$V_{GS} = \pm 35\text{V}$, $V_{DS} = 0$		± 10	pA
		$V_{GS} = 35\text{V}$, $V_{DS} = 0$, $T_A = 125^\circ\text{C}$		100	
I_{DSS}	Zero-Gate-Voltage Drain Current	$V_{DS} = 10\text{V}$, $V_{GS} = 0$		10	nA
		$T_A = 125^\circ\text{C}$		1.0	μA
$V_{GS(th)}$	Gate-Source Threshold Voltage	$V_{DS} = 10\text{V}$, $I_D = 10\mu\text{A}$	1.0	2.0	V
			1.5	3.0	
$I_{D(on)}$	"ON" Drain Current	$V_{GS} = 10\text{V}$, $V_{DS} = 10\text{V}$	10		mA
$V_{DS(on)}$	Drain-Source "ON" Voltage	$I_D = 10\text{mA}$, $V_{GS} = 10\text{V}$		2.0	V
$r_{ds(on)}$	Drain-Source ON Resistance	$V_{GS} = 10\text{V}$, $I_D = 0$, $f = 1.0\text{kHz}$		200	Ω

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NOTE: All typical values have been characterized but are not tested.

3875081 G E SOLID STATE

01E 11020 D

3N170, 3N171

3N170, 3N171**INTERSIL**

T-35-25

ELECTRICAL CHARACTERISTICS (Continued) ($T_A = 25^\circ\text{C}$ unless otherwise specified) Substrate connected to source.

Symbol	Parameter	Test Conditions	Limits		Units
			Min	Max	
$ Y_{fs} $	Forward Transfer Admittance	$V_{DS} = 10\text{V}$, $I_D = 2.0\text{mA}$, $f = 1.0\text{kHz}$	1000		μS
C_{rss}	Reverse Transfer Capacitance (Note 1)	$V_{DS} = 0$, $V_{GS} = 0$, $f = 1.0\text{MHz}$		1.3	pF
C_{iss}	Input Capacitance (Note 1)	$V_{DS} = 10\text{V}$, $V_{GS} = 0$, $f = 1.0\text{MHz}$		5.0	
$C_{d(sub)}$	Drain-Substrate Capacitance (Note 1)	$V_{D(sub)} = 10\text{V}$, $f = 1.0\text{MHz}$		5.0	
$t_{d(on)}$	Turn-On Delay Time (Note 1)	$V_{DD} = 10\text{V}$, $I_{D(on)} = 10\text{mA}$, $V_{GS(on)} = 10\text{V}$, $V_{GS(off)} = 0$, $R_G = 50\Omega$		3.0	ns
t_r	Rise Time (Note 1)			10	
$t_{d(off)}$	Turn-Off Delay Time (Note 1)			3.0	
t_f	Fall Time (Note 1)			15	

NOTE 1: For design reference only, not 100% tested.

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NOTE: All typical values have been characterized but are not tested.