

Radiation Hardened Single 8/Differential 4 Channel CMOS Analog Multiplexers with Active Overvoltage Protection

The HS-0548RH and HS-0549RH are radiation hardened analog multiplexers with Active Overvoltage Protection and guaranteed r_{ON} matching. Analog input levels may greatly exceed either power supply without damaging the device or disturbing the signal path of other channels. Active protection circuitry assures that signal fidelity is maintained even under fault conditions that would destroy other multiplexers. Analog inputs can withstand constant 70V peak-to-peak levels with $\pm 15V$ supplies and digital inputs will sustain continuous faults up to 4V greater than either supply. In addition, signal sources are protected from short circuiting should multiplexer supply loss occur: each input presents 1k Ω of resistance under this condition. These features make the HS-0548RH and HS-0549RH ideal for use in systems where the analog inputs originate from external equipment or separately powered circuitry. Both devices are fabricated with 44V dielectrically isolated CMOS technology. The HS-0548 is an 8 channel device and the HS-0549 is a 4 channel differential version. If input overvoltage protection is not needed, the HS-0508 and HS-509 multiplexers are recommended.

Specifications for Rad Hard QML devices are controlled by the Defense Supply Center in Columbus (DSCC). The SMD numbers listed here must be used when ordering.

Detailed Electrical Specifications for these devices are contained in SMD 5962-95694. A "hot-link" is provided on our homepage for downloading.
<http://www.intersil.com/spacedefense/space.htm>

Ordering Information

ORDERING NUMBER	INTERNAL MKT. NUMBER	TEMP. RANGE (°C)
5962D9569401VEA	HS1-0548RH-Q	-55 to 125
5962D9569401VEC	HS1B-0548RH-Q	-55 to 125
5962D9569402VEA	HS1-0549RH-Q	-55 to 125
5962D9569402VEC	HS1B-0549RH-Q	-55 to 125

Features

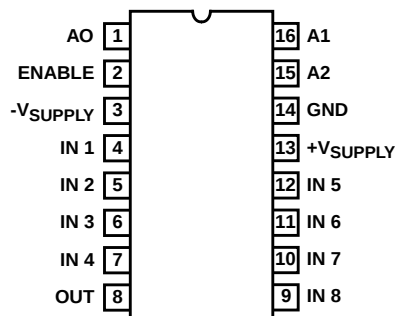
- Electrically Screened to SMD # 5962-95694
- QML Qualified per MIL-PRF-38535 Requirements
- Gamma Dose 1 x 10⁴RAD(Si)
- No Latch-Up
- No Channel Interaction During Overvoltage
- Guaranteed r_{ON} Matching
- Maximum Power Supply 44V
- Break-Before-Make Switching
- Analog Signal Range $\pm 15V$
- Access Time 1.0 μ s

Applications

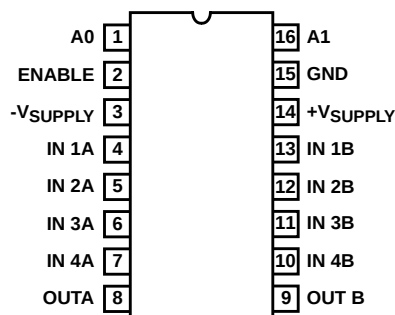
- Data Acquisition Systems
- Control Systems
- Telemetry

Pinouts

**HS-0548RH GDIP1-T16 (CERDIP)
OR CDIP2-T16 (SBDIP)
TOP VIEW**

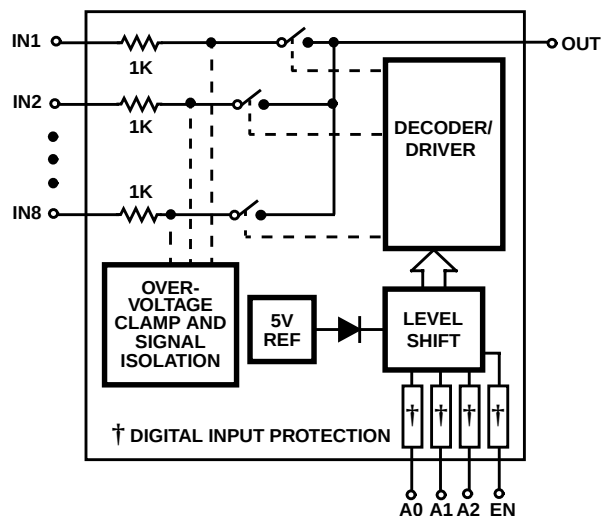


**HS-0549RH GDIP1-T16 (CERDIP)
OR CDIP2-T16 (SBDIP)
TOP VIEW**

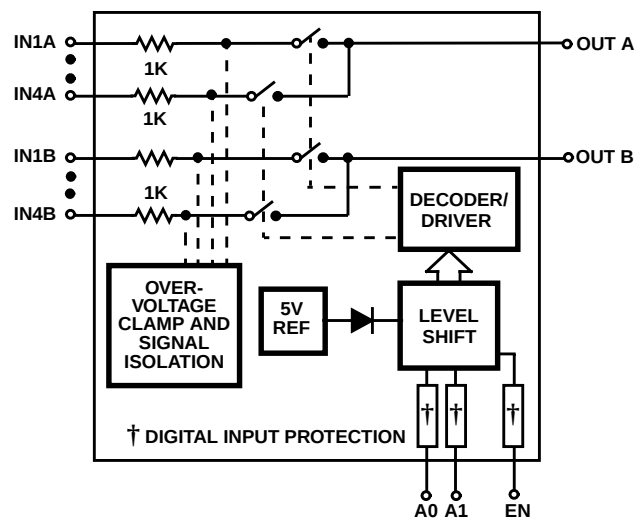


Functional Diagrams

HS-0548



HS-0549



HS-0548 TRUTH TABLE

A2	A1	A0	EN	"ON" CHANNEL
X	X	X	L	NONE
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

HS-0549 TRUTH TABLE

A1	A0	EN	"ON" CHANNEL PAIR
X	X	L	NONE
L	L	H	1
L	H	H	2
H	L	H	3
H	H	H	4

Switching Waveforms

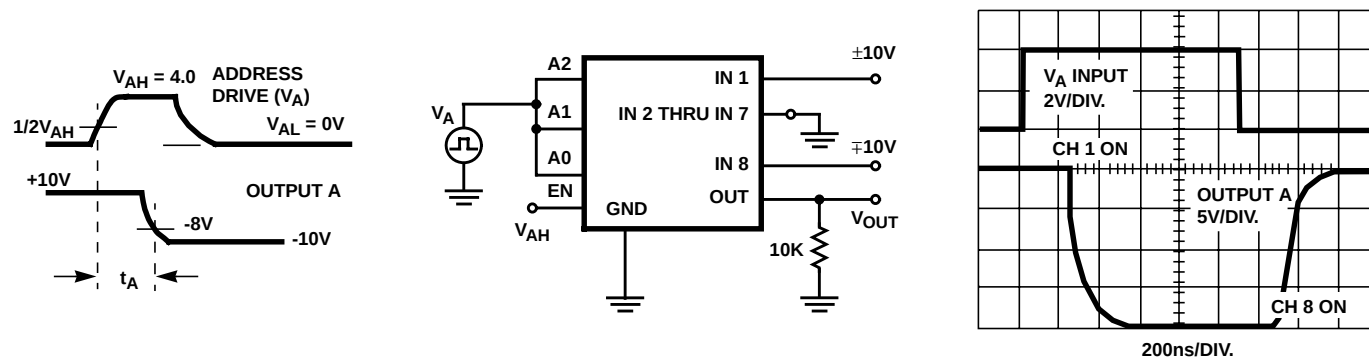


FIGURE 1. ACCESS TIME

Switching Waveforms (Continued)

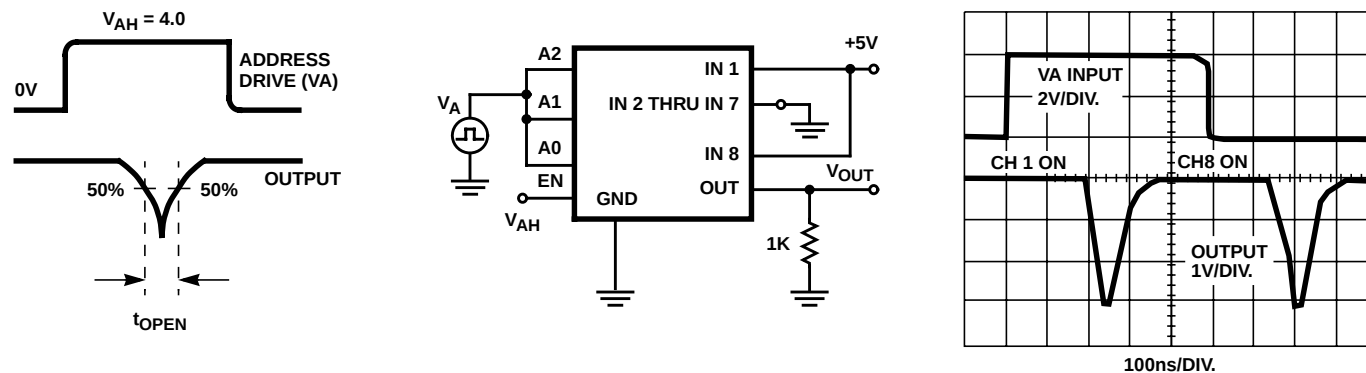


FIGURE 2. BREAK-BEFORE-MAKE DELAY (t_{OPEN})

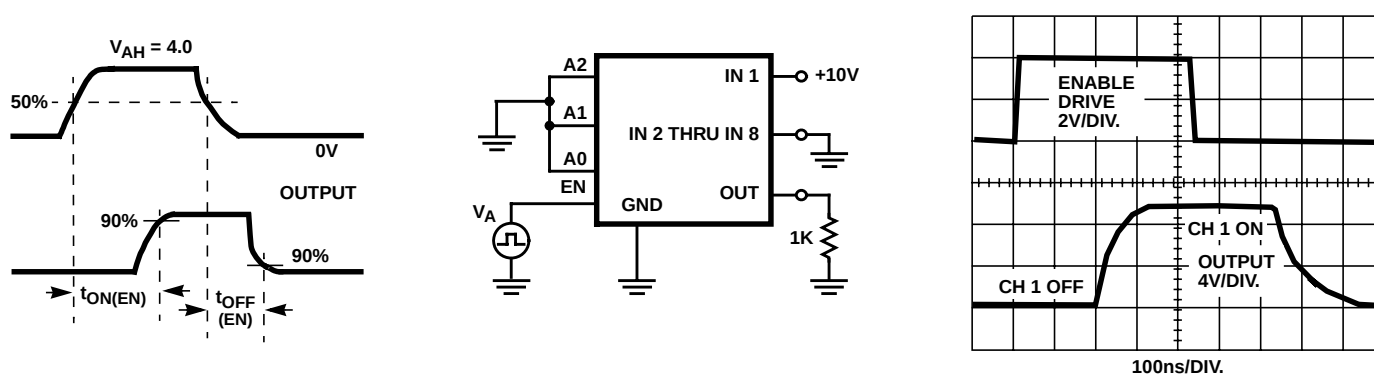
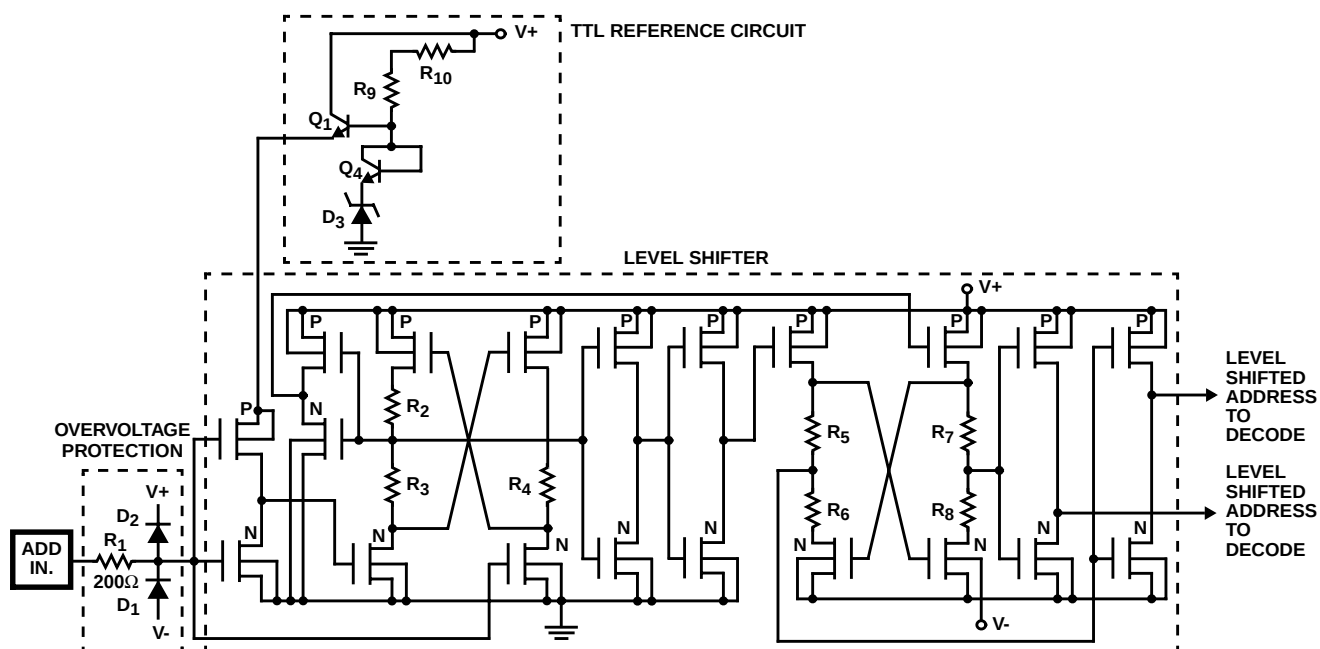


FIGURE 3. ENABLE DELAY $t_{ON(EN)}$, $t_{OFF(EN)}$

Schematic Diagrams



Schematic Diagrams (Continued)

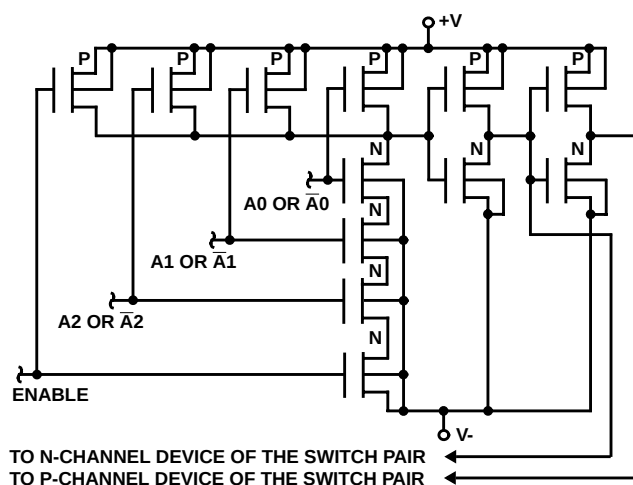


FIGURE 5. ADDRESS DECODER

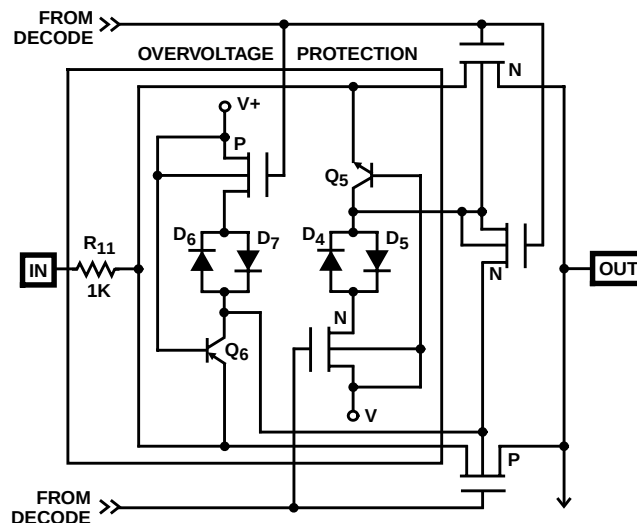
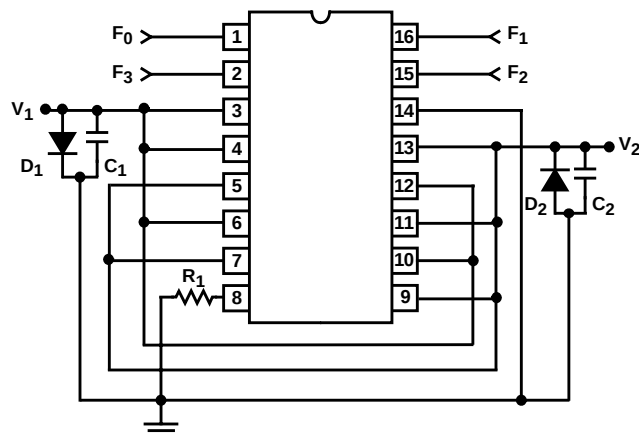


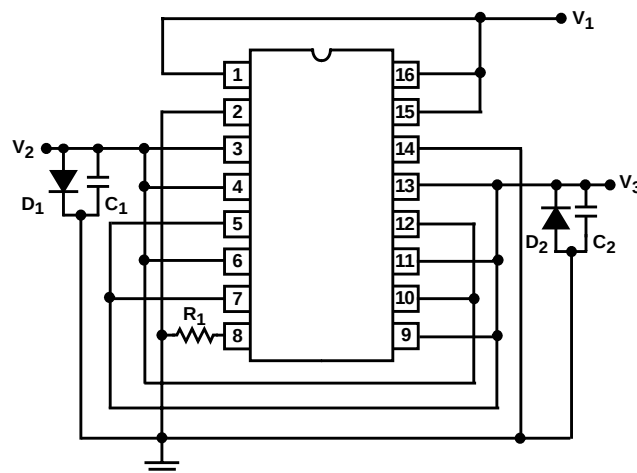
FIGURE 6. MULTIPLEX SWITCH

Burn-In/Life Test Circuits



HS-0548RH
DYNAMIC BURN-IN AND LIFE TEST CIRCUIT

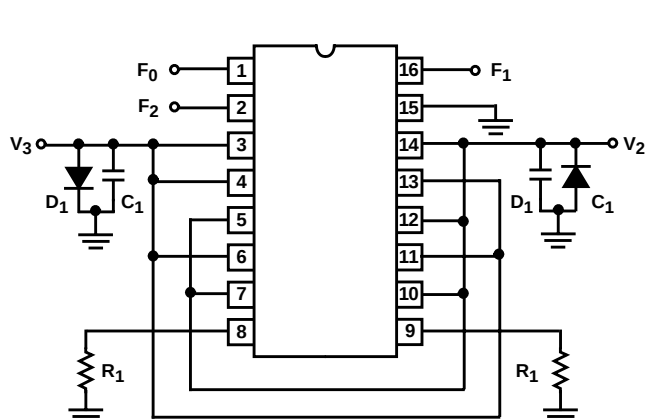
- V_1 = -15V maximum, -16V minimum
- V_2 = +15V minimum, +16V maximum
- R_1 = $10k\Omega \pm 5\%$ 1/4W
- C_1 = C_2 = 0.01 μ F minimum (per socket) or 0.1 μ F minimum (per row)
- D_1 = D_2 = 1N4002 (or equivalent)
- F_0 = 100kHz 50% duty cycle; V_{IL} = 0.8V Max; V_{IH} = 4.0V Min.
- F_1 = $F_0/2$
- F_2 = $F_1/2$
- F_3 = $F_2/2$



HS-0548RH
STATIC BURN-IN TEST CIRCUIT

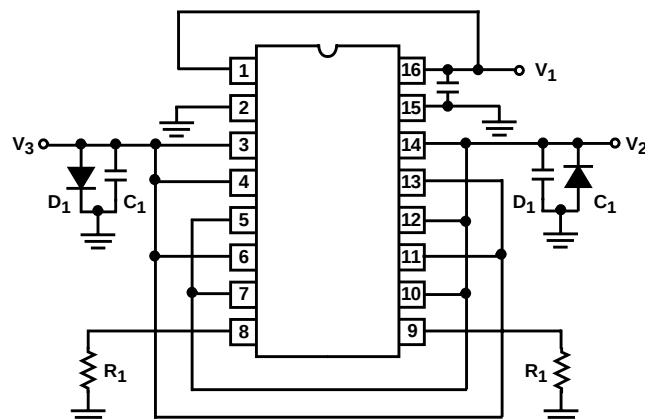
- V_1 = 5V minimum, 6V maximum
- V_2 = -15V maximum, -16V minimum
- V_3 = +15V minimum, +16V maximum
- R_1 = $10k\Omega \pm 5\%$ 1/4W
- C_1 = C_2 = 0.01 μ F minimum (per socket) or 0.1 μ F minimum (per row)
- D_1 = D_2 = 1N4002 (or equivalent)

Burn-In/Life Test Circuits (Continued)



HS-0549RH
DYNAMIC BURN-IN AND LIFE TEST CIRCUIT

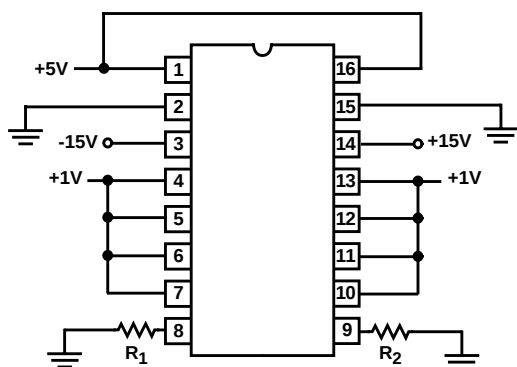
$V_2 = +15.5V, \pm 0.5V$
 $V_3 = -15.5V, \pm 0.5V$
 $R_1 = 10k\Omega, \pm 5\%$
 $C_1 = 0.01\mu F$ minimum (per socket)
 $D_1 = 1N4002$ or equivalent (per board)
 $F_0 = 100kHz, \pm 10\%$; $F_1 = F_0/2$; $F_2 = F_1/2$,
 50% duty cycle, $V_{IL} = 0.8V$ Max; $V_{IH} = 4.0V$ Min



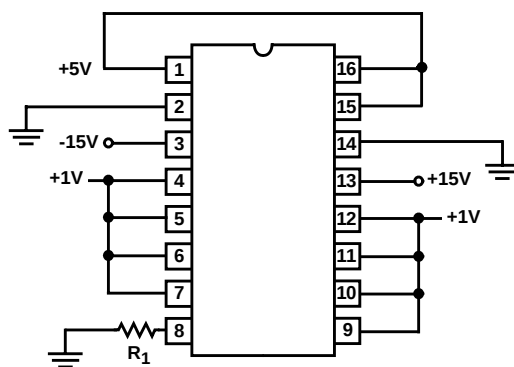
HS-0549RH
STATIC BURN-IN TEST CIRCUIT

$V_1 = +5.5V, \pm 0.5V$
 $V_2 = +15.5V, \pm 0.5V$
 $V_3 = -15.5V, \pm 0.5V$
 $R_1 = 10k\Omega, \pm 10\%$
 $C_1 = 0.01\mu F$ minimum (per socket)
 $D_1 = 1N4002$ or equivalent (per board)

Irradiation Circuits



HS-0549RH
 $R_1 = R_2 = 10k\Omega \pm 5\%$



HS-0548RH
 $R_1 = 10k\Omega \pm 5\%$

Die Characteristics

DIE DIMENSIONS:

83 mils x 108 mils x 19 mils

INTERFACE MATERIALS:

Glassivation:

Type: Nitride

Thickness: $7\text{k}\text{\AA} \pm 0.7\text{k}\text{\AA}$

Top Metallization:

Type: Al

Thickness: $16\text{k}\text{\AA} \pm 2\text{k}\text{\AA}$

Substrate:

CMOS, DI

ASSEMBLY RELATED INFORMATION:

Substrate Potential:

Floating

ADDITIONAL INFORMATION:

Worst Case Current Density:

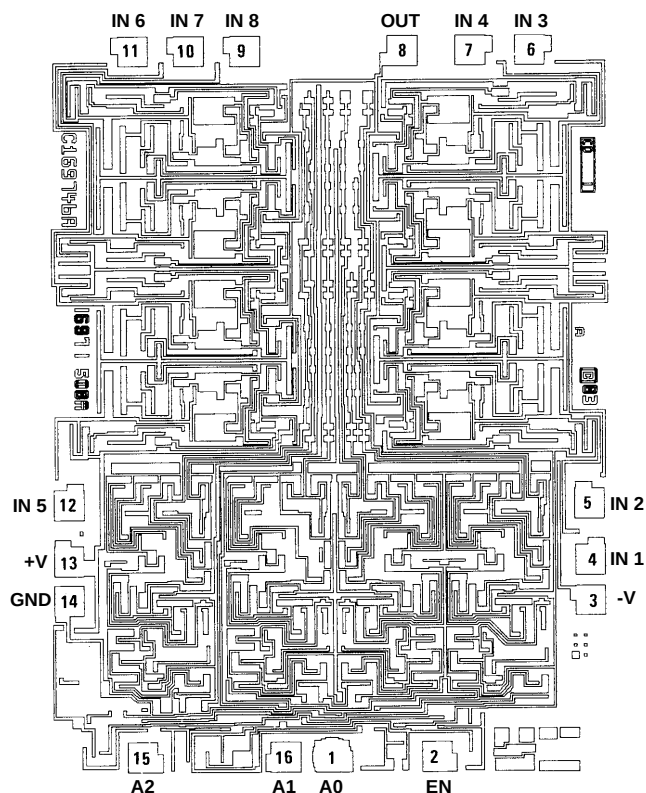
$1.4 \times 10^5 \text{ A/cm}^2$

Transistor Count:

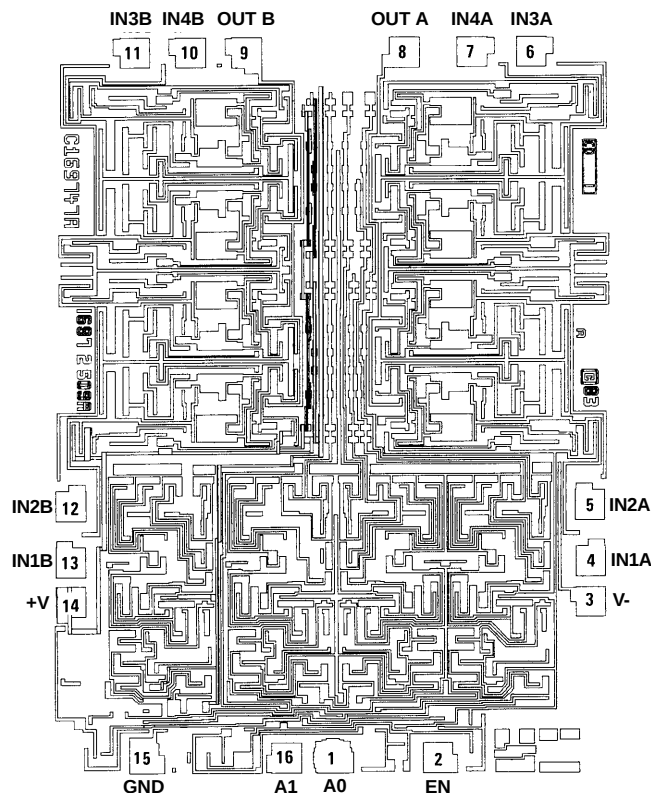
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Metallization Mask Layout

HS-0548RH



HS-0549RH



NOTE: Pad Numbers Correspond to DIP Pin Numbers Only

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