

March 1997

CMOS Octal Latching Bus Driver

Features

- Full Eight-Bit Parallel Latching Buffer
- Bipolar 8282 Compatible
- Three-State Noninverting Outputs
- Propagation Delay 35ns Max.
- Gated Inputs:
 - Reduce Operating Power
 - Eliminate the Need for Pull-Up Resistors
- Single 5V Power Supply
- Low Power Operation ICCSB = 10 μ A
- Operating Temperature Ranges
 - C82C82 0°C to +70°C
 - I82C82 -40°C to +85°C
 - M82C82 -55°C to +125°C

Description

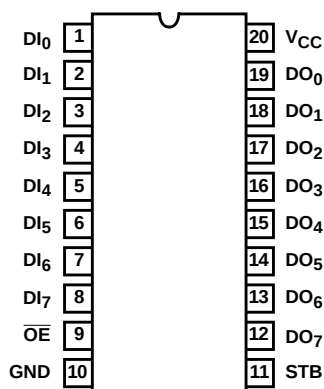
The Intersil 82C82 is a high performance CMOS Octal Latching Buffer manufactured using a self-aligned silicon gate CMOS process (Scaled SAJI IV). The 82C82 provides an eight-bit parallel latch/buffer in a 20 pin package. The active high strobe (STB) input allows transparent transfer of data and latches data on the negative transition of this signal. The active low output enable ($\overline{OE}$) permits simple interface to state-of-the-art microprocessor systems.

Ordering Information

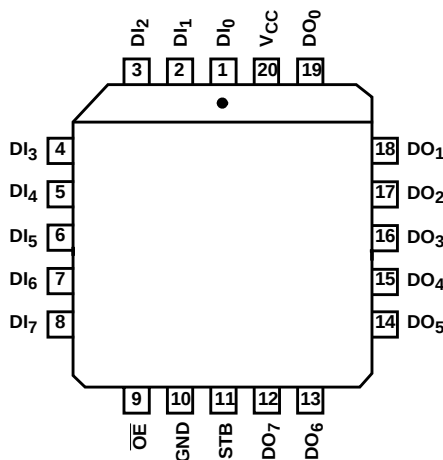
PART NUMBER	TEMP. RANGE	PACKAGE	PKG. NO.
CP82C82	0°C to +70°C	20 Ld PDIP	E20.3
IP82C82	-40°C to +85°C		
CS82C82	0°C to +70°C	20 Ld PLCC	N20.35
IS82C82	-40°C to +85°C		
CD82C82	0°C to +70°C	20 Ld Cerdip	F20.3
ID82C82	-40°C to +85°C		
MD82C82/B	-55°C to +125°C		
8406701RA		SMD #	
MR82C82/B	-55°C to +125°C	20 Pad CLCC	J20.A
84067012A		SMD #	

Pinouts

82C82 (PDIP, Cerdip)
TOP VIEW



82C82 (PLCC, CLCC)
TOP VIEW



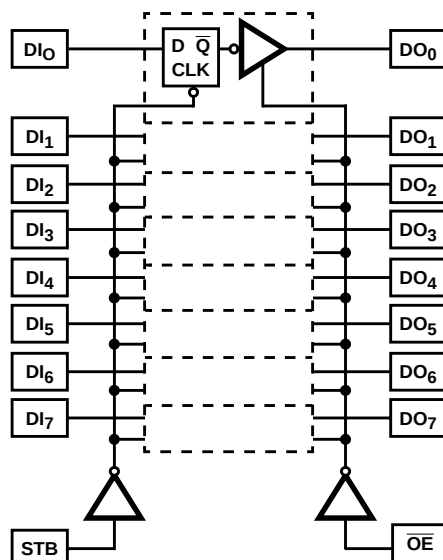
TRUTH TABLE

STB	$\overline{OE}$	DI	DO
X	H	X	Hi-Z
H	L	L	L
H	L	H	H
↓	L	X	†

H = Logic One
 L = Logic Zero
 X = Don't Care
 † = Latched to Value of Last Data
 Hi-Z = High Impedance
 ↓ = Neg. Transition

PIN NAMES

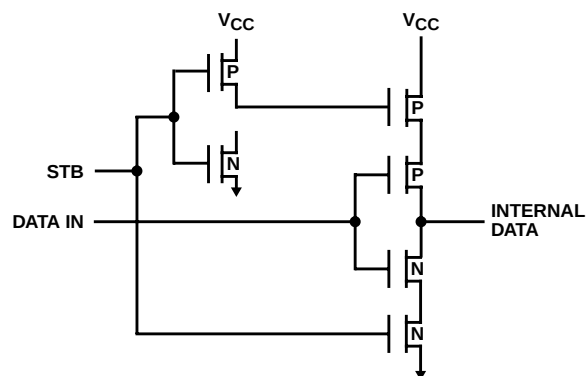
PIN	DESCRIPTION
DI ₀ -DI ₇	Data Input Pins
DO ₀ -DO ₇	Data Output Pins
STB	Active High Strobe
$\overline{OE}$	Active Low Output Enable



During normal system operation of a latch, signals on the bus at the device inputs will become high impedance or make transitions unrelated to the operation of the latch. These unrelated input transitions switch the input circuitry and typically cause an increase in power dissipation in CMOS devices by creating a low resistance path between V_{CC} and GND when the signal is at or near the input switching threshold. Additionally, if the driving signal becomes high impedance ("float" condition), it could create an indeterminate logic state at the input and cause a disruption in device operation.

DC input voltage levels can also cause an increase in ICC if these input levels approach the minimum V_{IH} or maximum V_{IL} conditions. This is due to the operation of the input circuitry in its linear operating region (partially conducting state). The 82C8X series gated inputs mean that this condition will occur only during the time the device is in the transparent mode (STB = logic one). ICC remains below the maximum ICC standby specification of 10mA during the time inputs are disabled, thereby, greatly reducing the average power dissipation of the 82C8X series devices

In a typical 80C86/88 system, the 82C82 is used to latch multiplexed addresses and the STB input is driven by ALE (Address Latch Enable) (see Figure 3). The high pulse width of ALE is approximately 100ns with a bus cycle time of 800ns (80C86/88 at 5MHz). The 82C82 inputs are active only 12.5% of the bus cycle time. Average power dissipation related to input transitioning is reduced by this factor also.



The circuit diagram shows a 3-to-8 decoder implemented using a 74VHC04 inverter and a 74VHC153 3-to-8 decoder. The 74VHC153 has three data inputs: $\overline{A}$, A , and B . The $\overline{A}$ input is connected to the $\overline{OE}$ output of the 74VHC04. The A input is connected to the $\overline{DATA\ IN}$ input of the 74VHC04. The B input is connected to the $\overline{DATA\ IN}$ input of the 74VHC04. The 74VHC153 has eight outputs, labeled Y_0 through Y_7 . The Y_0 output is connected to the $\overline{DATA\ IN}$ input of the 74VHC04. The Y_1 output is connected to the $\overline{DATA\ IN}$ input of the 74VHC04. The Y_2 output is connected to the $\overline{DATA\ IN}$ input of the 74VHC04. The Y_3 output is connected to the $\overline{DATA\ IN}$ input of the 74VHC04. The Y_4 output is connected to the $\overline{DATA\ IN}$ input of the 74VHC04. The Y_5 output is connected to the $\overline{DATA\ IN}$ input of the 74VHC04. The Y_6 output is connected to the $\overline{DATA\ IN}$ input of the 74VHC04. The Y_7 output is connected to the $\overline{DATA\ IN}$ input of the 74VHC04. The 74VHC04 has two inputs: $\overline{DATA\ IN}$ and $\overline{OE}$. The $\overline{DATA\ IN}$ input is connected to the $\overline{DATA\ IN}$ input of the 74VHC153. The $\overline{OE}$ output is connected to the $\overline{A}$ input of the 74VHC153. The 74VHC04 has two outputs: $\overline{DATA\ IN}$ and $\overline{OE}$. The $\overline{DATA\ IN}$ output is connected to the $\overline{DATA\ IN}$ input of the 74VHC153. The $\overline{OE}$ output is connected to the $\overline{A}$ input of the 74VHC153. The 74VHC153 has two power supply pins: V_{CC} and GND . The V_{CC} pin is connected to the V_{CC} pin of the 74VHC04. The GND pin is connected to the GND pin of the 74VHC04. The 74VHC04 has two power supply pins: V_{CC} and GND . The V_{CC} pin is connected to the V_{CC} pin of the 74VHC153. The GND pin is connected to the GND pin of the 74VHC153.

FIGURE 17. 82C86H/87H GATED INPUTS

Application Information

Decoupling Capacitors

The transient current required to charge and discharge the 300pF load capacitance specified in the 82C82 data sheet is determined by:

$$I = C_L (dv/dt) \quad (\text{EQ. 1})$$

Assuming that all outputs change state at the same time and that dv/dt is constant;

$$I = C_L \quad (\text{EQ. 2})$$

$$\frac{(V_{CC} \times 80\%)}{tR/tF} \quad (\text{EQ. 3})$$

where $tR = 20\text{ns}$, $V_{CC} = 5.0\text{V}$, $C_L = 300\text{pF}$ on each of eight outputs.

$$I = (8 \times 300 \times 10^{-12}) \times (5.0\text{V} \times 0.8) / (20 \times 10^{-9}) = 480\text{mA} \quad (\text{EQ. 4})$$

This current spike may cause a large negative voltage spike on V_{CC} , which could cause improper operation of the device. To filter out this noise, it is recommended that a $0.1\mu\text{F}$ ceramic disc decoupling capacitor be placed between V_{CC} and GND at each device, with placement being as near to the device as possible.

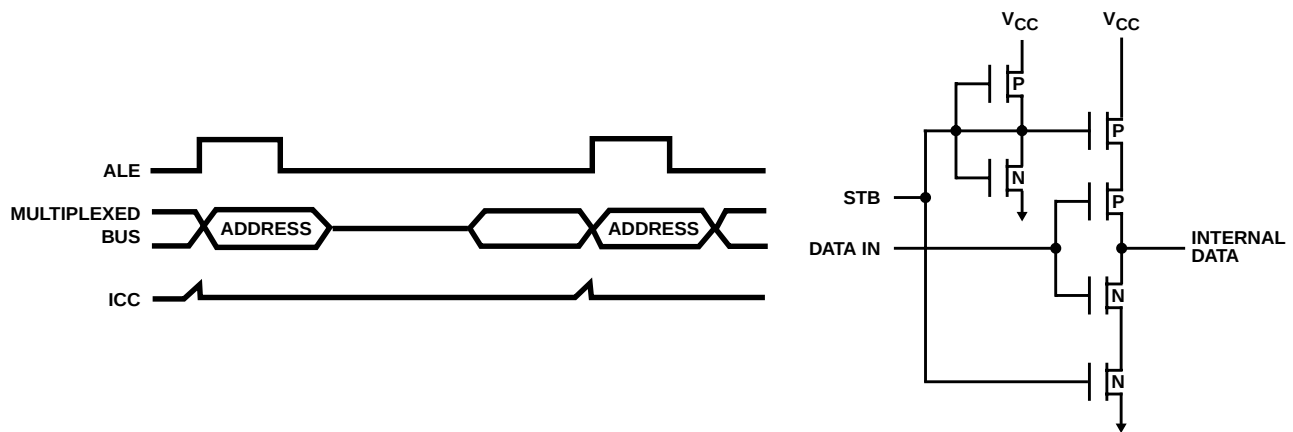


FIGURE 18. SYSTEM EFFECTS OF GATED INPUTS

82C82

Absolute Maximum Ratings

Supply Voltage +8.0V
 Input, Output or I/O Voltage GND-0.5V to $V_{CC} + 0.5V$
 ESD Classification Class 1

Operating Conditions

Operating Voltage Range +4.5V to +5.5V
 Operating Temperature Range
 C82C82 0°C to +70°C
 I82C82 -40°C to +85°C
 M82C82 -55°C to +125°C

Thermal Information

Thermal Resistance (Typical)	θ_{JA}	θ_{JC}
CERDIP	75°C/W	18°C/W
CLCC	85°C/W	22°C/W
PDIP	75	N/A
PLCC	75	N/A

Storage Temperature Range -65°C to +150°C
 Maximum Junction Temperature
 Ceramic Package +175°C
 Plastic Package +150°C
 Minimum Lead Temperature (Soldering 10s) +300°C
 (PLCC Lead Tips Only)

Die Characteristics

Gate Count 65 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

DC Electrical Specifications $V_{CC} = 5.0V \pm 10\%$;

$T_A = 0^\circ C$ to +70°C (C82C82);
 $T_A = -40^\circ C$ to +85°C (I82C82);
 $T_A = -55^\circ C$ to +125°C (M82C82)

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
V_{IH}	Logical One Input Voltage	2.0	-	V	C82C82, I82C82 (Note 1)
		2.2	-	V	M82C82 (Note 1)
V_{IL}	Logical Zero Input Voltage	-	0.8	V	
V_{OH}	Logical One Output Voltage	2.9	-	V	$I_{OH} = -8mA$, $\overline{OE} = GND$
		$V_{CC} - 0.4V$	-	V	$I_{OH} = -100\mu A$, $\overline{OE} = GND$
V_{OL}	Logical Zero Output Voltage	-	0.4	V	$I_{OL} = 8mA$, $\overline{OE} = GND$
II	Input Leakage Current	-1.0	1.0	μA	$V_{IN} = GND$ or V_{CC} , DIP Pins 1-9, 11
IO	Output Leakage Current	-10.0	10.0	μA	$V_O = GND$ or V_{CC} , $\overline{OE} \geq V_{CC} - 0.5V$ DIP Pins 12-19
ICCSB	Standby Power Supply Current	-	10	μA	$V_{IN} = V_{CC}$ or GND, $V_{CC} = 5.5V$, Outputs Open
ICCOP	Operating Power Supply Current	-	1	mA/MHz	$T_A = +25^\circ C$, $V_{CC} = 5V$, Typical (See Note 2)

NOTES:

- V_{IH} is measured by applying a pulse of magnitude = V_{IH} min to one data input at a time and checking the corresponding device output for a valid logical "1" during valid input high time. Control pins (STB, $\overline{OE}$) are tested separately with all device data input pins at $V_{CC} - 0.4$.
- Typical ICCOP = 1mA/MHz of STB cycle time. (Example: 5MHz μP , ALE = 1.25MHz, ICCOP = 1.25mA).

Capacitance $T_A = +25^\circ C$

SYMBOL	PARAMETER	TYPICAL	UNITS	TEST CONDITIONS
C_{IN}	Input Capacitance	13	pF	Freq = 1MHz, all measurements are referenced to device GND
C_{OUT}	Output Capacitance	20	pF	

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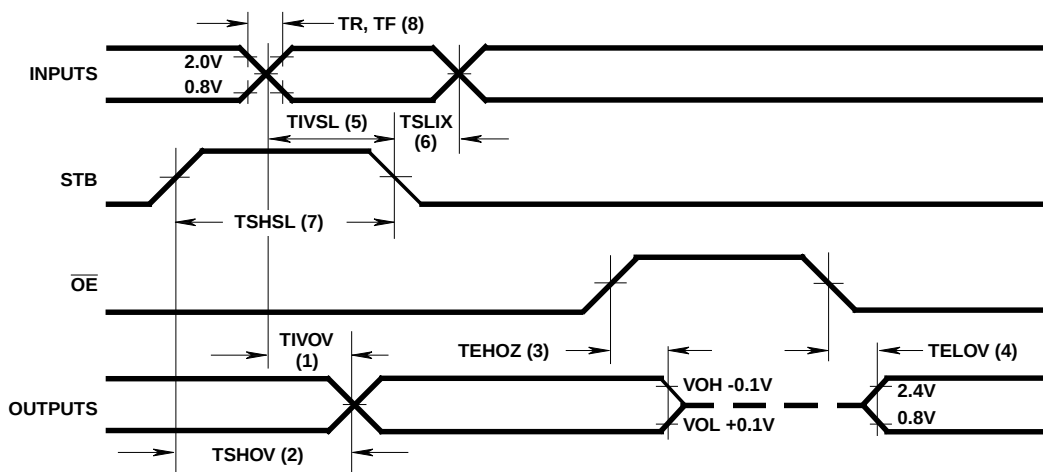
AC Electrical Specifications $V_{CC} = 5.0V \pm 10\%$; $T_A = 0^{\circ}C$ to $+70^{\circ}C$ (C82C82);
 $C_L = 300pF$ (Note 1), Freq = 1MHz $T_A = -40^{\circ}C$ to $+85^{\circ}C$ (I82C82);
 $T_A = -55^{\circ}C$ to $+125^{\circ}C$ (M82C82)

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
(1) TIOV	Propagation Delay Input to Output	-	35	ns	Notes 2, 3
(2) TSHOV	Propagation Delay STB to Output	-	55	ns	Notes 2, 3
(3) TEHOZ	Output Disable Time	-	35	ns	Notes 2, 3
(4) TELOV	Output Enable Time	-	50	ns	Notes 2, 3
(5) TIVSL	Input to STB Setup Time	0	-	ns	Notes 2, 3
(6) TSLIX	Input to STB Hold Time	25	-	ns	Notes 2, 3
(7) TSHSL	STB High Time	25	-	ns	Notes 2, 3
(8) TR, TF	Input Rise/Fall Times	-	20	ns	Notes 2, 3

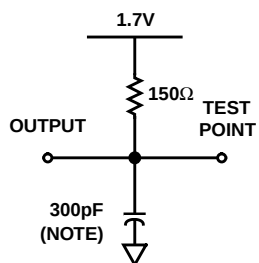
NOTES:

- Output load capacitance is rated at 300pF for ceramic and plastic packages.
- All AC parameters tested as per test circuits and definitions below. Input rise and fall times are driven at 1ns/V.
- Input test signals must switch between $V_{IL} - 0.4V$ and $V_{IH} + 0.4V$.

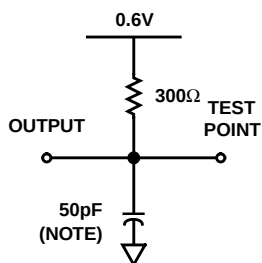
Timing Waveforms



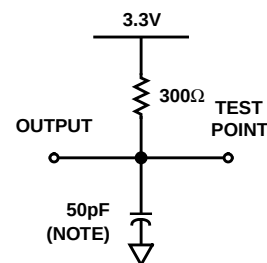
Test Load Circuits



TIOV, TSHOV, TELOV



TEHOZ OUTPUT HIGH DISABLE

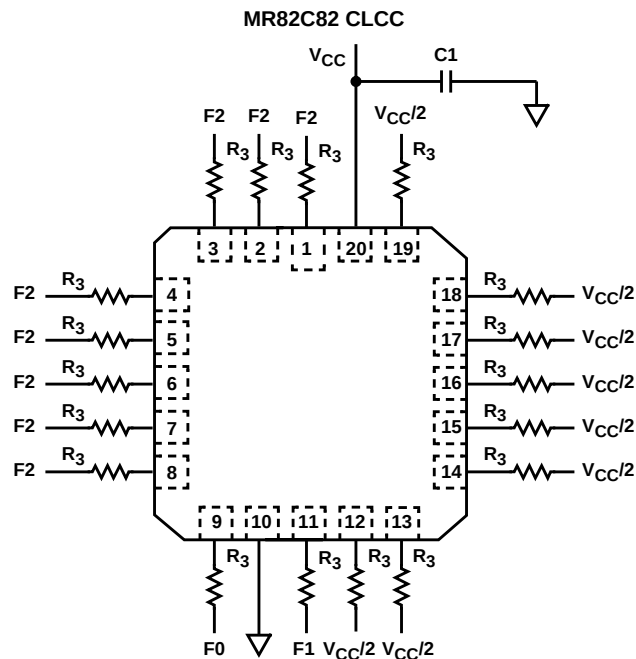
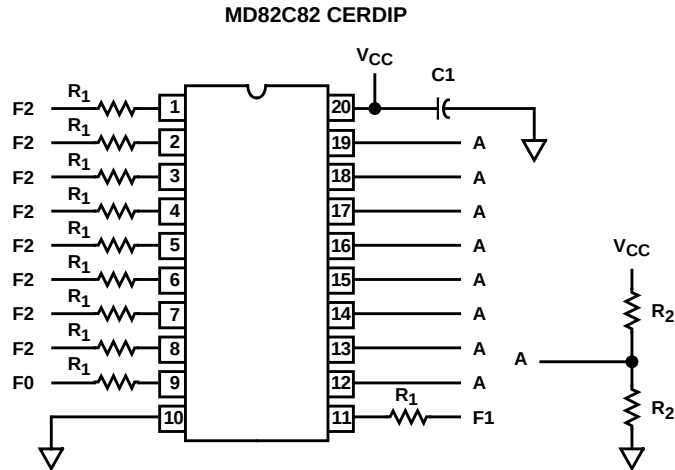


TEHOZ OUTPUT LOW DISABLE

NOTE: Includes stray and jig capacitance.

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Burn-In Circuits



NOTES:

1. $V_{CC} = 5.5 \pm 0.5V$, GND = 0V.
2. $V_{IH} = 4.5V \pm 10\%$.
3. $V_{IL} = -0.2V$ to $0.4V$.
4. $R_1 = 47k\Omega \pm 5\%$.
5. $R_2 = 2.0k\Omega \pm 5\%$.
6. $R_3 = 4.2k\Omega \pm 5\%$.
7. $R_4 = 470k\Omega \pm 5\%$.
8. $C_1 = 0.01\mu F$ minimum.
9. $F_0 = 100kHz \pm 10\%$.
10. $F_1 = F_0/2$, $F_2 = F_1/2$.

Die Characteristics

DIE DIMENSIONS:

118.1 x 92.1 x 19 ±1mils

METALLIZATION:

Type: Si - Al

Thickness: 11kÅ ±1kÅ

GLASSIVATION:

Type: SiO₂

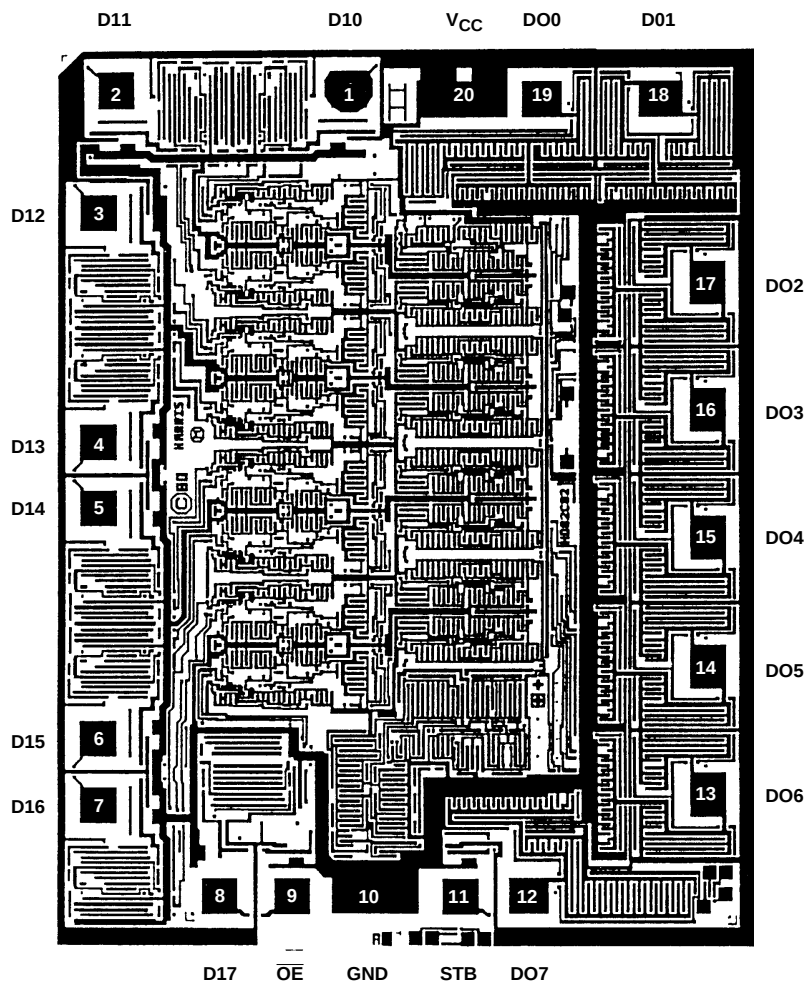
Thickness: 8kÅ ±1kÅ

WORST CASE CURRENT DENSITY:

2.00 x 10⁵ A/cm²

Metallization Mask Layout

82C82



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