

Successive Approximation Registers

FEATURES

- Contains all the storage and control for successive approximation A to D converters.
- Provision for register extension or truncation.
- Can be operated in START-STOP or continuous conversion mode.
- 100% reliability assurance testing in compliance with MIL-STD-883.
- Can be used as serial-to-parallel counter or ring counters.
- Electrically tested and optically inspected dice for the assemblers of hybrid products.

GENERAL DESCRIPTION

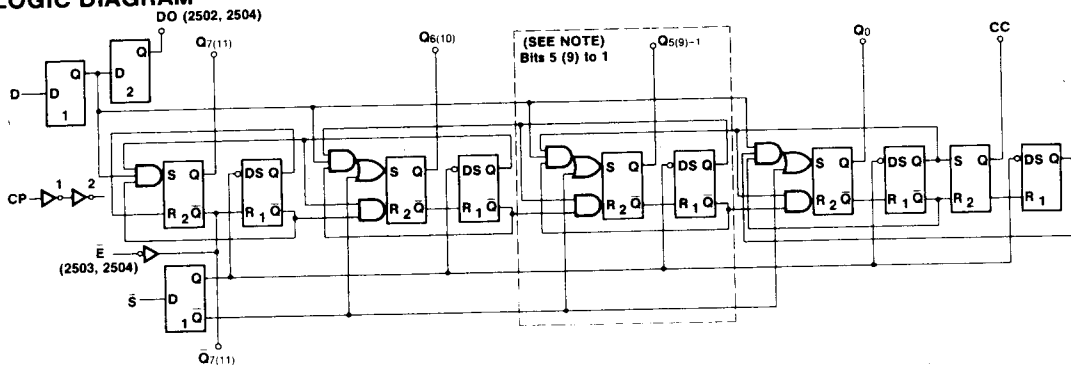
The AM2502/3/4 are 8-bit and 12-bit TTL Successive Approximation Registers. They contain all the digital control and storage necessary for successive approximation analog to digital conversion and can also be used in digital

systems as the control and storage element in recursive digital routines.

The registers consist of a set of master latches which act as the control elements and change state when the input clock is LOW, and a set of slave latches that hold the register data and change on the input clock LOW to HIGH transition. Externally the device acts as a special purchase serial to parallel converter which accepts data at the D input of the register and sends the data to the appropriate slave latch to appear at the register output and the DO output on the 2502 and 2504 when the clock goes from LOW to HIGH. There are no restrictions on the data input; it can change state at any time except during the set-up time just prior to the clock transition. At the same time data enters the register bit the next less significant bit is set to a LOW, ready for the next iteration.

The AM25L02/L03/L04 are low power equivalents of the AM2502/03/04.

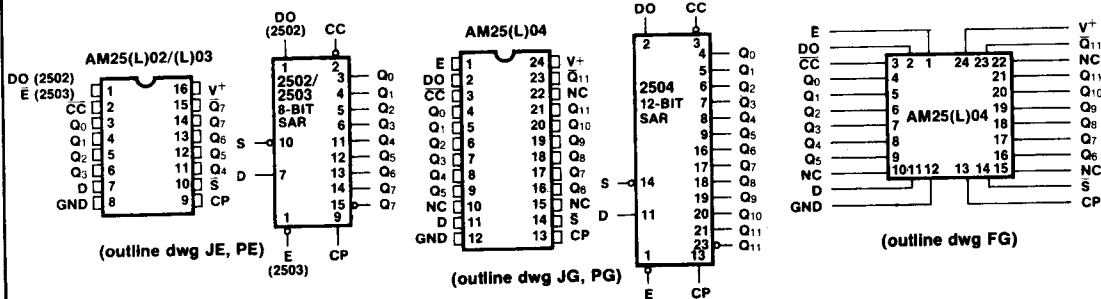
LOGIC DIAGRAM



NOTES

1. CELL LOGIC IS REPEATED FOR REGISTER STAGES.
Q₅ TO Q₁: 2502/3
Q₉ TO Q₁: 2504
2. NUMBERS IN PARENTHESES ARE FOR 2504

PIN CONFIGURATIONS AND LOGIC SYMBOLS



AM2502/3/4, AM25L02/3/4

INTERSIL

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	-0.5V to +7V
DC Voltage Applied to Outputs for High Output State	-0.5V to V ⁺
DC Input Voltage	-0.5V to +5.5V
Output Current, Into Outputs	30mA
DC Input Current	-30mA to +5.0mA
Storage Temperature	-65°C to +150°C
Operating Temperatures	
M devices	-55°C to +125°C
C devices	0°C to +70°C
Lead Temperature (soldering, 10s)	300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CHARACTERISTICS V⁺ = 5V, T_A = Operating Temperature Range unless otherwise specified

PARAMETER		SYMBOL	TEST CONDITIONS	LIMITS			UNIT	
				MIN.	TYP. ⁽¹⁾	MAX.		
Output high voltage		V _{OH}	V ⁺ = min, I _{OH} = -0.48mA V _{IN} = V _{IL} or V _{IH}	2.4	3.6		V	
Output low voltage		V _{OL}	V ⁺ = min, I _{OH} = 0.96mA V _{IN} = V _{IL} or V _{IH}		0.2	0.4	V	
Input high voltage		V _{IH}	Guaranteed input logic HIGH voltage for all inputs	2.0			V	
Input low voltage		V _{IL}	Guaranteed input logic LOW voltage for all inputs			0.8	V	
Unit load input low current (2)	AM2502/3/4	I _{IL}	V ⁺ = max, V _{IN} = 0.4V		-1.0	-1.6	mA	
	AM25L02/3/4				-0.25	-0.4		
Unit load input high current (2)	AM2502/3/4	I _{IH}	V ⁺ = max, V _{IN} = 2.4V		6.0	40	μA	
	AM25L02/3/4				2.0	20		
Input high current		I _{IH}	V ⁺ = max, V _{IN} = 5.5V			1.0	mA	
Output short circuit current		I _{SC}	V ⁺ = max, V _O = 0V	2502/3/4	-10	-25	-45	mA
				25L02/3/4	-3	-7	-16	
Power Supply Current		I [*]	V ⁺ = max	AM2502/3	C	65	95	mA
					M	65	85	
				AM25L02/3	C	25	35	mA
					M	25	33	
				AM2504	C	90	124	mA
					M	90	110	
AM25L04	C	30	45	mA				
	M	30	42					

NOTES: 1. Typical limits are with V⁺ = 5.0V, T_A = 25°C and maximum loading.

2. Actual input currents are obtained by multiplying unit load current by input load factor (see Loading Rules).

SWITCHING CHARACTERISTICS T_A = 25°C, V⁺ = 5.0V, C_L = 15pF

PARAMETERS	DESCRIPTION	AM2502/3/4			AM25L02/3/4			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
t _{pd+}	Turn Off Delay CP to Output HIGH	10	26	38	20	75	110*	ns
t _{pd-}	Turn On Delay CP to Output LOW	10	18	28	20	75	100	ns
t _{s(D)}	Set-up Time Data Input	-10	4	8	-15	8	20	ns
t _{s(S)}	Set-up Time Start Input	0	9	16	0	20	25	ns
t _{pd+(E)}	Turn Off Delay E to Q ₇₍₁₁₎		13	19		50	75	ns
t _{pd-(E)}	Turn On Delay E to Q ₇₍₁₁₎ LOW		16	24		60	75	ns
t _{pwL} (CP)	Minimum LOW Clock Pulse Width		28	46		100	150	ns
t _{pwH} (CP)	Minimum HIGH Clock Pulse Width		12	20		70	100	ns
f _{max}	Maximum Clock Frequency	15	25		3.5	5.0		MHz

*Q₁₁, Q₁₁ 30 ns slower

AM2502/3/4, AM25L02/3/4

INTERMIL

25(L)02/3 LOADING RULES (IN UNIT LOADS)

INPUT/ OUTPUT	PIN NO.'s	INPUT UNIT LOAD		FANOUT	
		LOW	HIGH	OUTPUT HIGH	OUTPUT LOW
\bar{E} (2503)	1	2	2	—	—
DO (2502)	1	—	—	12	6
CC	2	—	—	12	6
Q ₀	3	—	—	12	6
Q ₁	4	—	—	12	6
Q ₂	5	—	—	12	6
Q ₃	6	—	—	12	6
D	7	2	2	—	—
GND	8	—	—	—	—
CP	9	1	1	—	—
S	10	1	2	—	—
Q ₄	11	—	—	12	6
Q ₅	12	—	—	12	6
Q ₆	13	—	—	12	6
Q ₇	14	—	—	12	6
Q ₇	15	—	—	12	6
V ⁺	16	—	—	—	—

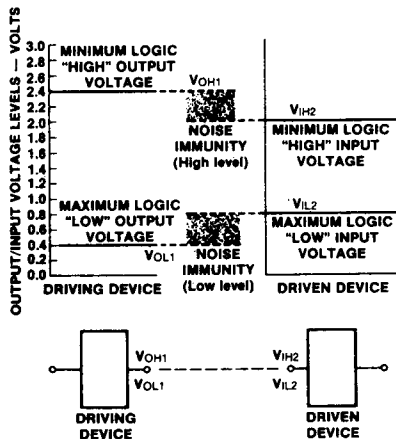
25(L)04 LOADING RULES (IN UNIT LOADS)

INPUT/ OUTPUT	PIN NO.'s	INPUT UNIT LOAD		FANOUT	
		LOW	HIGH	OUTPUT HIGH	OUTPUT LOW
\bar{E}	1	2	2	—	—
DO	2	—	—	12	6
CC	3	—	—	12	6
Q ₀	4	—	—	12	6
Q ₁	5	—	—	12	6
Q ₂	6	—	—	12	6
Q ₃	7	—	—	12	6
Q ₄	8	—	—	12	6
Q ₅	9	—	—	12	6
NC	10	—	—	—	—
D	11	2	2	—	—
GND	12	—	—	—	—
CP	13	1	1	—	—
\bar{S}	14	1	2	—	—
NC	15	—	—	—	—
Q ₆	16	—	—	12	6
Q ₇	17	—	—	12	6
Q ₈	18	—	—	12	6
Q ₉	19	—	—	12	6
Q ₁₀	20	—	—	12	6
\bar{Q}_{11}	21	—	—	12	6
NC	22	—	—	—	—
Q ₁₁	23	—	—	12	6
V ⁺	24	—	—	—	—

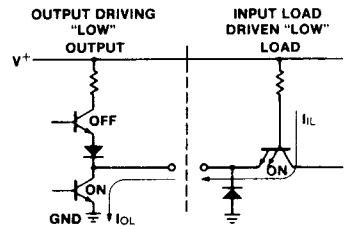
NC = No Connection

INPUT/OUTPUT INTERFACE CONDITIONS

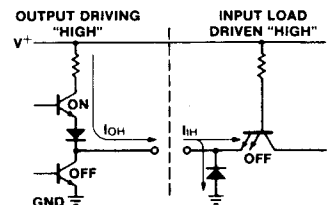
VOLTAGE INTERFACE CONDITIONS — LOW & HIGH



CURRENT INTERFACE CONDITIONS — LOW



CURRENT INTERFACE CONDITIONS — HIGH



AM25(L)02/3 TRUTH TABLE

TIME	INPUTS			OUTPUTS										
	t _n	D	S	E	D ₀	Q ₇	Q ₆	Q ₅	Q ₄	Q ₃	Q ₂	Q ₁	Q ₀	CC
0	X	L	L	X	X	X	X	X	X	X	X	X	X	X
1	D ₇	H	L	X	L	H	H	H	H	H	H	H	H	H
2	D ₆	H	L	D ₇	D ₇	L	H	H	H	H	H	H	H	H
3	D ₅	H	L	D ₆	D ₇	D ₆	L	H	H	H	H	H	H	H
4	D ₄	H	L	D ₅	D ₇	D ₆	D ₅	L	H	H	H	H	H	H
5	D ₃	H	L	D ₄	D ₇	D ₆	D ₅	D ₄	L	H	H	H	H	H
6	D ₂	H	L	D ₃	D ₇	D ₆	D ₅	D ₄	D ₃	L	H	H	H	H
7	D ₁	H	L	D ₂	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	L	H	H	H
8	D ₀	H	L	D ₁	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	L	H	H
9	X	H	L	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	L	L
10	X	X	L	X	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	L	L
	X	X	H	X	H	NC	NC	NC	NC	NC	NC	NC	NC	NC

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Don't Care
 NC = No Change

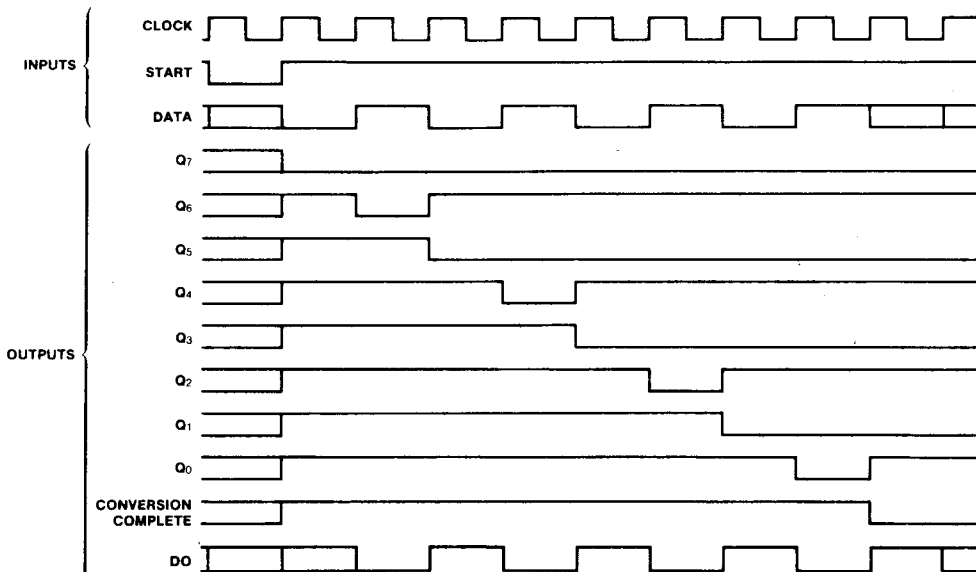
Note: Truth Table for 25(L)04 is extended to include 12 outputs.

USER NOTES FOR A/D CONVERSION

- The register can be used with current switches which are either active high or active low. If active low current switches are used, the resulting digital output from the register is active LOW. That is, a logic "1" is represented as a low voltage level. If active high current switches are used then the digital output is active HIGH; a logic "1" is represented as a high voltage level.
- For a maximum digital error of $\pm 1/2$ LSB the comparator must be biased. If active high current switches are used, the comparator should be biased $+1/2$ LSB and if the current switches are active low, the comparator must be biased $-1/2$ LSB.
- The register, by suitable selection of resistor ladder network, can be used to perform either binary or BCD conversion.
- The register can also be used to perform 2's complement conversion by offsetting the comparator $1/2$ full range $+1/2$ LSB and using the complement of the MSB Q₇(11) as the sign bit.
- If the register is truncated and operated in the continuous conversion mode a lock-up condition may occur on power-on. This situation can be overcome by making the START input the OR function of \overline{CC} and the appropriate register output.



AM25(L)02/3 TIMING CHART

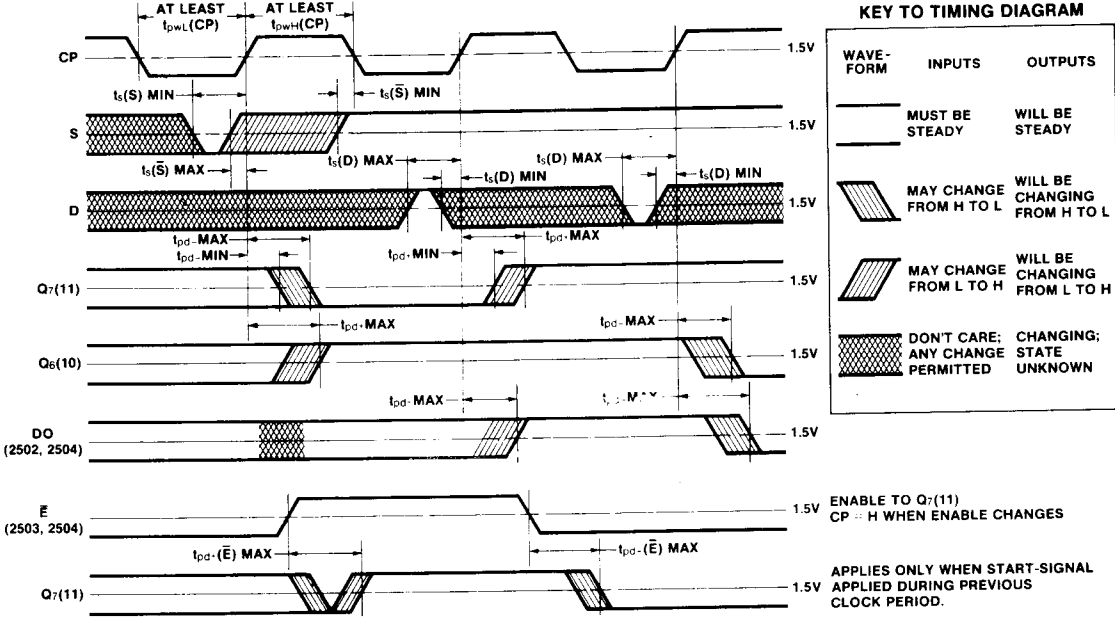


Note: Arbitrary Conversion shown. Timing chart for AM25(L)04 is extended to include 12 outputs, starting with Q₁₁.

AM2502/3/4, AM25L02/3/4

INTERSiL

SWITCHING TIME WAVEFORMS



WAVE-FORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN

DEFINITION OF TERMS

SUBSCRIPT TERMS:

H—HIGH, applying to a HIGH logic level or when used with V_{CC} to indicate high V_{CC} value.

I—Input.

L—LOW, applying to LOW logic level or when used with V_{CC} to indicate low V_{CC} value.

O—Output.

FUNCTIONAL TERMS:

Fan-Out—The logic HIGH or LOW output drive capability in terms of Input Unit Loads.

Input Unit Load—One T2L gate input load. In the HIGH state it is equal to I_{IH} and in the LOW state it is equal to I_{IL} .

CP—The clock input of the register.

CC—The conversion complete output. This output remains HIGH during a conversion and goes LOW when a conversion is complete.

D—The serial data input of the register.

E—The register enable. This input is used to expand the length of the register and when HIGH forces the $Q_7(11)$ register output HIGH and inhibits conversion. When not used for expansion the enable is held at a LOW logic level (Ground).

Q7(11)—The true output of the MSB of the register.

Q7(11)—The complement output of the MSB of the register.

Q_i, i = 7(11) to 0—The outputs of the register.

S—The start input. If the start input is held LOW for at least a clock period the register will be reset to $Q_7(11)$ LOW and all the remaining outputs HIGH. A start pulse that is LOW for a shorter period of time can be used if it meets the set-up time requirements of the S input.

DO—The serial data output. (The D input delayed one bit.)

OPERATIONAL TERMS:

I_{IL}—Forward input load current.

I_{OH}—Output HIGH current, forced out of the output V_{OH} test.

I_{OL}—Output LOW current, forced into the output in V_{OL} test.

I_{IH}—Reverse input load current.

Negative Current—Current flowing out of the device.

Positive Current—Current flowing into the device.

V_{IH}—Minimum logic HIGH input voltage.

V_{IL}—Maximum logic LOW input voltage.

V_{OH}—Minimum logic HIGH output voltage with output HIGH current I_{OH} flowing out of output.

V_{OL}—Maximum logic LOW output voltage with output LOW current I_{OL} flowing into output.

SWITCHING TERMS: (Measured at the 1.5V logic level.)

t_{pd-}—The propagation delay from the clock signal LOW-HIGH transition to an output signal HIGH-LOW transition.

t_{pd+}—The propagation delay from the clock signal LOW-HIGH transition to an output signal LOW-HIGH transition.

t_{pd-(E)}—The propagation delay from the Enable signal HIGH-LOW transition to the $Q_7(11)$ output signal HIGH-LOW transition.

t_{pd-(E)}—The propagation delay from the Enable signal LOW-HIGH transition to $Q_7(11)$ output signal LOW-HIGH transition.

t_{s(D)}—Set-up time required for the logic level to be present at the data input prior to the clock transition from LOW to HIGH in order for the register to respond. The data input should remain steady between t_s max, and t_s min, before the clock.

t_{s(S)}—Set-up time required for a LOW level to be present at the S input prior to the clock transition from LOW to HIGH in order for the register to be reset, or time required for a HIGH level to be present on S before the HIGH to LOW clock transition to prevent resetting.

t_{pw(CP)}—The minimum clock pulse width (LOW or HIGH) required for proper register operation.

