OBSOLETE PRODUCT
NO RECOMMENDED REPLACEMENT

October 2002 FN0561.4

FM IF System

Description

Intersil CA3089 is a monolithic integrated circuit that provides all the functions of a comprehensive FM-IF system. The block diagram shows the CA3089 features, which include a three-stage FM-IF amplifier/limiter configuration with level detectors for each stage, a doubly-balanced quadrature FM detector and an audio amplifier that features the optional use of a muting (squelch) circuit.

The advanced circuit design of the IF system includes desirable deluxe features such as delayed AGC for the RF tuner, and AFC drive circuit, and an output signal to drive a tuning meter and/or provide stereo switching logic. In addition, internal power supply regulators maintain a nearly constant current drain over the voltage supply range of +8.5V to +16V.

The CA3089 is ideal for high-fidelity operation. Distortion in a CA3089 FM-IF System is primarily a function of the phase linearity characteristic of the outboard detector coil.

Part Number Information

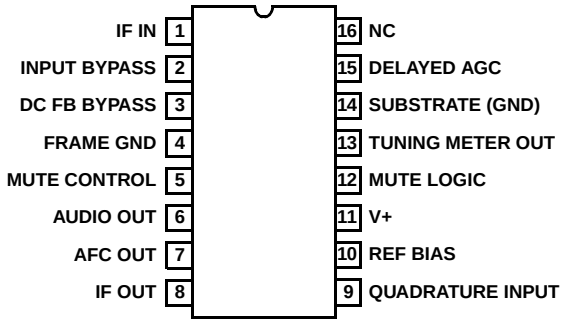
PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
CA3089E	-40 to 85	16 Ld PDIP	E16.3
CA3089M1 (3089M)	-40 to 85	20 Ld SOIC	M20.3

Features

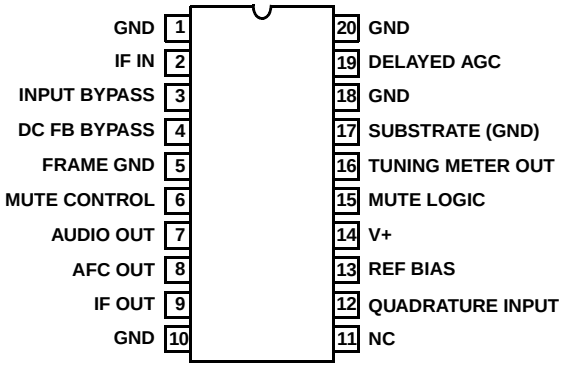
- For FM IF Amplifier Applications in High-Fidelity, Automotive, and Communications Receivers
- Includes: IF Amplifier, Quadrature Detector, AF Preamplifier, and Specific Circuits for AGC, AFC, Muting (Squelch), and Tuning Meter
- Exceptional Limiting Sensitivity at -3dB Point. . . . . 12µV (Typ)
- Low Distortion: (with Double-Tuned Coil) . . . . . 0.1% (Typ)
- Single-Coil Tuning Capability
- High Recovered Audio . . . . . .400mV (Typ)
- Provides Specific Signal for Control of Interchannel Muting (Squelch)
- Provides Specific Signal for Direct Drive of a Tuning Meter
- Provides Delayed AGC Voltage for RF Amplifier
- Provides a Specific Circuit for Flexible AFC
- Internal Supply-Voltage Regulators

Pinouts

CA3089
(PDIP)
TOP VIEW



CA3089
(SOIC)
TOP VIEW



Absolute Maximum Ratings

Supply Voltage
- Between V+ and Frame GND 16V
- Between V+ and Substrate GND 16V

DC Current (Out of Delayed AGC) 2mA

Operating Conditions

Temperature Range . . . . . -40^oC to 85^oC

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^oC/W$)
PDIP Package	90
SOIC Package	95

Maximum Junction Temperature (Plastic Package) . . . . . 150^oC

Maximum Storage Temperature Range . . . . . -65^oC to 150^oC

Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications V+ = 12V (See Figures 3 and 4)

(NOTE 3) PARAMETER		TEST CONDITIONS		TEMP. (^oC)	MIN	TYP	MAX	UNITS
DC CHARACTERISTICS								
Quiescent Circuit Current		No signal input, Non muted		25	16	23	30	mA
DC Voltages	Terminal 1 (IF Input)			25	1.2	1.9	2.4	V
	Terminal 2 (AC Return to Input)			25	1.2	1.9	2.4	V
	Terminal 3 (DC Bias to Input)			25	1.2	1.9	2.4	V
	Terminal 6 (Audio Output)			25	5.0	5.6	6.0	V
	Terminal 10 (DC Reference)			25	5.0	5.6	6.0	V
DYNAMIC CHARACTERISTICS								
Input Limiting Voltage (-3dB point), V_1 (lim)		-	f_O = 10.7MHz, f_{MOD} = 400Hz, Deviation = ±75kHz	25	-	12	25	µV
AM Rejection (Terminal 6), AMR		V_{IN} = 0.1V, AM Mod. = 30%		25	45	55	-	dB
Recovered AF Voltage (Terminal 6) V_O (AF)		V_{IN} = 0.1V		25	300	400	500	mV
Total Harmonic Distortion, THD (Note 2)	Single Tuned (Terminal 6)			25	-	0.5	1.0	%
	Double Tuned (Terminal 6)			25	-	0.1	-	%
Signal Plus Noise to Noise Ratio (Terminal 6)				25	60	67	-	dB

NOTES:

2. THD characteristics are essentially a function of the phase characteristics of the network connected between Terminals 8, 9, and 10.
3. Terminal numbers refer to 16 Lead PDIP.

Application Information

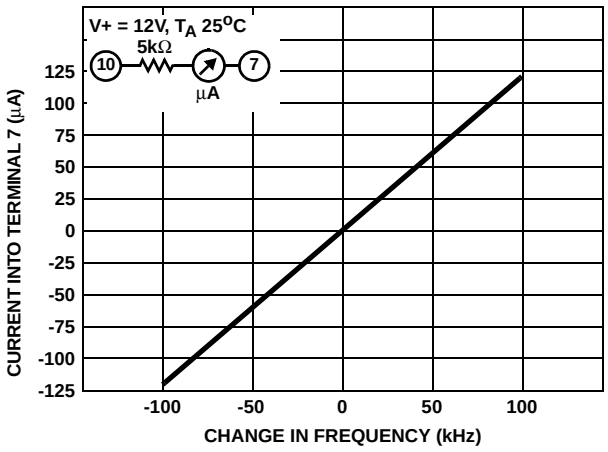


FIGURE 1. AFC CHARACTERISTICS (CURRENT AT TERMINAL 7) vs CHANGE IN FREQUENCY. (SEE TEST CIRCUIT FIGURE 3)

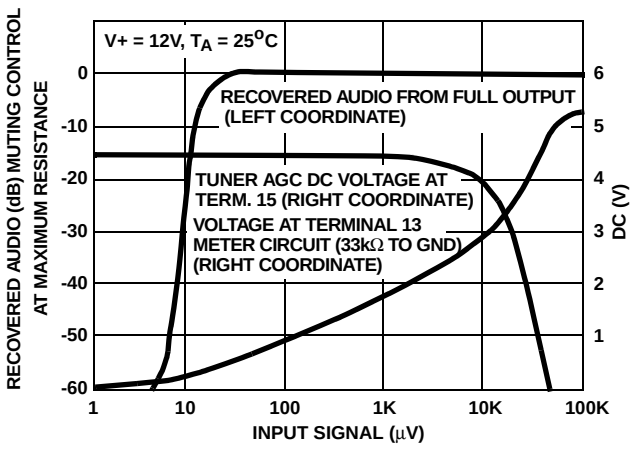
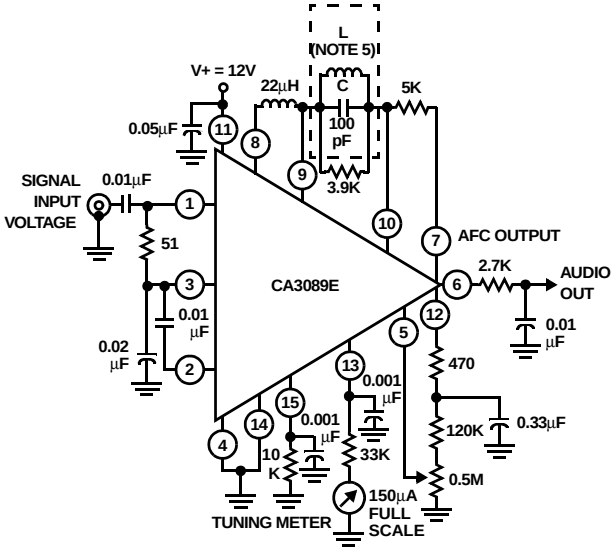


FIGURE 2. MUTING ACTION, TUNER AGC, AND TUNING METER OUTPUT vs INPUT SIGNAL VOLTAGE. (SEE TEST CIRCUIT FIGURE 3)

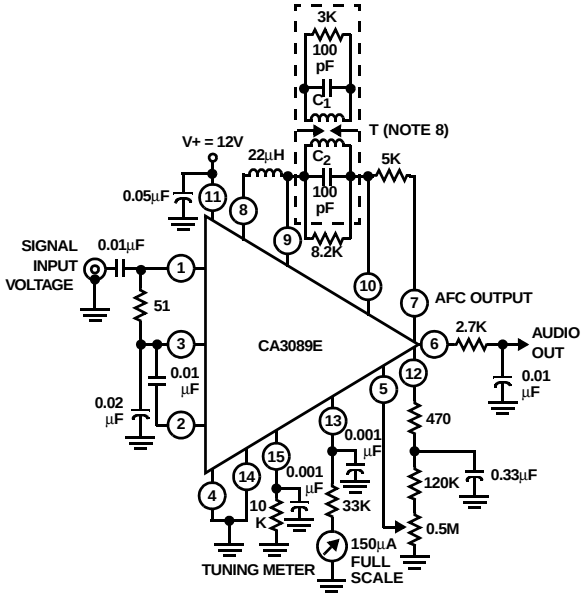
Test Circuits



NOTES:

4. All resistance values are in ohms.
5. L tunes with 100pF (C) at 10.7MHz.
6. Q_0 (unloaded) ≅ 75 (G.I. Automatic Mfg. Div. EX22741 or equivalent)

FIGURE 3. TEST CIRCUIT FOR CA3089E USING A SINGLE-TUNED DETECTOR COIL

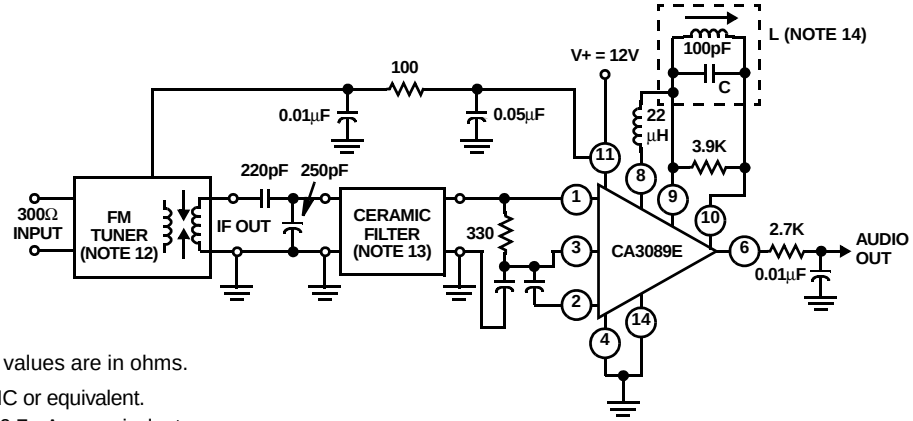


NOTES:

7. All resistance values are in ohms.
8. T PRI. - Q_0 (unloaded) ≅ 75 (tunes with 100pF (C_1) 20↑ of 34e on $^7/_{32}$" dia. form).
9. SEC. - Q_0 (unloaded) ≅ 75 (tunes with 100pF (C_2) 20↑ of 34e on $^7/_{32}$" dia. form).
10. kQ (percent of critical coupling) ≅ 70%.
    (Adjusted for coil voltage V_C) = 150mV.
    Above values permit proper operation of mute (squelch) circuit "E" type slugs, spacing 4mm.

FIGURE 4. TEST CIRCUIT FOR CA3089E USING A DOUBLE-TUNED DETECTOR COIL

Test Applications



NOTES:

11. All resistance values are in ohms.
12. Waller 4SN3FIC or equivalent.
13. Murata SFG 10.7mA or equivalent.
14. L tunes with 100pF (C) at 10.7MHz Q_0 unloaded ≅ 75 (G.I. EX22741 or equivalent).

Performance Data at f_O = 98MHz, f_{MOD} = 400Hz, Deviation = ±75kHz:

-3dB Limiting Sensitivity . . . . . 2µV (Antenna Level)
20dB Quieting Sensitivity . . . . . 1µV (Antenna Level)
30dB Quieting Sensitivity . . . . . .1.5µV (Antenna Level)

FIGURE 5. TYPICAL FM TUNER USING THE CA3089E WITH A SINGLE TUNED DETECTOR COIL

Test Applications (Continued)

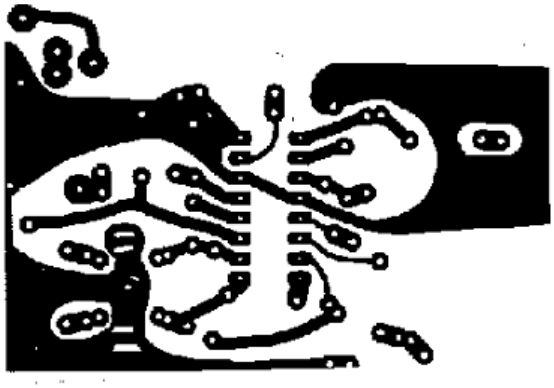


FIGURE 6A. BOTTOM VIEW OF PRINTED CIRCUIT BOARD

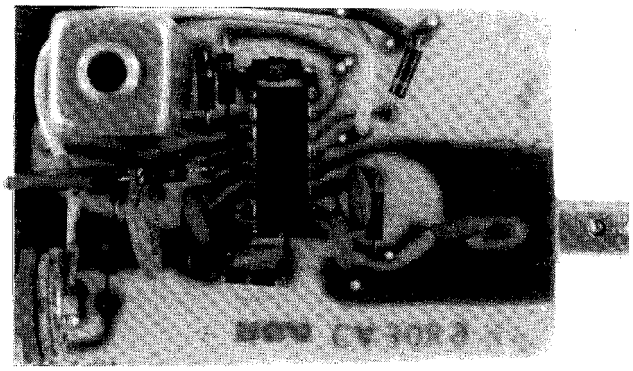
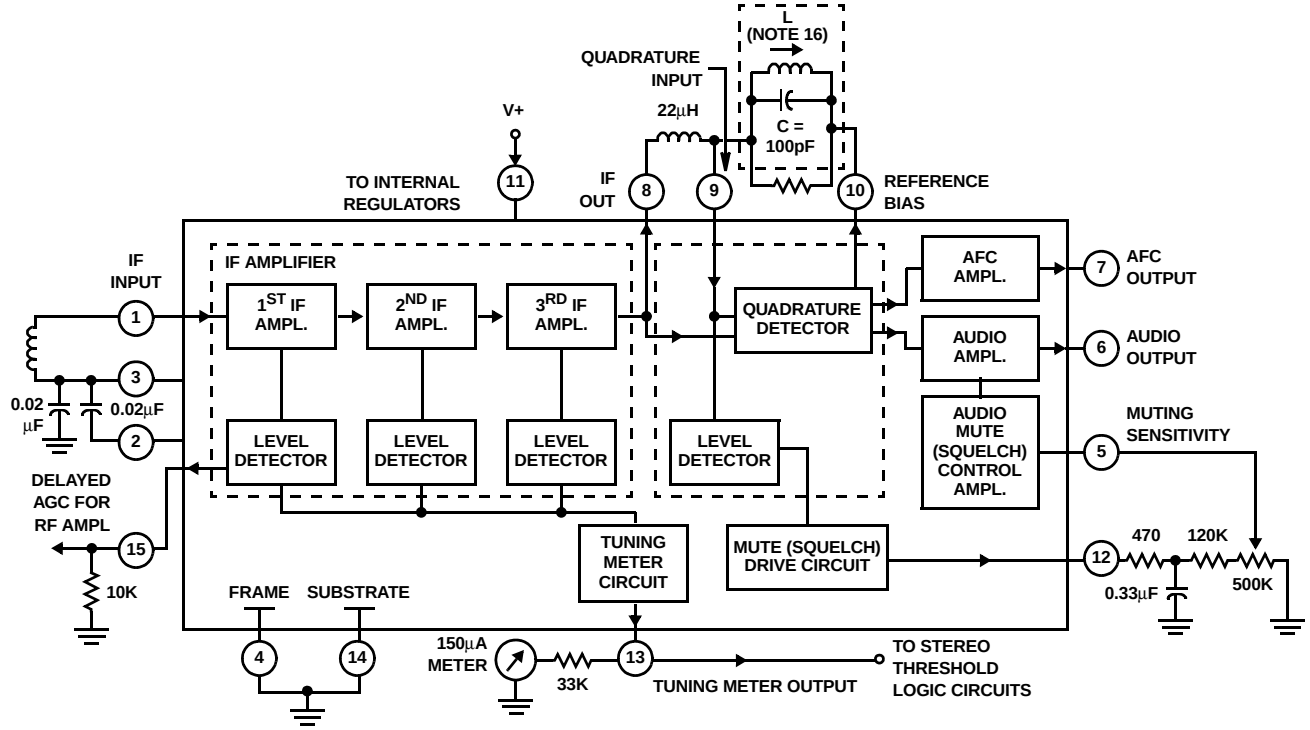


FIGURE 6B. COMPONENT SIDE - TOP VIEW

FIGURE 6. ACTUAL SIZE PHOTOGRAPHS OF THE CA3089E AND OUTBOARD COMPONENTS MOUNTED ON A PRINTED-CIRCUIT BOARD

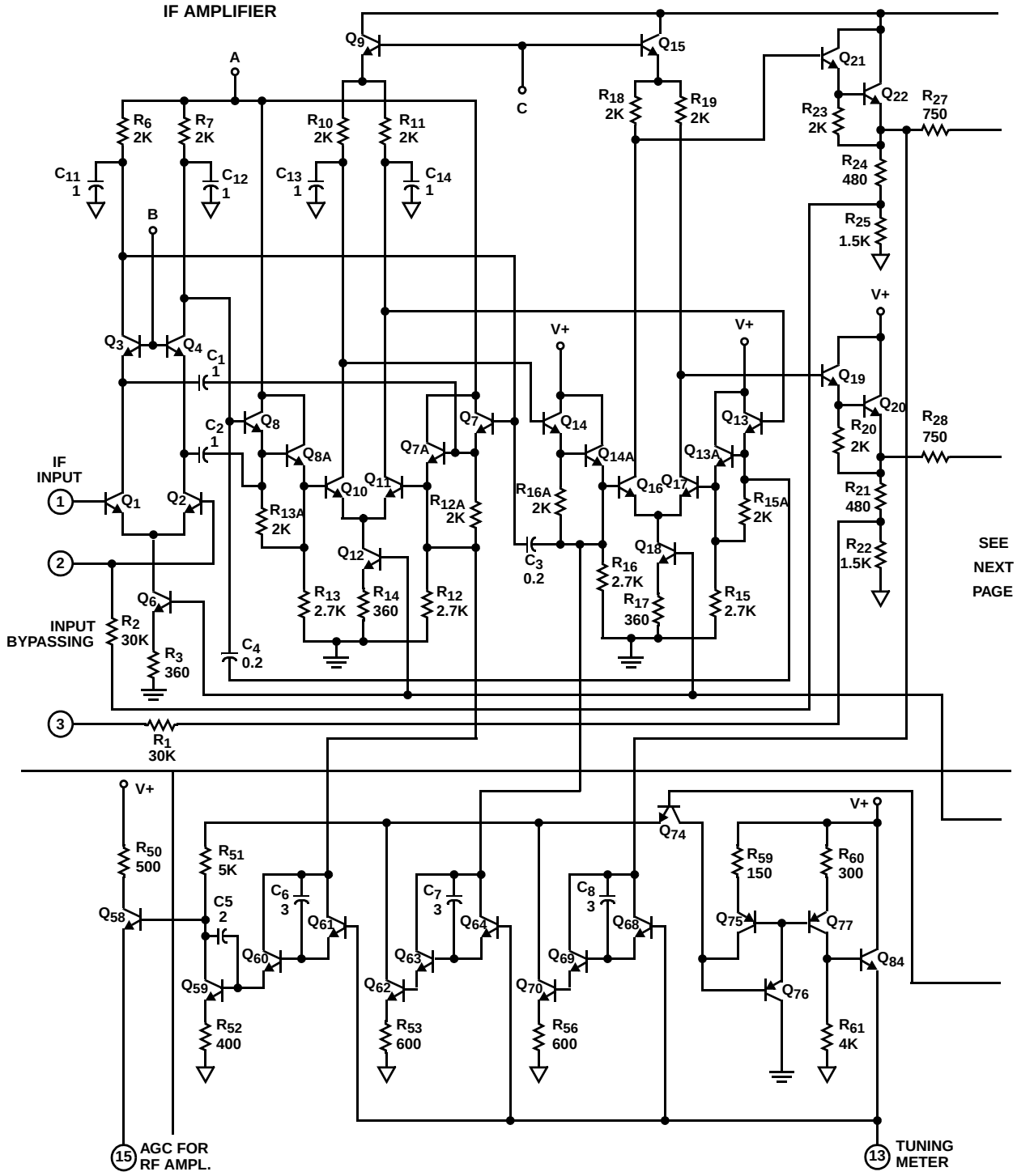
Block Diagram



NOTES:

15. All resistance values are in ohms.
16. L Tunes with 100pF (C) at 10.7MHz.
17. QO @ 75 (G.I. EX22741 or equivalent).
18. Pin numbers refer to 16 lead DIP.

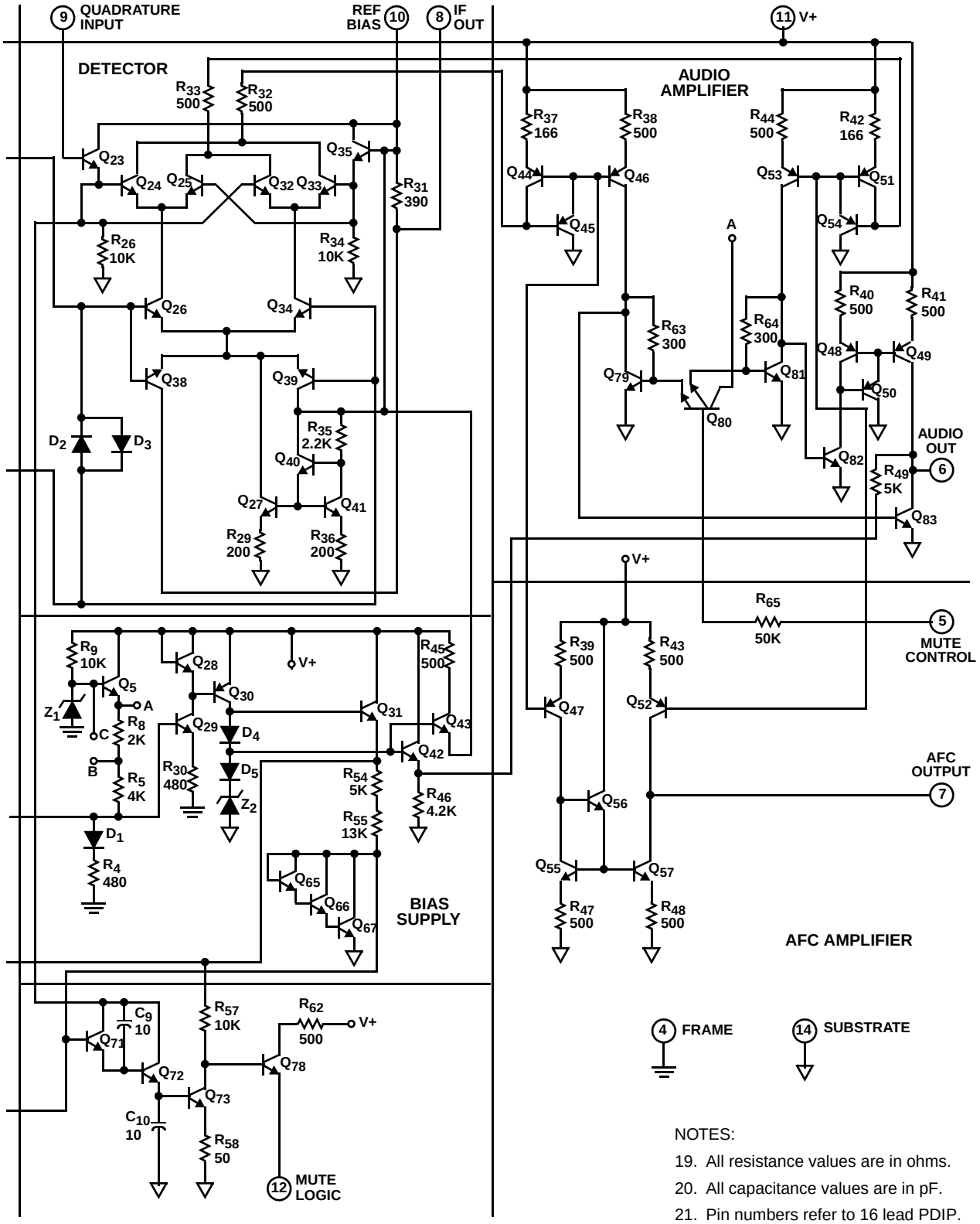
Schematic Diagram



NOTE: Pin numbers refer to 16 lead PDIP.

LEVEL DETECTOR AND METER CIRCUIT

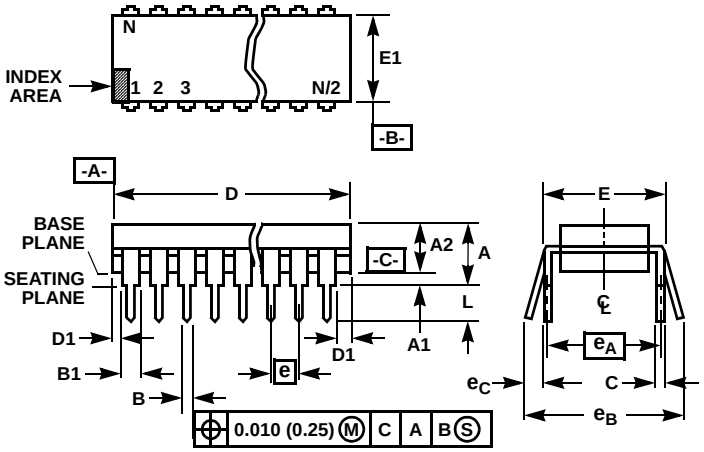
Schematic Diagram (Continued)



NOTES:

19. All resistance values are in ohms.
20. All capacitance values are in pF.
21. Pin numbers refer to 16 lead PDIP.

Dual-In-Line Plastic Packages (PDIP)



NOTES:

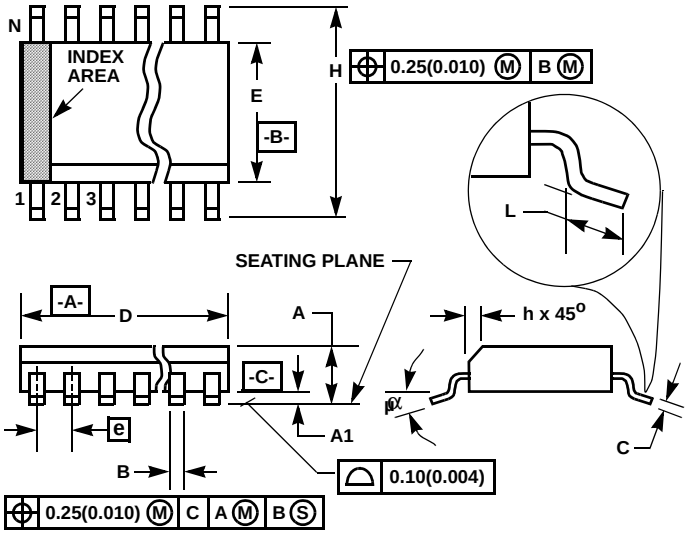
1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E16.3 (JEDEC MS-001-BB ISSUE D)
16 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8, 10
C	0.008	0.014	0.204	0.355	-
D	0.735	0.775	18.66	19.68	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	16		16		9

Rev. 0 12/93

Small Outline Plastic Packages (SOIC)



NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

M20.3 (JEDEC MS-013-AC ISSUE C)
20 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.0200	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.4961	0.5118	12.60	13.00	3
E	0.2914	0.2992	7.40	7.60	4
e	0.050 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.010	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	20		20		7
α	0^o	8^o	0^o	8^o	-

Rev. 0 12/93