

CMOS Dual 4-Stage Static Shift Register With Serial Input/Parallel Output

December 1992

Features

- High-Voltage Type (20V Rating)
- Medium Speed Operation 12MHz (typ.) Clock Rate at VDD - VSS = 10V
- Fully Static Operation
- 8 Master-Slave Flip-Flops Plus Input and Output Buffering
- 100% Tested For Quiescent Current at 20V
- 5V, 10V and 15V Parametric Ratings
- Standardized Symmetrical Output Characteristics
- Maximum Input Current of 1 μ A at 18V Over Full Package-Temperature Range; 100nA at 18V and 25°C
- Noise Margin (Full Package-Temperature Range) =
 - 1V at VDD = 5V
 - 2V at VDD = 10V
 - 2.5V at VDD = 15V
- Meets All Requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications

- Serial-Input/Parallel-Output Data Queueing
- Serial to Parallel Data Conversion
- General-Purpose Register

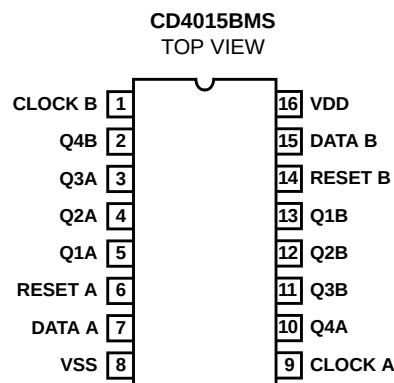
Description

CD4015BMS consists of two identical, independent, 4-stage serial-input/parallel output registers. Each register has independent CLOCK and RESET inputs as well as a single serial DATA input. "Q" outputs are available from each of the four stages on both registers. All register stages are D type, master-slave flip-flops. The logic level present at the DATA input is transferred into the first register stage and shifted over one stage at each positive-going clock transition. Resetting of all stages is accomplished by a high level on the reset line. Register expansion to 8 stages using one CD4015BMS package, or to more than 8 stages using additional CD4015BMS's is possible.

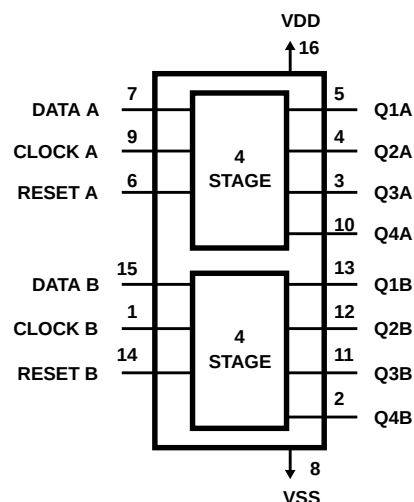
The CD4015BMS is supplied in these 16 lead outline packages:

Braze Seal DIP	H4X
Frit Seal DIP	H1F
Ceramic Flatpack	H6W

Pinout



Functional Diagram



Specifications CD4015BMS

Absolute Maximum Ratings

DC Supply Voltage Range, (VDD) -0.5V to +20V
 (Voltage Referenced to VSS Terminals)
 Input Voltage Range, All Inputs -0.5V to VDD +0.5V
 DC Input Current, Any One Input $\pm 10\text{mA}$
 Operating Temperature Range -55°C to $+125^{\circ}\text{C}$
 Package Types D, F, K, H
 Storage Temperature Range (TSTG) -65°C to $+150^{\circ}\text{C}$
 Lead Temperature (During Soldering) $+265^{\circ}\text{C}$
 At Distance $1/16 \pm 1/32$ Inch ($1.59\text{mm} \pm 0.79\text{mm}$) from case for
 10s Maximum

Reliability Information

Thermal Resistance θ_{ja} θ_{jc}
 Ceramic DIP and FRIT Package 80°C/W 20°C/W
 Flatpack Package 70°C/W 20°C/W
 Maximum Package Power Dissipation (PD) at $+125^{\circ}\text{C}$
 For TA = -55°C to $+100^{\circ}\text{C}$ (Package Type D, F, K) 500mW
 For TA = $+100^{\circ}\text{C}$ to $+125^{\circ}\text{C}$ (Package Type D, F, K) Derate
 Linearity at $12\text{mW}/^{\circ}\text{C}$ to 200mW
 Device Dissipation per Output Transistor 100mW
 For TA = Full Package Temperature Range (All Package Types)
 Junction Temperature $+175^{\circ}\text{C}$

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
						MIN	MAX	
Supply Current	IDD	VDD = 20V, VIN = VDD or GND		1	$+25^{\circ}\text{C}$	-	10	μA
				2	$+125^{\circ}\text{C}$	-	1000	μA
		VDD = 18V, VIN = VDD or GND		3	-55°C	-	10	μA
Input Leakage Current	IIL	VIN = VDD or GND	VDD = 20	1	$+25^{\circ}\text{C}$	-100	-	nA
				2	$+125^{\circ}\text{C}$	-1000	-	nA
			VDD = 18V	3	-55°C	-100	-	nA
Input Leakage Current	IIH	VIN = VDD or GND	VDD = 20	1	$+25^{\circ}\text{C}$	-	100	nA
				2	$+125^{\circ}\text{C}$	-	1000	nA
			VDD = 18V	3	-55°C	-	100	nA
Output Voltage	VOL15	VDD = 15V, No Load		1, 2, 3	$+25^{\circ}\text{C}$, $+125^{\circ}\text{C}$, -55°C	-	50	mV
Output Voltage	VOH15	VDD = 15V, No Load (Note 3)		1, 2, 3	$+25^{\circ}\text{C}$, $+125^{\circ}\text{C}$, -55°C	14.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V		1	$+25^{\circ}\text{C}$	0.53	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V		1	$+25^{\circ}\text{C}$	1.4	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V		1	$+25^{\circ}\text{C}$	3.5	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V		1	$+25^{\circ}\text{C}$	-	-0.53	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V		1	$+25^{\circ}\text{C}$	-	-1.8	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V		1	$+25^{\circ}\text{C}$	-	-1.4	mA
Output Current (Source)	IOH15	VDD = 15V, VOUT = 13.5V		1	$+25^{\circ}\text{C}$	-	-3.5	mA
N Threshold Voltage	VNTH	VDD = 10V, ISS = $-10\mu\text{A}$		1	$+25^{\circ}\text{C}$	-2.8	-0.7	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = $10\mu\text{A}$		1	$+25^{\circ}\text{C}$	0.7	2.8	V
Functional	F	VDD = 2.8V, VIN = VDD or GND		7	$+25^{\circ}\text{C}$	VOH > VDD/2	VOL < VDD/2	V
		VDD = 20V, VIN = VDD or GND		7	$+25^{\circ}\text{C}$			
		VDD = 18V, VIN = VDD or GND		8A	$+125^{\circ}\text{C}$			
		VDD = 3V, VIN = VDD or GND		8B	-55°C			
Input Voltage Low (Note 2)	VIL	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	$+25^{\circ}\text{C}$, $+125^{\circ}\text{C}$, -55°C	-	1.5	V
Input Voltage High (Note 2)	VIH	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	$+25^{\circ}\text{C}$, $+125^{\circ}\text{C}$, -55°C	3.5	-	V
Input Voltage Low (Note 2)	VIL	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	$+25^{\circ}\text{C}$, $+125^{\circ}\text{C}$, -55°C	-	4	V
Input Voltage High (Note 2)	VIH	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	$+25^{\circ}\text{C}$, $+125^{\circ}\text{C}$, -55°C	11	-	V

NOTES: 1. All voltages referenced to device GND, 100% testing being implemented.
 2. Go/No Go test with limits applied to inputs
 3. For accuracy, voltage is measured differentially to VDD. Limit is 0.050V max.

Specifications CD4015BMS

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1, 2)	GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Propagation Delay Clock To Q	TPHL1 TPLH1	VDD = 5V, VIN = VDD or GND	9	+25°C	-	320	ns
			10, 11	+125°C, -55°C	-	432	ns
Propagation Delay Reset To Q	TPHL2	VDD = 5V, VIN = VDD or GND	9	+25°C	-	400	ns
			10, 11	+125°C, -55°C	-	540	ns
Transition Time	TTHL TTLH	VDD = 5V, VIN = VDD or GND	9	+25°C	-	200	ns
			10, 11	+125°C, -55°C	-	270	ns
Maximum Clock Input Frequency	FCL	VDD = 5V, VIN = VDD or GND	9	+25°C	3	-	MHz
			10, 11	+125°C, -55°C	3/1.35	-	MHz

NOTES:

1. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
2. -55°C and +125°C limits guaranteed, 100% testing being implemented.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Supply Current	IDD	VDD = 5V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	5	μA
				+125°C	-	150	μA
		VDD = 10V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	10	μA
				+125°C	-	300	μA
		VDD = 15V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	10	μA
				+125°C	-	600	μA
Output Voltage	VOL	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOL	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	4.95	-	V
Output Voltage	VOH	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	9.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V	1, 2	+125°C	0.36	-	mA
				-55°C	0.64	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V	1, 2	+125°C	0.9	-	mA
				-55°C	1.6	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V	1, 2	+125°C	2.4	-	mA
				-55°C	4.2	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V	1, 2	+125°C	-	-0.36	mA
				-55°C	-	-0.64	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V	1, 2	+125°C	-	-1.15	mA
				-55°C	-	-2.0	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V	1, 2	+125°C	-	-0.9	mA
				-55°C	-	-1.6	mA
Output Current (Source)	IOH15	VDD = 15V, VOUT = 13.5V	1, 2	+125°C	-	-2.4	mA
				-55°C	-	-4.2	mA
Input Voltage Low	VIL	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	-	3	V

Specifications CD4015BMS

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Input Voltage High	VIH	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	+7	-	V
Propagation Delay Clock To Q	TPHL1 TPLH1	VDD = 10V	1, 2, 3	+25°C	-	160	ns
		VDD = 15V	1, 2, 3	+25°C	-	120	ns
Propagation Delay Reset To Q	TPHL2	VDD = 10V	1, 2, 3	+25°C	-	200	ns
		VDD = 15V	1, 2, 3	+25°C	-	160	ns
Transition Time	TTHL TTLH	VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	80	ns
Maximum Clock Input Frequency	FCL	VDD = 10V	1, 2, 3	+25°C	6	-	MHz
		VDD = 15V	1, 2, 3	+25°C	8.5	-	MHz
Minimum Data Setup Time	TS	VDD = 5V	1, 2, 3	+25°C	-	70	ns
		VDD = 10V	1, 2, 3	+25°C	-	40	ns
		VDD = 15V	1, 2, 3	+25°C	-	30	ns
Clock Rise and Fall Time	TRCL TFCL	VDD = 5V	1, 2, 3	+25°C	-	15	μs
		VDD = 10V	1, 2, 3	+25°C	-	15	μs
		VDD = 15V	1, 2, 3	+25°C	-	15	μs
Minimum Clock Pulse Width	TWCL	VDD = 5V	1, 2, 3	+25°C	-	180	ns
		VDD = 10V	1, 2, 3	+25°C	-	80	ns
		VDD = 15V	1, 2, 3	+25°C	-	50	ns
Minimum Reset Pulse Width	TWR	VDD = 5V	2, 3	+25°C	-	200	ns
		VDD = 10V	2, 3	+25°C	-	80	ns
		VDD = 15V	2, 3	+25°C	-	60	ns
Input Capacitance	CIN	Any Input	1, 2	+25°C	-	7.5	pF

NOTES:

1. All voltages referenced to device GND.
2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.
3. CL = 50pF, RL = 200K, Input TR, TF < 20ns.

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1, 4	+25°C	-	25	μA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10μA	1, 4	+25°C	-2.8	-0.2	V
N Threshold Voltage Delta	ΔVNTH	VDD = 10V, ISS = -10μA	1, 4	+25°C	-	±1	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10μA	1, 4	+25°C	0.2	2.8	V
P Threshold Voltage Delta	ΔVPTH	VSS = 0V, IDD = 10μA	1, 4	+25°C	-	±1	V
Functional	F	VDD = 18V, VIN = VDD or GND	1	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 3V, VIN = VDD or GND					
Propagation Delay Time	TPHL TPLH	VDD = 5V	1, 2, 3, 4	+25°C	-	1.35 x +25°C Limit	ns

NOTES: 1. All voltages referenced to device GND.

2. CL = 50pF, RL = 200K, Input TR, TF < 20ns.

3. See Table 2 for +25°C limit.

4. Read and Record

Specifications CD4015BMS

TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25°C

PARAMETER	SYMBOL	DELTA LIMIT
Supply Current - MSI-2	IDD	± 1.0μA
Output Current (Sink)	IOL5	± 20% x Pre-Test Reading
Output Current (Source)	IOH5A	± 20% x Pre-Test Reading

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP		MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 1 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 2 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Interim Test 3 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Final Test		100% 5004	2, 3, 8A, 8B, 10, 11	
Group A		Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample 5005	1, 7, 9	
Group D		Sample 5005	1, 2, 3, 8A, 8B, 9	Subgroups 1, 2 3

NOTE: 1. 5% Parametric, 3% Functional; Cumulative for Static 1 and 2.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	MIL-STD-883 METHOD	TEST		READ AND RECORD	
		PRE-IRRAD	POST-IRRAD	PRE-IRRAD	POST-IRRAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4

TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V	OSCILLATOR	
					50kHz	25kHz
Static Burn-In 1 Note 1	2 - 5, 10 - 13	1, 6 - 9, 14, 15	16			
Static Burn-In 2 Note 1	2 - 5, 10 - 13	8	1, 6, 7, 9, 14 - 16			
Dynamic Burn-In Note 1	-	6, 8, 14	16	2 - 5, 10 - 13	1, 9	7, 15
Irradiation Note 2	2 - 5, 10 - 13	8	1, 6, 7, 9, 14 - 16			

NOTE:

- Each pin except VDD and GND will have a series resistor of 10K ± 5%, VDD = 18V ± 0.5V
- Each pin except VDD and GND will have a series resistor of 47K ± 5%; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, VDD = 10V ± 0.5V

Specifications CD4015BMS

Logic Diagram

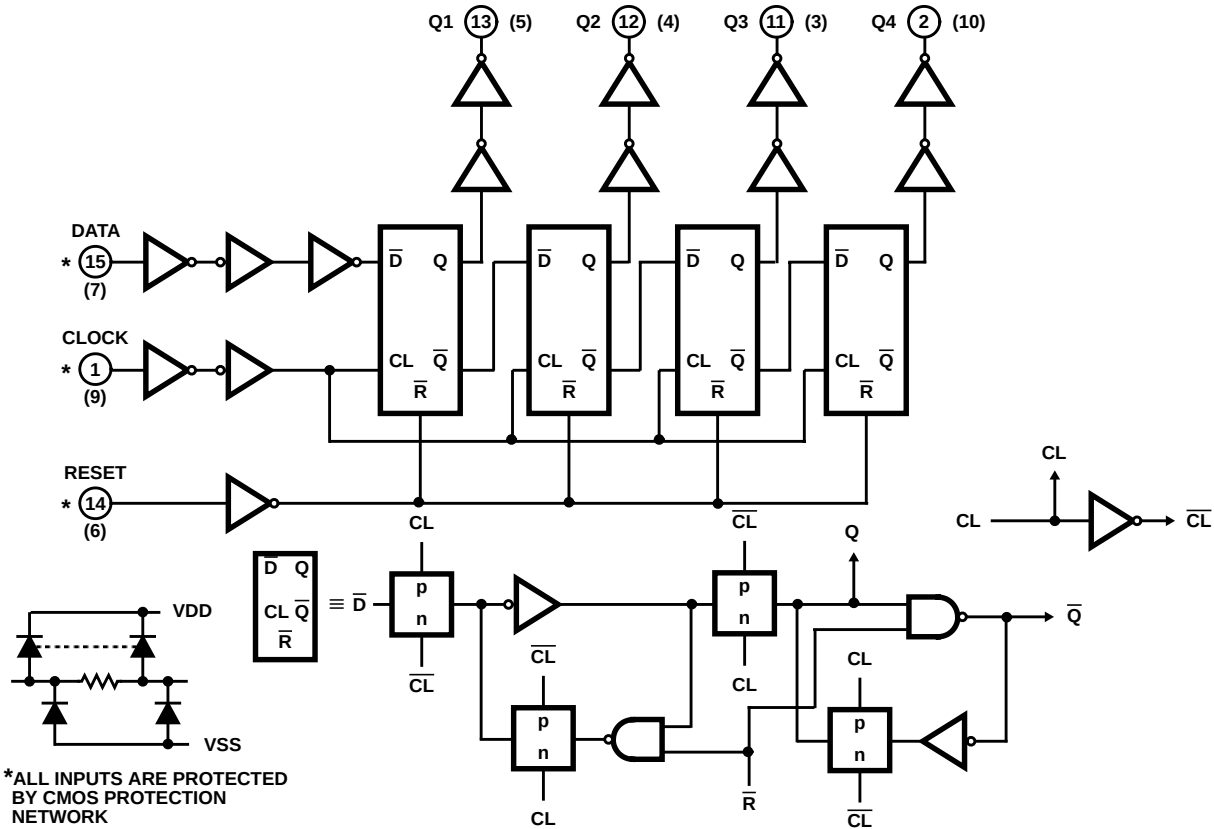


FIGURE 1. CD4015BMS LOGIC DIAGRAM

TRUTH TABLE

CL	D	R	Q1	Qn
	0	0	0	Qn-1
	1	0	1	Qn-1
	X	0	Q1	Qn
X	X	1	0	0

(No Change)

X = Don't care Case

All Intersil semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.

Intersil products are sold by description only. Intersil Corporation reserves the right to make changes in circuit design and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.

For information regarding Intersil Corporation and its products, see web site <http://www.intersil.com>

Sales Office Headquarters

NORTH AMERICA
Intersil Corporation
P. O. Box 883, Mail Stop 53-204
Melbourne, FL 32902
TEL: (321) 724-7000
FAX: (321) 724-7240

EUROPE
Intersil SA
Mercure Center
100, Rue de la Fusee
1130 Brussels, Belgium
TEL: (32) 2.724.2111
FAX: (32) 2.724.22.05

ASIA
Intersil (Taiwan) Ltd.
Taiwan Limited
7F-6, No. 101 Fu Hsing North Road
Taipei, Taiwan
Republic of China
TEL: (886) 2 2716 9310
FAX: (886) 2 2715 3029

Typical Performance Characteristics

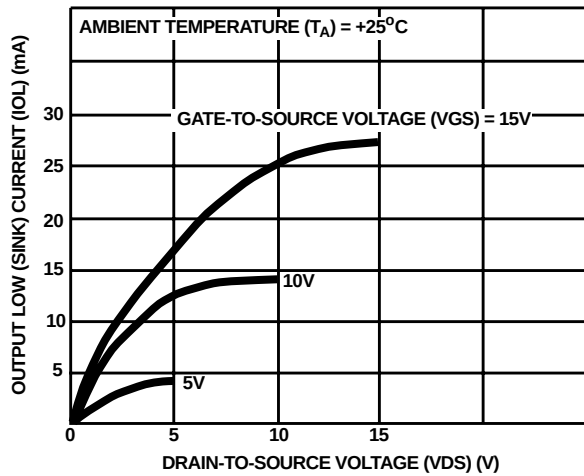


FIGURE 2. TYPICAL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

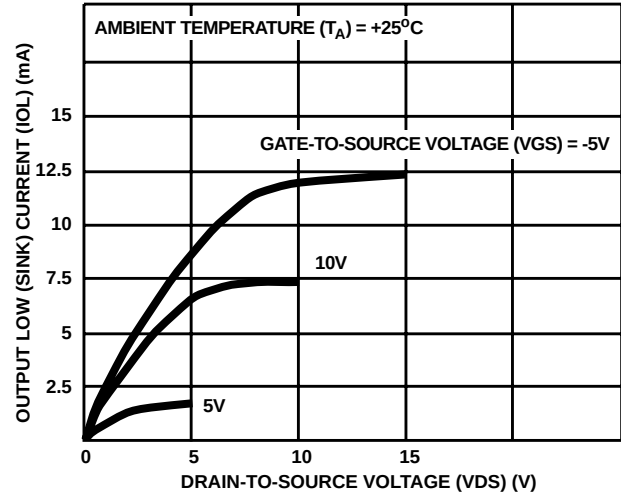


FIGURE 3. MINIMUM OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

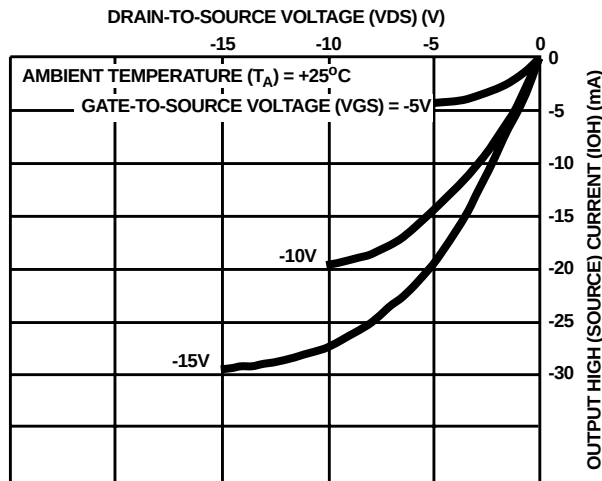


FIGURE 4. TYPICAL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

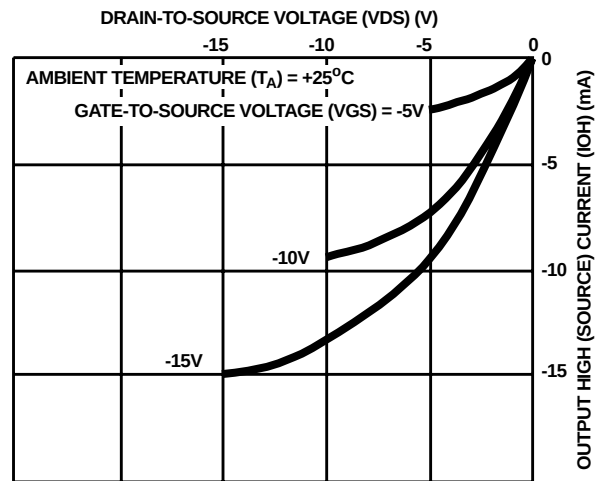


FIGURE 5. MINIMUM OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

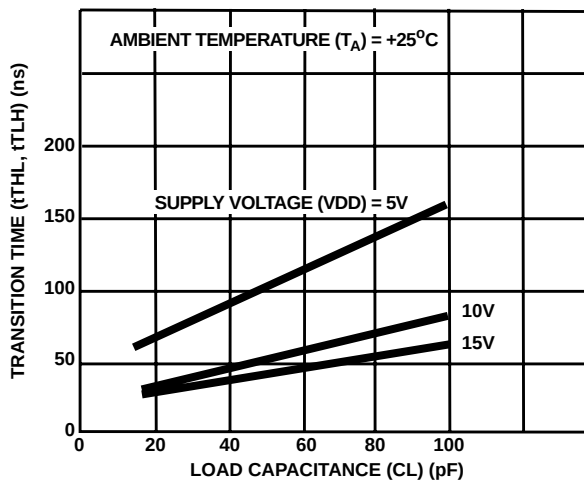


FIGURE 6. TYPICAL TRANSITION TIME AS A FUNCTION OF LOAD CAPACITANCE

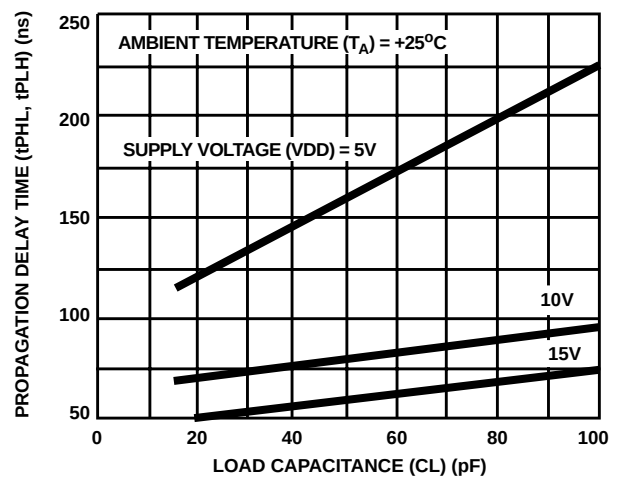


FIGURE 7. TYPICAL PROPAGATION DELAY TIME AS A FUNCTION OF LOAD CAPACITANCE

Typical Performance Characteristics (Continued)

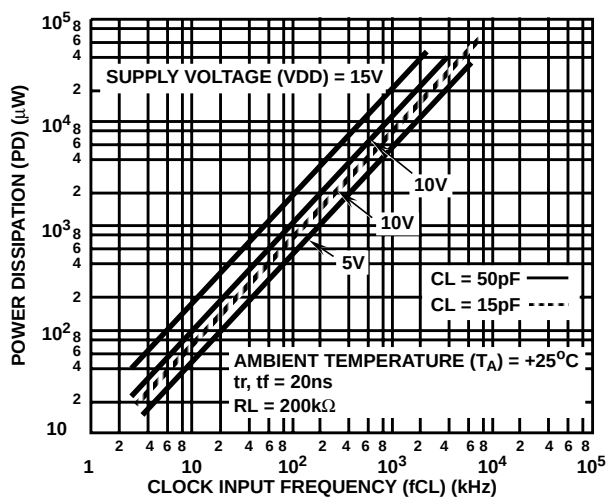
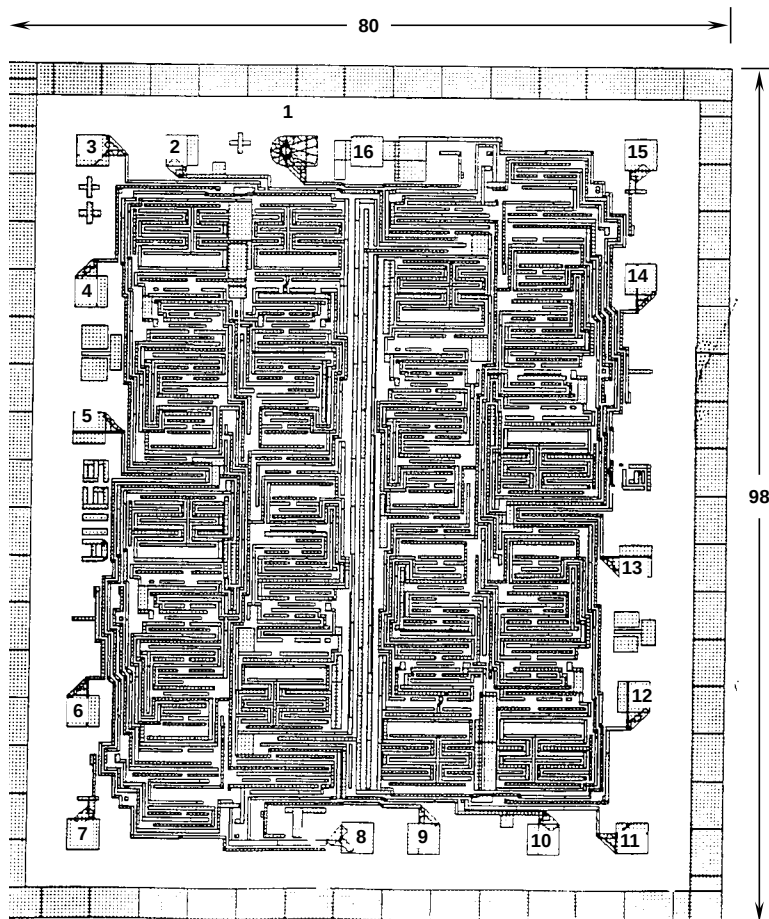


FIGURE 8. TYPICAL POWER DISSIPATION AS A FUNCTION OF FREQUENCY

Chip Dimensions and Pad Layout



METALLIZATION: Thickness: $11\text{k}\text{\AA} - 14\text{k}\text{\AA}$, AL.

PASSIVATION: $10.4\text{k}\text{\AA} - 15.6\text{k}\text{\AA}$, Silane

BOND PADS: 0.004 inches X 0.004 inches MIN

DIE THICKNESS: 0.0198 inches - 0.0218 inches

DIE SIZE: X = 80 (77 - 85) = (1.956 - 2.159)

Y = 98 (95 - 103) = (2.413 - 2.616)

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch)