Data Sheet June 1999 File Number 3116.5

Single 16-Channel/Differential 8-Channel, CMOS Analog Multiplexers

The DG406 and DG407 monolithic CMOS analog multiplexers are drop-in replacements for the popular DG506A and DG507A series devices. They each include an array of sixteen analog switches, a TTL and CMOS compatible digital decode circuit for channel selection, a voltage reference for logic thresholds, and an ENABLE input for device selection when several multiplexers are present.

These multiplexers feature lower signal ON resistance (<100Ω) and faster transition time (t_{TRANS} < 300ns) compared to the DG506A and DG507A. Charge injection has been reduced, simplifying sample and hold applications.

The improvements in the DG406 series are made possible by using a high voltage silicon-gate process. An epitaxial layer prevents the latch-up associated with older CMOS technologies. The 44V maximum voltage range permits controlling $30V_{P-P}$ signals when operating with ±15V power supplies.

The sixteen switches are bilateral, equally matched for AC or bidirectional signals. The ON resistance variation with analog signals is quite low over a ±5V analog input range.

Features

- ON-Resistance (Max) 100Ω
- Low Power Consumption (P_D) . . . . . <1.2mW
- Fast Transition Time (Max) 300ns
- Low Charge Injection
- TTL, CMOS Compatible
- Single or Split Supply Operation

Applications

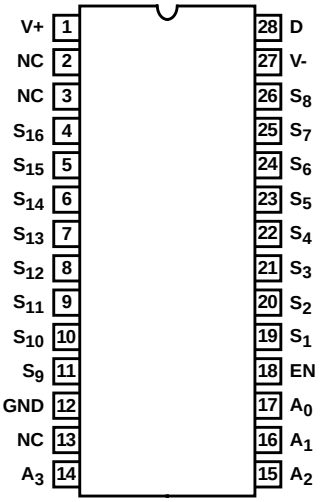
- Battery Operated Systems
- Data Acquisition
- Medical Instrumentation
- Hi-Rel Systems
- Communication Systems
- Automatic Test Equipment

Ordering Information

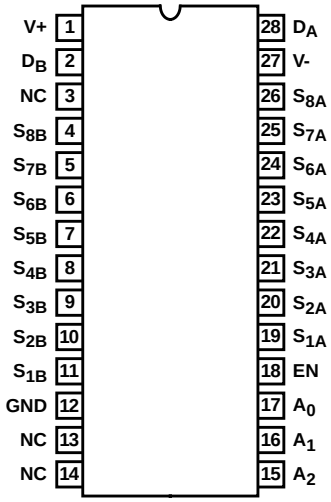
PART NUMBER	TEMP. RANGE (^oC)	PACKAGE	PKG. NO.
DG406DJ	-40 to 85	28 Ld PDIP	E28.6
DG406DY	-40 to 85	28 Ld SOIC	M28.3
DG407DJ	-40 to 85	28 Ld PDIP	E28.6
DG407DY	-40 to 85	28 Ld SOIC	M28.3
DG407DN	-40 to 85	28 Ld PLCC	N28.45

Pinouts

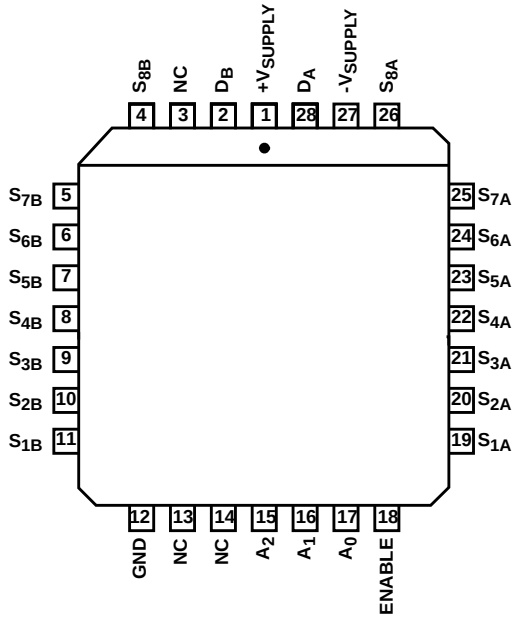
DG406 (PDIP, SOIC)
TOP VIEW



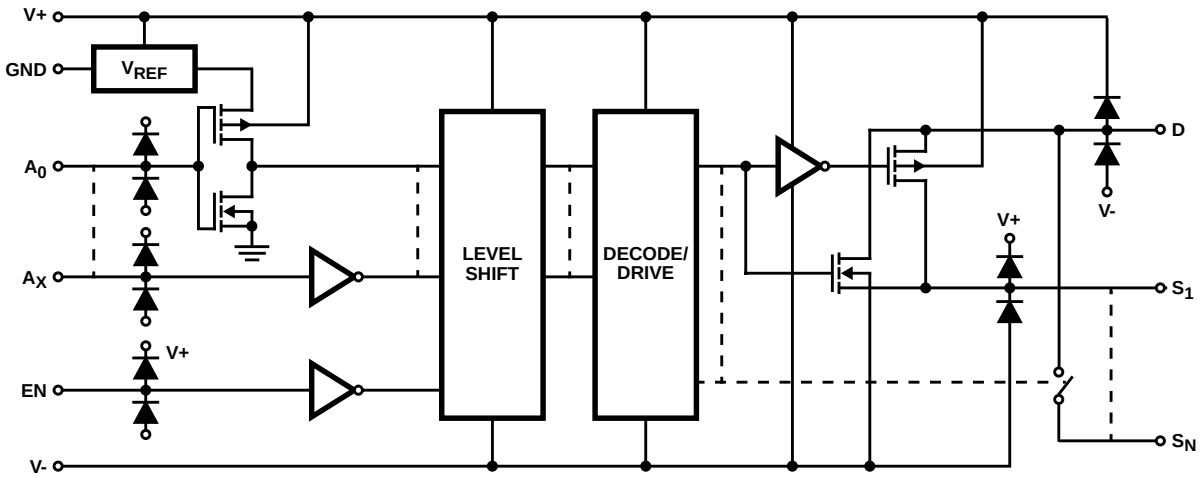
DG407 (PDIP, SOIC)
TOP VIEW



DG407 (PLCC)
TOP VIEW

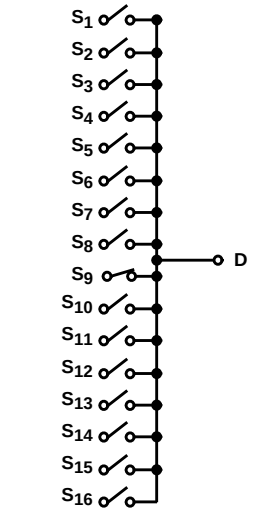


Schematic Diagram (Typical Channel)

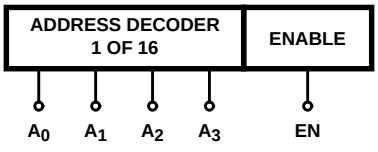


Functional Diagrams

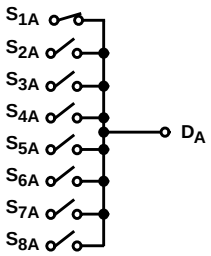
DG406

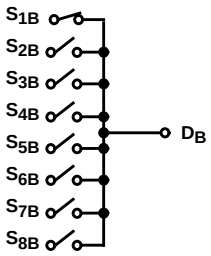


TO DECODER LOGIC CONTROLLING BOTH TIERS OF MUXING

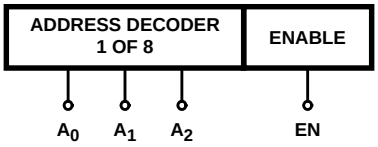


DG407





TO DECODER LOGIC CONTROLLING BOTH TIERS OF MUXING



DG406 TRUTH TABLE

A_3	A_2	A_1	A_0	EN	ON SWITCH
X	X	X	X	0	None
0	0	0	0	1	1
0	0	0	1	1	2
0	0	1	0	1	3
0	0	1	1	1	4
0	1	0	0	1	5
0	1	0	1	1	6
0	1	1	0	1	7
0	1	1	1	1	8
1	0	0	0	1	9
1	0	0	1	1	10
1	0	1	0	1	11
1	0	1	1	1	12
1	1	0	0	1	13
1	1	0	1	1	14
1	1	1	0	1	15
1	1	1	1	1	16

DG407 TRUTH TABLE

A_2	A_1	A_0	EN	ON SWITCH PAIR
X	X	X	0	None
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

Logic “0” = V_{AL} < 0.8V.
Logic “1” = V_{AH} > 2.4V.
X = Don’t Care.

Absolute Maximum Ratings

V+ to V- 44.0V
GND to V-. 25V
Digital Inputs, V_S, V_D (Note 1). . . . . (V-) -2V to (V+) +2V or 20mA, Whichever Occurs First
Continuous Current (Any Terminal) 30mA
Peak Current, S or D (Pulsed 1ms, 10% Duty Cycle Max) 100mA

Operating Conditions

Temperature Range . . . . . -40^oC to 85^oC

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} ($^oC/W$)
PDIP Package	60
SOIC Package	75
PLCC Package	65

Maximum Junction Temperature . . . . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(PLCC and SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Signals on S_X, D_X, EN or A_X exceeding V+ or V- are clamped by internal diodes. Limit diode current to maximum current ratings.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

Test Conditions: V+ = +15V, V- = -15V, V_{AL} = 0.8V, V_{AH} = 2.4V Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP (^oC)	(NOTE 3) MIN	(NOTE 4) TYP	(NOTE 3) MAX	UNITS
DYNAMIC CHARACTERISTICS						
Transition Time, t_{TRANS}	(See Figure 1)	25	-	200	300	ns
		Full	-	-	400	ns
Break-Before-Make Interval, t_{OPEN}	(See Figure 3)	25	25	50	-	ns
		Full	10	-	-	ns
Enable Turn-ON Time, $t_{ON(EN)}$	(See Figure 2)	25	-	150	200	ns
		Full	-	-	400	ns
Enable Turn-OFF Time, $t_{OFF(EN)}$		25	-	70	150	ns
		Full	-	-	300	ns
Charge Injection, Q	C_L = 1nF, V_S = 0V, R_S = 0Ω	25	-	40	-	pC
OFF Isolation, OIRR	V_{EN} = 0V, R_L = 1kΩ, f = 100kHz (Note 7)	25	-	-69	-	dB
Logic Input Capacitance, C_{IN}	f = 1MHz	25	-	7	-	pF
Source OFF Capacitance, $C_{S(OFF)}$	V_{EN} = 0V, V_S = 0V, f = 1MHz	25	-	8	-	pF
Drain OFF Capacitance, $C_{D(OFF)}$ DG406	V_{EN} = 0V, V_D = 0V, f = 1MHz	25	-	160	-	pF
DG407		25	-	80	-	pF
Drain ON Capacitance, $C_{D(ON)}$ DG406	V_{EN} = 5V, V_D = 0V, f = 1MHz	25	-	180	-	pF
DG407		25	-	90	-	pF
DIGITAL INPUT CHARACTERISTICS						
Logic High Input Voltage, V_{INH}		Full	2.4	-	-	V
Logic Low Input Voltage, V_{INL}		Full	-	-	0.8	V
Logic High Input Current, I_{AH}	V_A = 2.4V, 15V	Full	-1	-	1	µA
Logic Low Input Current, I_{AL}	V_{EN} = 0V, 2.4V, V_A = 0V	Full	-1	-	1	µA

Electrical Specifications Test Conditions: V+ = +15V, V- = -15V, V_{AL} = 0.8V, V_{AH} = 2.4V Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP (^{o}C)	(NOTE 3) MIN	(NOTE 4) TYP	(NOTE 3) MAX	UNITS
ANALOG SWITCH CHARACTERISTICS						
Drain-Source ON Resistance, $r_{DS(ON)}$	V_D = ±10V, I_S = ∓10mA (Note 5)	25	-	50	100	Ω
		Full	-	-	125	Ω
$r_{DS(ON)}$ Matching Between Channels, $\Delta r_{DS(ON)}$	V_D = 10V, -10V (Note 6)	25	-	5	-	%
Source OFF Leakage Current, $I_{S(OFF)}$	V_{EN} = 0V, V_S = ±10V, V_D = ∓10V	25	-0.5	0.01	0.5	nA
		Full	-5	-	5	nA
Drain OFF Leakage Current, $I_{D(OFF)}$ DG406		25	-1	0.04	1	nA
		Full	-40	-	40	nA
DG407		25	-1	0.04	1	nA
		Full	-20	-	20	nA
Drain ON Leakage Current, $I_{D(ON)}$ DG406	V_S = V_D = ±10V (Note 5)	25	-1	0.04	1	nA
		Full	-40	-	40	nA
DG407		25	-1	0.04	1	nA
		Full	-20	-	20	nA
POWER SUPPLY CHARACTERISTICS						
Positive Supply Current, I+	V_{EN} = V_A = 0V or 5V (Standby)	25	-	13	30	µA
		Full	-	-	75	µA
Negative Supply Current, I-		25	-1	-0.01	-	µA
		Full	-10	-	-	µA
Positive Supply Current, I+	V_{EN} = 2.4V, V_A = 0V (Enabled)	25	-	-0.01	100	µA
		Full	-	-	200	µA
Negative Supply Current, I-		25	-1	-	-	µA
		Full	-10	-	-	µA

Electrical Specifications Single Supply Test Conditions: V+ = 12V, V- = 0V, V_{AL} = 0.8V, V_{AH} = 2.4V, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP (^{o}C)	(NOTE 3) MIN	(NOTE 4) TYP	(NOTE 3) MAX	UNITS
DYNAMIC CHARACTERISTICS						
Switching Time of Multiplexer, t_{TRANS}	V_{S1} = 8V, V_{S8} = 0V, V_{IN} = 2.4V	25	-	300	450	ns
Enable Turn-ON Time, $t_{ON(EN)}$	V_{INH} = 2.4V, V_{INL} = 0V, V_{S1} = 5V	25	-	250	600	ns
Enable Turn-OFF Time, $t_{OFF(EN)}$		25	-	150	300	ns
Charge Injection, Q	C_L = 1nF, V_S = 6V, R_S = 0Ω	25	-	20	-	pC

Electrical Specifications Single Supply Test Conditions: V+ = 12V, V- = 0V, V_{AL} = 0.8V, V_{AH} = 2.4V, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP (^{O}C)	(NOTE 3) MIN	(NOTE 4) TYP	(NOTE 3) MAX	UNITS
ANALOG SWITCH CHARACTERISTICS						
Analog Signal Range, V_{ANALOG}		Full	0	-	12	V
Drain-Source ON-Resistance, $r_{DS(ON)}$	V_D = 3V, 10V, I_S = -1mA (Note 5)	25	-	90	120	Ω
$r_{DS(ON)}$ Matching Between Channels (Note 6), $\Delta r_{DS(ON)}$		25	-	5	-	%
Source Off Leakage Current, $I_{S(OFF)}$	V_{EN} = 0V, V_D = 10V or 0.5V, V_S = 0.5V or 10V	25	-	0.01	-	nA
Drain Off Leakage Current, $I_{D(OFF)}$						
DG406		25	-	0.04	-	nA
DG407		25	-	0.04	-	nA
Drain On Leakage Current, $I_{D(ON)}$	V_S = V_D = ±10V (Note 5)					
DG406		25	-	0.04	-	nA
DG407		25	-	0.04	-	nA
POWER SUPPLY CHARACTERISTICS						
Positive Supply Current (I+) (Standby)	V_{EN} = 0V or 5V, V_A = 0V or 5V	25	-	13	30	µA
		Full	-	13	75	µA
Negative Supply Current (I-) (Enabled)		25	-1	-0.01	-	µA
		Full	-5	-0.01	-	µA

NOTES:

3. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
4. Typical values are for Design Aid Only, not guaranteed nor production tested.
5. Sequence each switch ON.
6. $\Delta r_{DS(ON)}$ = ($r_{DS(ON)}$(Max) - $r_{DS(ON)}$(Min)) ÷ $r_{DS(ON)}$ average.
7. Worst case isolation occurs on channel 8B due to proximity to the drain pin.

Test Circuits and Waveforms

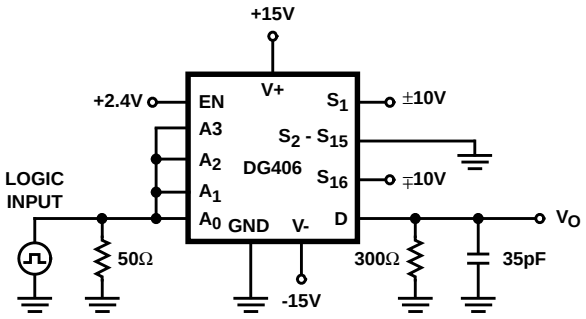


FIGURE 1A. DG406 TEST CIRCUIT

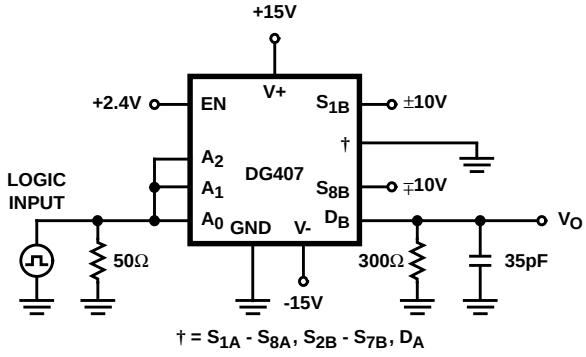


FIGURE 1B. DG407 TEST CIRCUIT

Test Circuits and Waveforms (Continued)

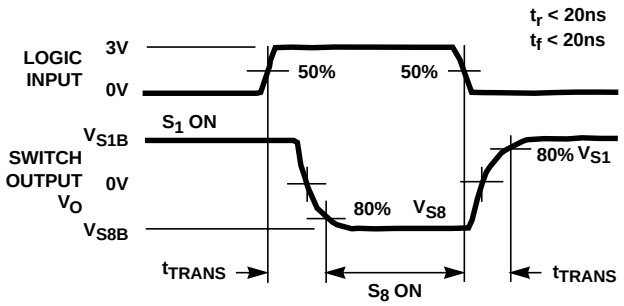


FIGURE 1C. MEASUREMENT POINTS

FIGURE 1. TRANSITION TIME

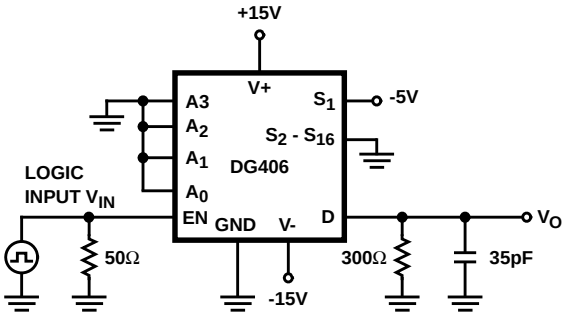


FIGURE 2A. DG406 TEST CIRCUIT

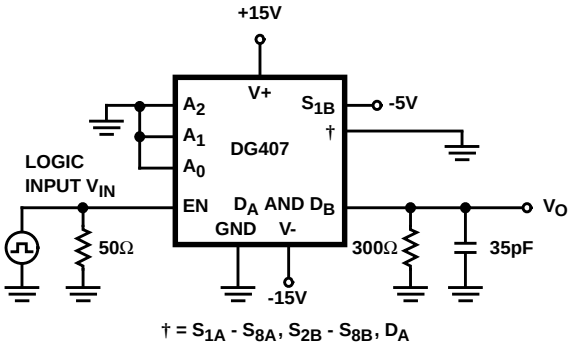


FIGURE 2B. DG407 TEST CIRCUIT

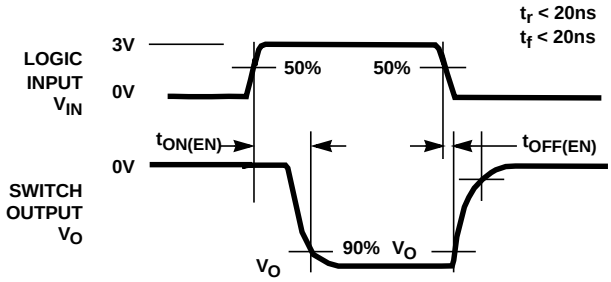


FIGURE 2C. MEASUREMENT POINTS

FIGURE 2. ENABLE SWITCHING TIMES

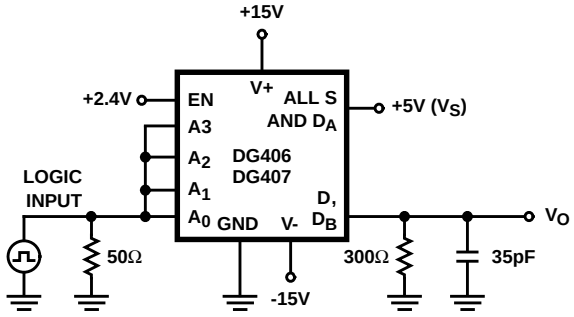


FIGURE 3A. TEST CIRCUIT

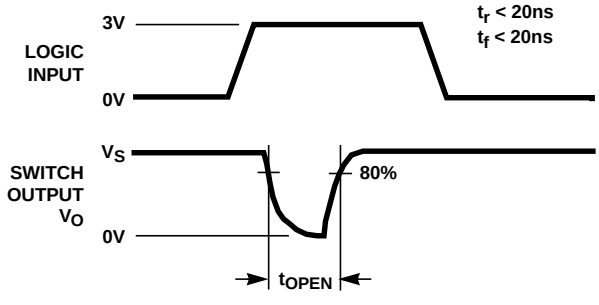


FIGURE 3B. MEASUREMENT POINTS

FIGURE 3. BREAK-BEFORE-MAKE INTERVAL

Typical Performance Curves

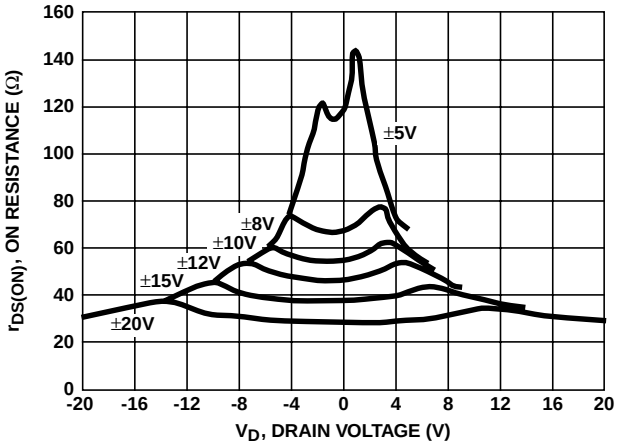


FIGURE 4. $r_{DS(ON)}$ vs V_D AND SUPPLY

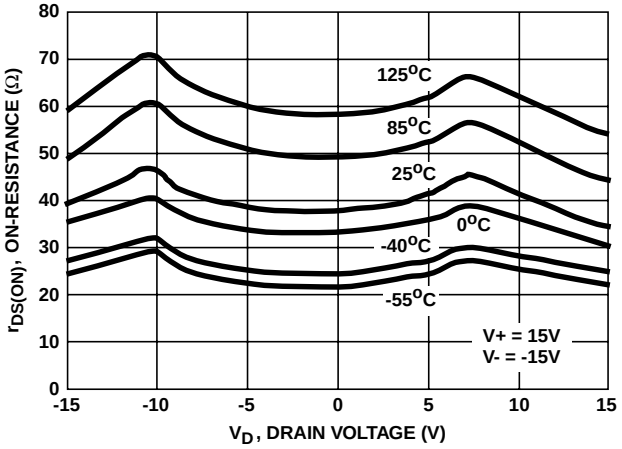


FIGURE 5. $r_{DS(ON)}$ vs V_D AND TEMPERATURE

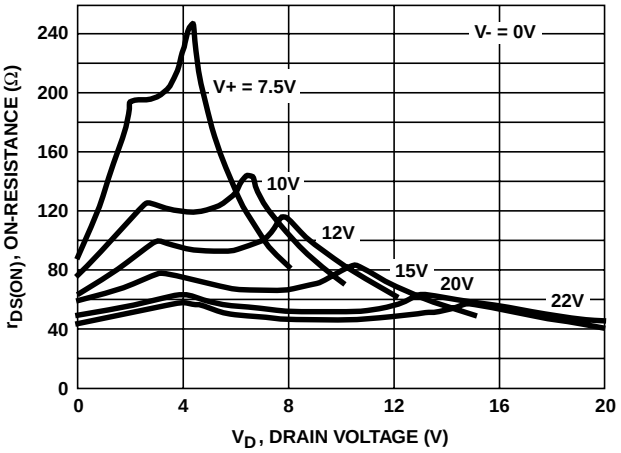


FIGURE 6. $r_{DS(ON)}$ vs V_D AND SUPPLY

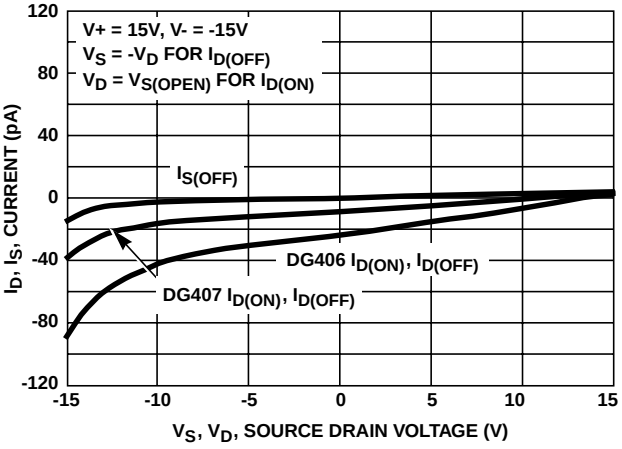


FIGURE 7. I_D, I_S LEAKAGE CURRENTS vs ANALOG VOLTAGE

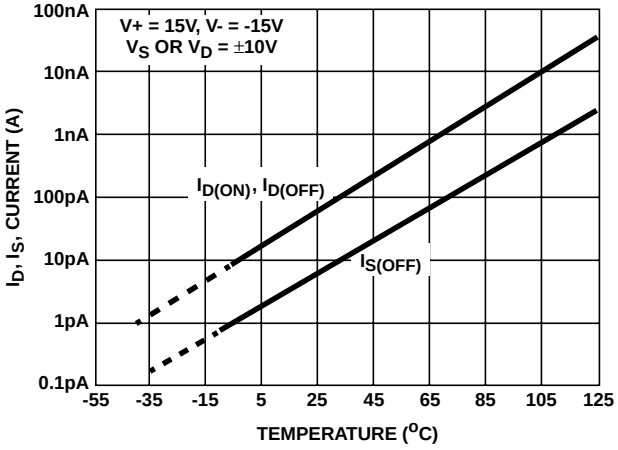


FIGURE 8. I_D, I_S LEAKAGE vs TEMPERATURE

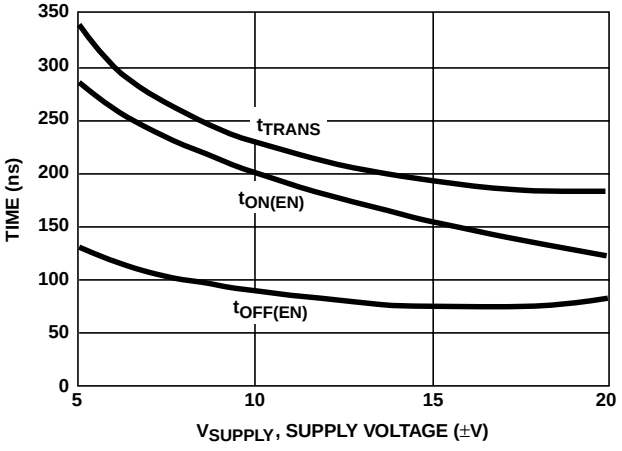


FIGURE 9. SWITCHING TIMES vs BIPOLAR SUPPLIES

Typical Performance Curves (Continued)

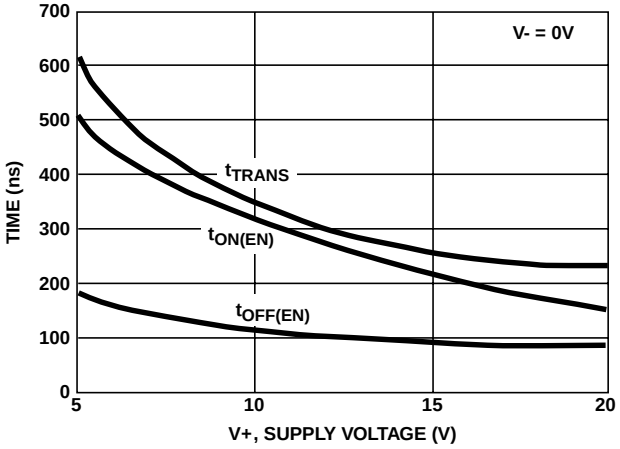


FIGURE 10. SWITCHING TIMES vs SINGLE SUPPLY

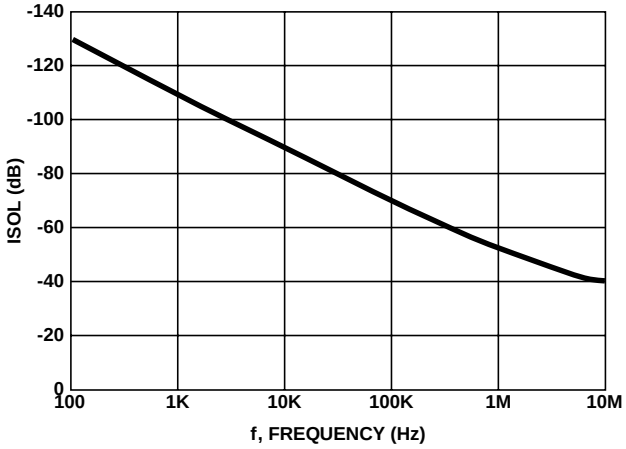


FIGURE 11. OFF ISOLATION vs FREQUENCY

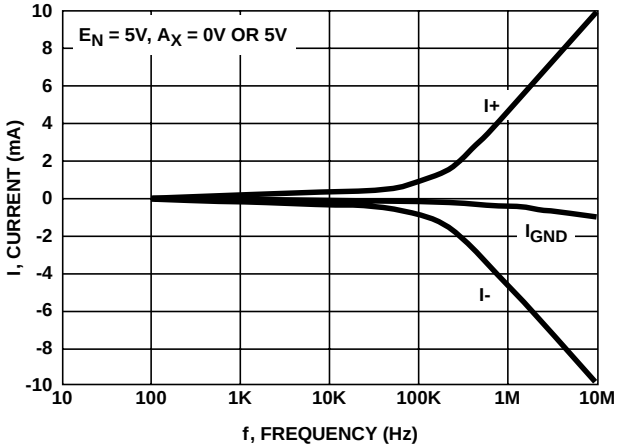


FIGURE 12. SUPPLY CURRENTS vs SWITCHING FREQUENCY

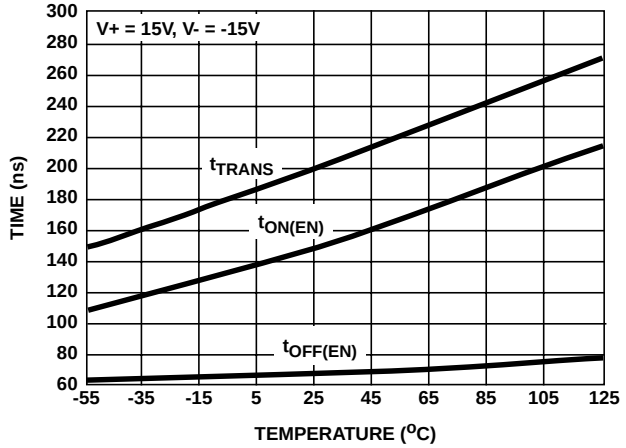


FIGURE 13. t_{ON}/t_{OFF} vs TEMPERATURE

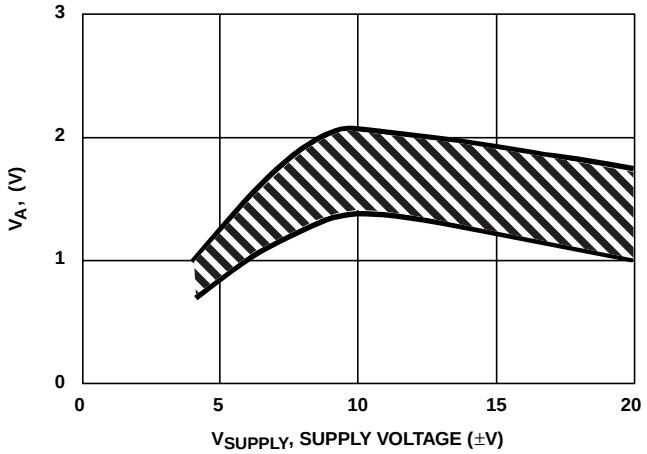


FIGURE 14. SWITCHING THRESHOLD vs SUPPLY VOLTAGE

Die Characteristics

DIE DIMENSIONS:

2490µm x 4560µm x 485µm

METALLIZATION:

Type: SiAl
Thickness: 12kÅ ±1kÅ

PASSIVATION:

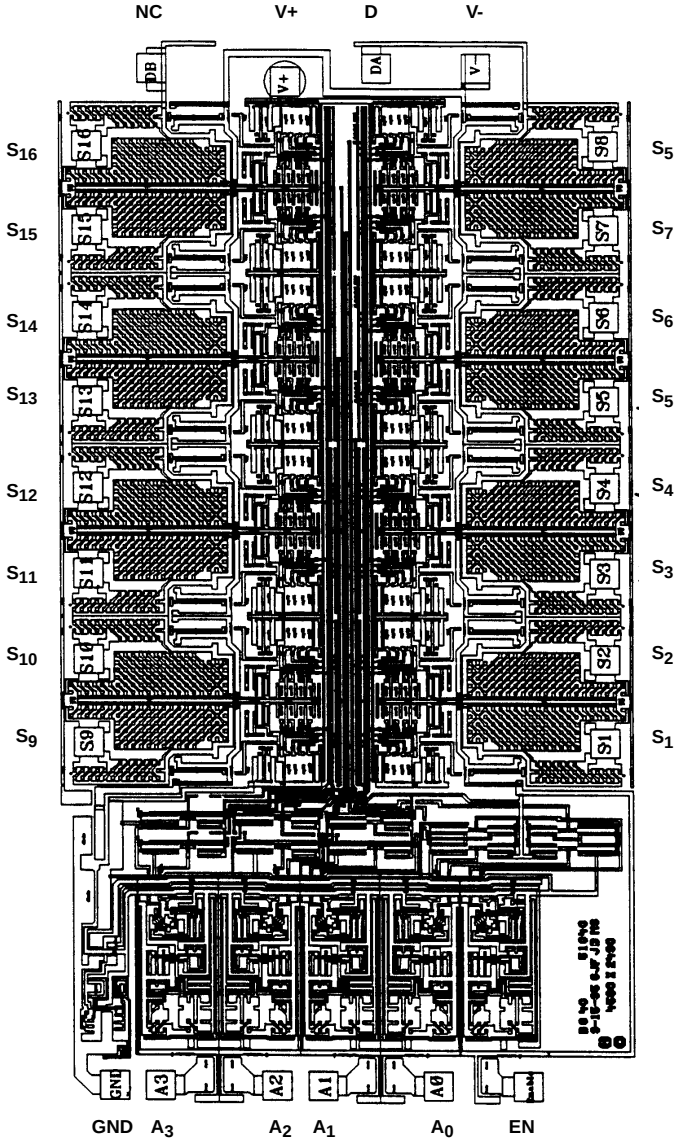
Type: Nitride
Thickness: 8kÅ ±1kÅ

WORST CASE CURRENT DENSITY:

9.1×10^4 A/cm^2

Metallization Mask Layout

DG406



Die Characteristics

DIE DIMENSIONS:

2490µm x 4560µm x 485µm

METALLIZATION:

Type: SiAl
Thickness: 12kÅ ±1kÅ

PASSIVATION:

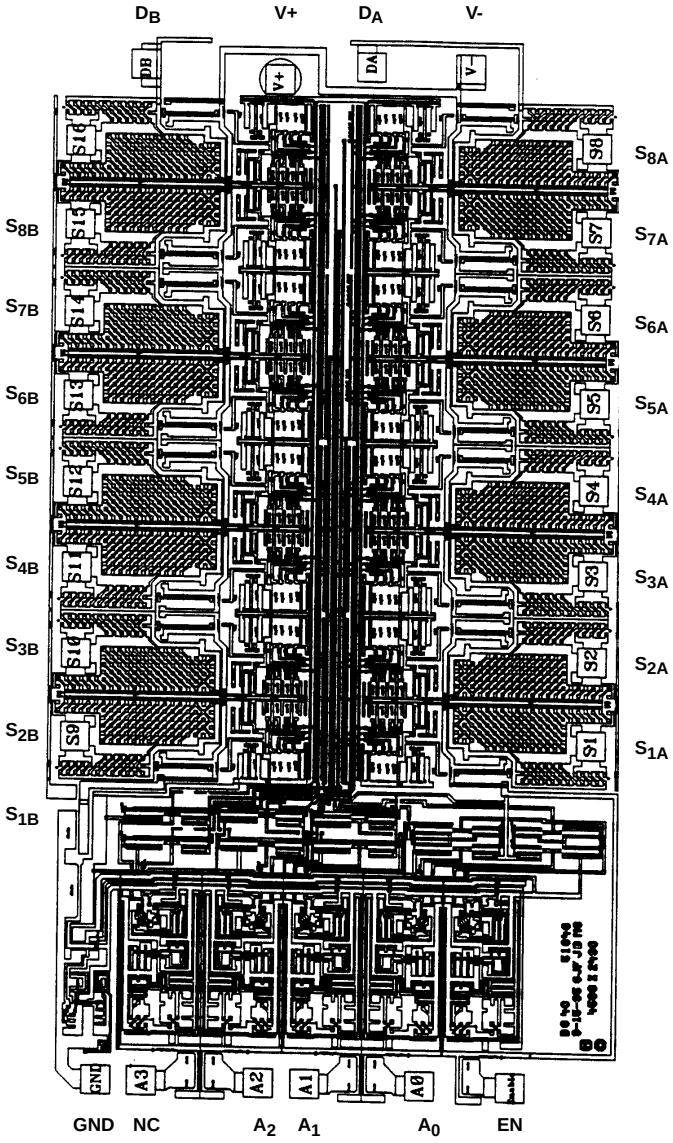
Type: Nitride
Thickness: 8kÅ ±1kÅ

WORST CASE CURRENT DENSITY:

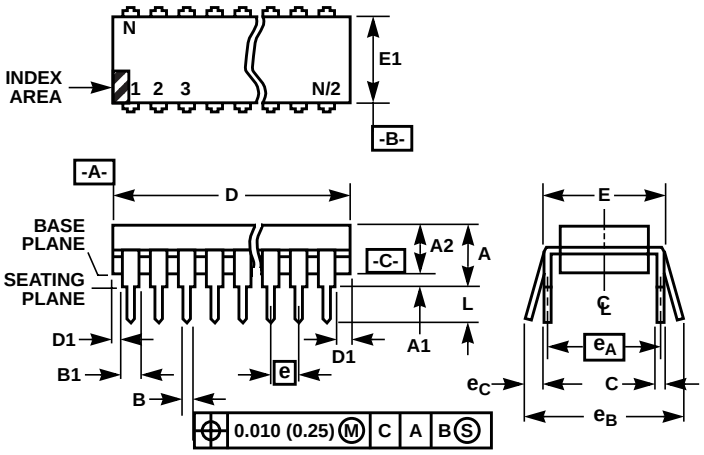
9.1×10^4 A/cm^2

Metallization Mask Layout

DG407



Dual-In-Line Plastic Packages (PDIP)



NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E28.6 (JEDEC MS-001-BF ISSUE D)
28 LEAD NARROW BODY DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.250	-	6.35	4
A1	0.015	-	0.39	-	4
A2	0.125	0.195	3.18	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.030	0.070	0.77	1.77	8
C	0.008	0.015	0.204	0.381	-
D	1.380	1.565	35.1	39.7	5
D1	0.005	-	0.13	-	5
E	0.600	0.625	15.24	15.87	6
E1	0.485	0.580	12.32	14.73	5
e	0.100 BSC		2.54 BSC		-
e_A	0.600 BSC		15.24 BSC		6
e_B	-	0.700	-	17.78	7
L	0.115	0.200	2.93	5.08	4
N	28		28		9

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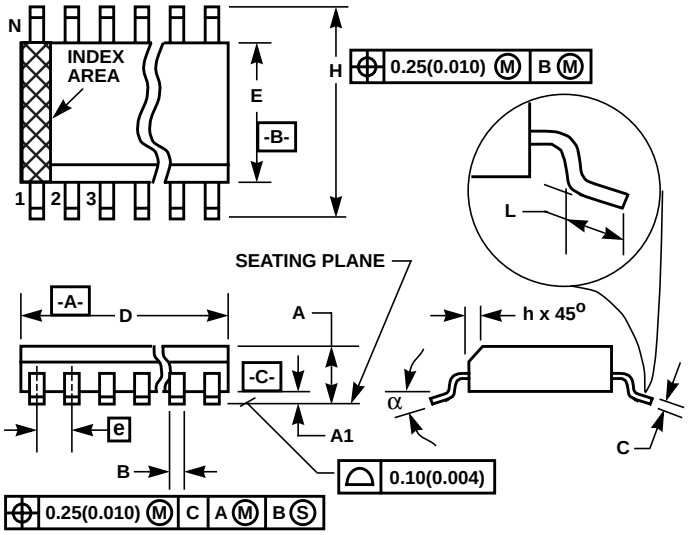
Small Outline Plastic Packages (SOIC)



NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

M28.3 (JEDEC MS-013-AE ISSUE C)
28 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

	INCHES		MILLIMETERS		
SYMBOL	MIN	MAX	MIN	MAX	NOTES
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.0200	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.6969	0.7125	17.70	18.10	3
E	0.2914	0.2992	7.40	7.60	4
e	0.05 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.01	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	28		28		7
α	0^o	8^o	0^o	8^o	-

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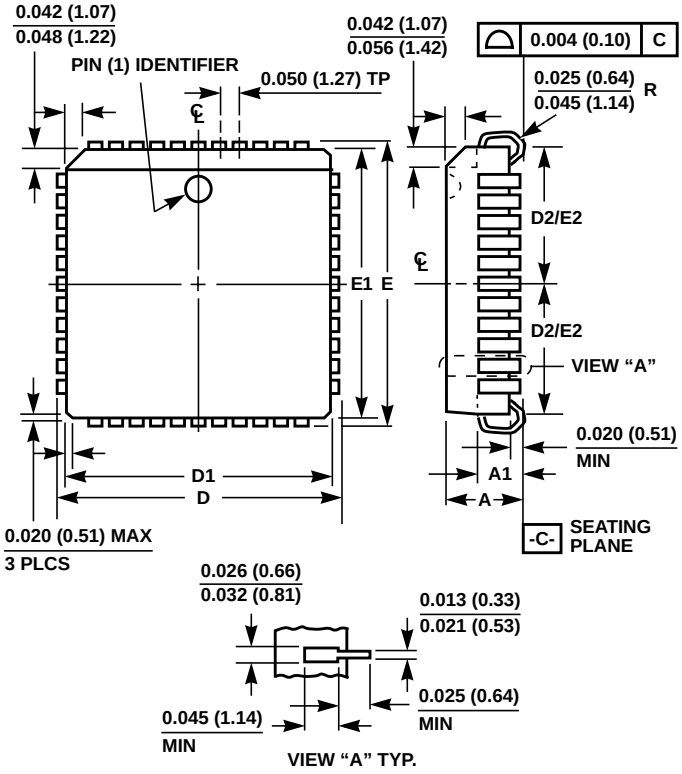
Plastic Leaded Chip Carrier Packages (PLCC)



N28.45 (JEDEC MS-018AB ISSUE A)
28 LEAD PLASTIC LEADED CHIP CARRIER PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.165	0.180	4.20	4.57	-
A1	0.090	0.120	2.29	3.04	-
D	0.485	0.495	12.32	12.57	-
D1	0.450	0.456	11.43	11.58	3
D2	0.191	0.219	4.86	5.56	4, 5
E	0.485	0.495	12.32	12.57	-
E1	0.450	0.456	11.43	11.58	3
E2	0.191	0.219	4.86	5.56	4, 5
N	28		28		6

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NOTES:

1. Controlling dimension: INCH. Converted millimeter dimensions are not necessarily exact.
2. Dimensions and tolerancing per ANSI Y14.5M-1982.
3. Dimensions D1 and E1 do not include mold protrusions. Allowable mold protrusion is 0.010 inch (0.25mm) per side. Dimensions D1 and E1 include mold mismatch and are measured at the extreme material condition at the body parting line.
4. To be measured at seating plane -C- contact point.
5. Centerline to be determined where center leads exit plastic body.
6. "N" is the number of terminal positions.

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