Data Sheet | March 12, 2004 | FN7050.1

125MHz Single Supply, Clamping Op Amps

The EL2150 and EL2157 are the electronics industry's fastest single supply op amps available. Prior single supply op amps have generally been limited to bandwidths and slew rates ¼ that of the EL2150 and EL2157. The 125MHz bandwidth, 275V/µs slew rate, and 0.05%/0.05° differential gain/differential phase makes this part ideal for single or dual supply video speed applications. With its voltage feedback architecture, these amplifiers can accept reactive feedback networks, allowing them to be used in analog filtering applications. The inputs can sense signals below the bottom supply rail and as high as 1.2V below the top rail. Connecting the load resistor to ground and operating from a single supply, the outputs swing completely to ground without saturating. The outputs can also drive to within 1.2V of the top rail. The EL2150 and EL2157 will output ±100mA and will operate with single supply voltages as low as 2.7V, making them ideal for portable, low power applications.

The EL2157 has a high speed disable feature. Applying a low logic level to this pin reduces the supply current to 0µA within 50ns. This is useful for both multiplexing and reducing power consumption.

The EL2157 also has an output voltage clamp feature. This clamp is a fast recovery (<7ns) output clamp that prevents the output voltage from going above the preset clamp voltage. This feature is desirable for A/D applications, as A/D converters can require long times to recover if overdriven.

For applications where board space is critical the EL2150 is available in the tiny 5-pin SOT-23 package, which has a footprint 28% the size of an 8-pin SO. The EL2150 and EL2157 are both available in an 8-pin SO package. All parts operate over the industrial temperature range of -40°C to +85°C. For dual, triple, or quad applications, contact the factory.

Features

- Specified for 3V, 5V, or ±5V applications
- Power-down to 0µA (EL2157)
- Output voltage clamp (EL2157)
- Large input common mode range $0V < V_{CM} < V_S - 1.2V$
- Output swings to ground without saturating
- -3dB bandwidth = 125MHz
- ±0.1dB bandwidth = 30MHz
- Low supply current = 5mA
- Slew rate = 275V/µs
- Low offset voltage = 2mV max (SO package)
- Output current = ±100mA
- High open loop gain = 80dB
- Diff gain/phase = 0.05%/0.05°

Applications

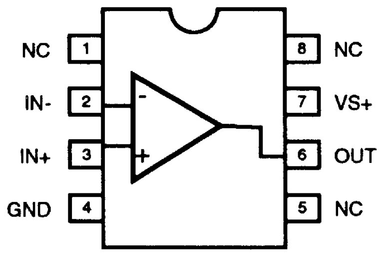
- Video amplifiers
- PCMCIA applications
- A/D drivers
- Line drivers
- Portable computers
- High speed communications
- RGB applications
- Broadcast equipment
- Active filtering

Ordering Information

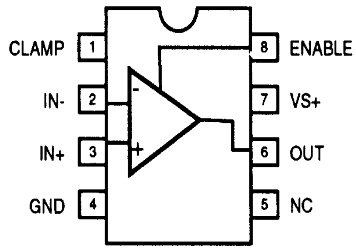
PART NUMBER	PACKAGE	TAPE & REEL	PKG. DWG. #
EL2150CS	8-Pin SO	-	MDP0027
EL2150CS-T7	8-Pin SO	7”	MDP0027
EL2150CS-T13	8-Pin SO	13”	MDP0027
EL2150CW-T7	5-Pin SOT-23	7” (3K pcs)	MDP0038
EL2150CW-T7A	5-Pin SOT-23	7” (250 pcs)	MDP0038
EL2157CS	8-Pin SO	-	MDP0027
EL2157CS-T7	8-Pin SO	7”	MDP0027
EL2157CS-T13	8-Pin SO	13”	MDP0027

Pinouts

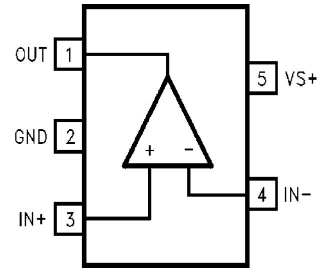
EL2150
(8-PIN SO)
TOP VIEW



EL2157
(8-PIN SO)
TOP VIEW



EL2150
(5-PIN SOT-23)
TOP VIEW



Absolute Maximum Ratings (T_A = 25°C)

Supply Voltage between V_S+ and GND . . . . +12.6V
Input Voltage (IN+, IN-, ENABLE, CLAMP) . . . GND-0.3V, V_S+0.3V
Differential Input Voltage . . . .±6V
Maximum Output Current. 90mA
Output Short Circuit Duration. . . . . (Note 1)
Power Dissipation . . . . See Curves
Storage Temperature Range . . . .-65°C to +150°C
Ambient Operating Temperature Range . . . .-40°C to +85°C
Operating Junction Temperature. . . . . 150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

DC Electrical Specifications

V_S = +5V, GND = 0V, T_A = 25°C, V_{CM} = 1.5V, V_{OUT} = 1.5V, V_{CLAMP} = +5V, V_{ENABLE} = +5V, unless otherwise specified. (Note 1)

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
V_{OS}	Offset Voltage	SO package	-2		2	mV
		SOT-23 package	-3		3	mV
TCV_{OS}	Offset Voltage Temperature Coefficient	Measured from T_{MIN} to T_{MAX}		10		µV/°C
IB	Input Bias Current	V_{IN} = 0V		-5.5	-10	µA
I_{OS}	Input Offset Current	V_{IN} = 0V	-750	150	750	nA
TCI_{OS}	Input Bias Current Temperature Coefficient	Measured from T_{MIN} to T_{MAX}		50		nA/°C
PSRR	Power Supply Rejection Ratio	V_S = V_{ENABLE} = 2.7V to 12V, V_{CLAMP} = OPEN	55	70		dB
CMRR	Common Mode Rejection Ratio	V_{CM} = 0V to 3.8V	55	65		dB
		V_{CM} = 0V to 3.0V	55	70		dB
CMIR	Common Mode Input Range		0		V_S-1.2	V
R_{IN}	Input Resistance	Common mode	1	2		MΩ
C_{IN}	Input Capacitance	SO package		1		pF
R_{OUT}	Output Resistance	A_V = 1		40		mΩ
$I_{S,ON}$	Supply Current - Enabled	V_S = V_{CLAMP} = 12V, V_{ENABLE} = 12V		5	6.5	mA
$I_{S,OFF}$	Supply Current - Shut Down	V_S = V_{CLAMP} = 10V, V_{ENABLE} = 0.5V		0	50	µA
		V_S = V_{CLAMP} = 12V, V_{ENABLE} = 0.5V		5		µA
PSOR	Power Supply Operating Range		2.7		12.0	V
AVOL	Open Loop Gain	V_S = V_{CLAMP} = 12V, V_{OUT} = 2V	65	80		dB
		9V, R_L = 1kΩ to GND				
		V_{OUT} = 1.5V to 3.5V		70		dB
		R_L = 1kΩ to GND				
		V_{OUT} = 1.5V to 3.5V		60		dB
		R_L = 150Ω to GND				
V_{OP}	Positive Output Voltage Swing	V_S = 12V, A_V = 1, R_L= 1kΩ to 0V		10.8		V
		V_S = 12V, A_V = 1, R_L = 150Ω to 0V	9.6	10.0		V
		V_S = ±5V, A_V = 1, R_L = 1kΩ to 0V		4.0		V
		V_S = ±5V, A_V = 1, R_L = 150Ω to 0V	3.4	3.8		V
		V_S = 3V, A_V = 1, R_L = 150Ω to 0V	1.8	1.95		V

DC Electrical Specifications

V_S = +5V, GND = 0V, T_A = 25°C, V_{CM} = 1.5V, V_{OUT} = 1.5V, V_{CLAMP} = +5V, V_{ENABLE} = +5V, unless otherwise specified. (Note 1) **(Continued)**

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
V_{ON}	Negative Output Voltage Swing	V_S = 12V, A_V = 1, R_L = 150Ω to 0V		5.5	8	mV
		V_S = ±5V, A_V = 1, R_L = 1kΩ to 0V		-4.0		V
		V_S = ±5V, A_V = 1, R_L = 150Ω to 0V		-3.7	-3.4	V
I_{OUT}	Output Current (Note 2)	V_S = ±5V, A_V = 1, R_L = 10Ω to 0V	±75	±100		mA
		V_S = ±5V, A_V = 1, R_L = 50Ω to 0V		±60		mA
$I_{OUT,OFF}$	Output Current, Disabled	V_{ENABLE} = 0.5V		0	20	µA
V_{IH-EN}	ENABLE pin Voltage for Power Up	Relative to GND pin	2.0			V
V_{IL-EN}	ENABLE pin Voltage for Shut Down	Relative to GND pin			0.5	V
I_{IH-EN}	ENABLE pin Input Current-High (Note 3)	V_S = V_{CLAMP} = 12V, V_{ENABLE} = 12V		340	410	µA
I_{IL-EN}	ENABLE pin Input Current-Low (Note 3)	V_S = V_{CLAMP} = 12V, V_{ENABLE} = 0.5V		0	1	µA
V_{OR-CL}	Voltage Clamp Operating Range (Note 4)	Relative to GND pin	1.2		V_{OP}	V
V_{ACC-CL}	CLAMP Accuracy	V_{IN} = 4V, R_L = 1kΩ to GND	-250	100	250	mV
		V_{CLAMP} = 1.5V and 3.5V				
I_{IH-CL}	CLAMP pin Input Current - High	V_S = V_{CLAMP} = 12V		12	25	µA
I_{IL-CL}	CLAMP pin Input Current - Low	V_S = 12V, V_{CLAMP} = 1.2V	-20	-15		µA

NOTES:

1. CLAMP pin and ENABLE pin specifications apply only to the EL2157.
2. Internal short circuit protection circuitry has been built into the EL2150/EL2157. See the Applications section.
3. If the disable feature is not desired, tie the ENABLE pin to the V_S pin, or apply a logic high level to the ENABLE pin.
4. The maximum output voltage that can be clamped is limited to the maximum positive output Voltage, or V_{OP}. Applying a voltage higher than V_{OP} inactivates the clamp. If the clamp feature is not desired, either tie the CLAMP pin to the V_S pin, or simply let the CLAMP pin float.

Closed Loop AC Electrical Specifications

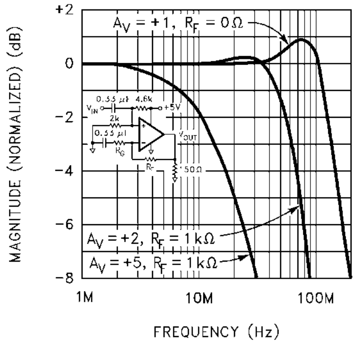
V_S = +5V, GND = 0V, T_A = 25°C, V_{CM} = +1.5V, V_{OUT} = +1.5V, V_{CLAMP} = +5V, V_{ENABLE} = +5V, A_V = +1, R_F = 0Ω, R_L = 150Ω to GND pin, unless otherwise specified. (Notes 1 and 2)

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
BW	-3dB Bandwidth (V_{OUT} = 400mV_{P-P})	V_S = 5V, A_V = 1, R_F = 0Ω		125		MHz
		V_S = 5V, A_V = -1, R_F = 500Ω		60		MHz
		V_S = 5V, A_V = 2, R_F = 500Ω		60		MHz
		V_S = 5V, A_V = 10, R_F = 500Ω		6		MHz
		V_S = 12V, A_V = 1, R_F = 0Ω		150		MHz
		V_S = 3V, A_V = 1, R_F = 0Ω		100		MHz
BW	±0.1dB Bandwidth (V_{OUT} = 400mV_{P-P})	V_S = 12V, A_V = 1, R_F = 0Ω		25		MHz
		V_S = 5V, A_V = 1, R_F = 0Ω		30		MHz
		V_S = 3V, A_V = 1, R_F = 0Ω		20		MHz
GBWP	Gain Bandwidth Product	V_S = 12V, @ A_V = 10		60		MHz
PM	Phase Margin	R_L = 1kΩ, C_L = 6 pF		55		°
SR	Slew Rate	V_S = 10V, R_L = 150Ω, V_{OUT} = 0V to 6V	200	275		V/µs
		V_S = 5V, R_L = 150Ω, V_{OUT} = 0V to 3V		300		V/µs
t_R,t_F	Rise Time, Fall Time	±0.1V step		2.8		ns
OS	Overshoot	±0.1V step		10		%
t_{PD}	Propagation Delay	±0.1V step		3.2		ns
t_S	0.1% Settling Time	V_S = ±5V, R_L = 500Ω, A_V = 1, V_{OUT} = ±3V		40		ns
	0.01% Settling Time	V_S = ±5V, R_L = 500Ω, A_V = 1, V_{OUT} = ±3V		75		ns
dG	Differential Gain (Note 3)	A_V = 2, R_F = 1kΩ		0.05		%
dP	Differential Phase (Note 3)	A_V = 2, R_F = 1kΩ		0.05		°
e_N	Input Noise Voltage	f = 10kHz		48		nV/√Hz
i_N	Input Noise Current	f = 10kHz		1.25		pA/√Hz
t_{DIS}	Disable Time (Note 4)			50		ns
t_{EN}	Enable Time (Note 4)			25		ns
t_{CL}	Clamp Overload Recovery			7		ns

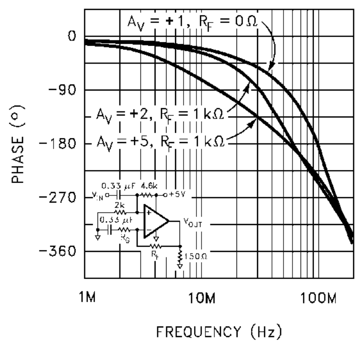
NOTES:

1. CLAMP pin and ENABLE pin specifications apply only to the EL2157.
2. All AC tests are performed on a “warmed up” part, except slew rate, which is pulse tested.
3. Standard NTSC signal = 286mV_{P-P}, f = 3.58MHz, as V_{IN} is swept from 0.6V to 1.314V.R_L is DC coupled.
4. Disable/Enable time is defined as the time from when the logic signal is applied to the ENABLE pin to when the supply current has reached half its final value.

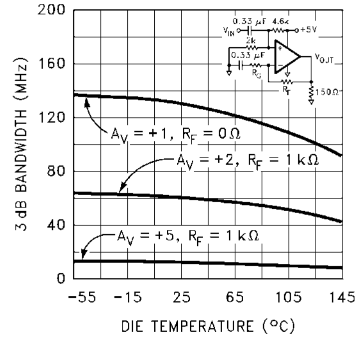
Typical Performance Curves



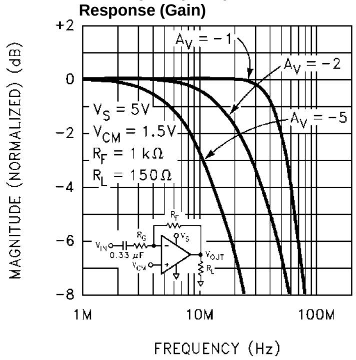
Non-Inverting Frequency Response (Gain)



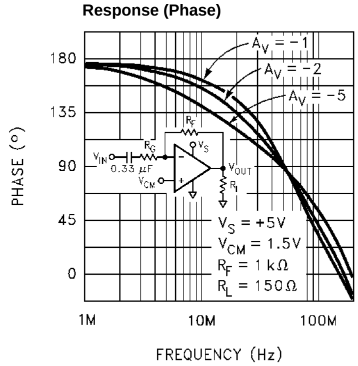
Non-Inverting Frequency Response (Phase)



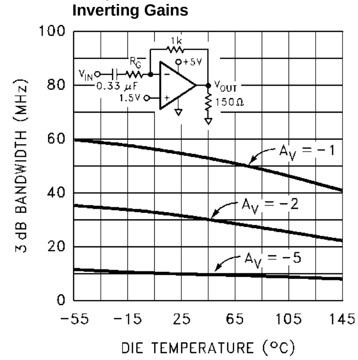
3dB Bandwidth vs Temperature for Non-Inverting Gains



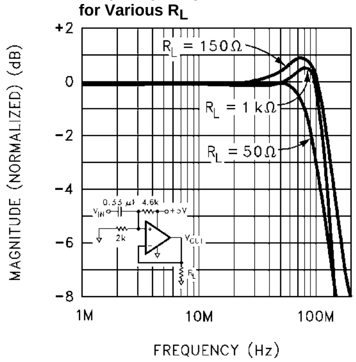
Inverting Frequency Response (Gain)



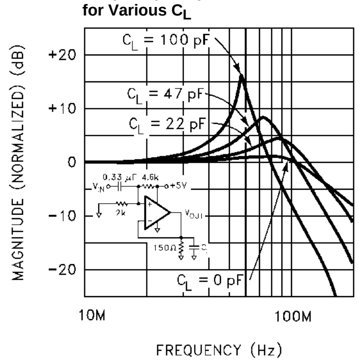
Inverting Frequency Response (Phase)



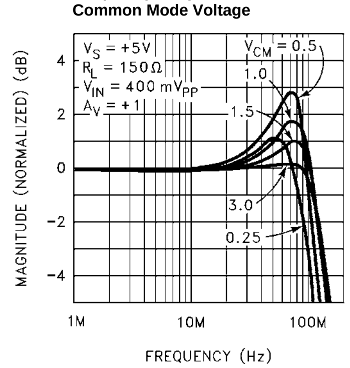
In 3dB Bandwidth vs Temperature for Inverting Gains



Frequency Response for Various R_L



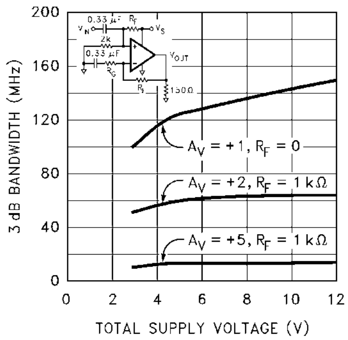
Frequency Response for Various C_L



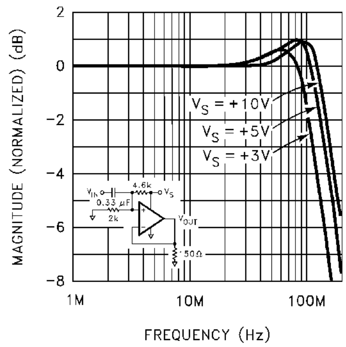
Non-Inverting Frequency Response vs Common Mode Voltage

Typical Performance Curves (Continued)

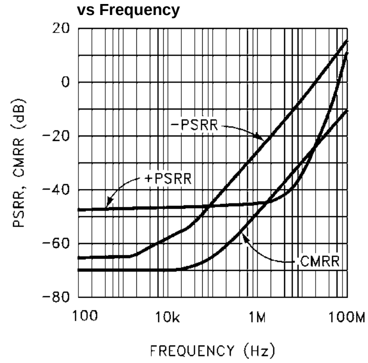
3dB Bandwidth vs Supply Voltage for Non-Inverting Gains



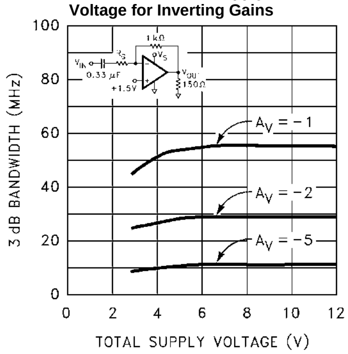
Frequency Response for Various Supply Voltages, $A_V = +1$



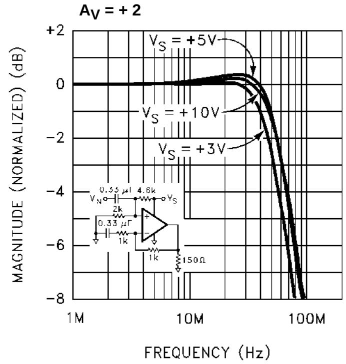
PSSR and CMRR vs Frequency



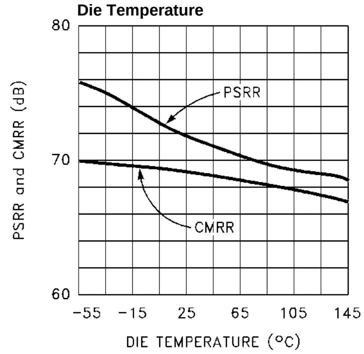
3dB Bandwidth vs Supply Voltage for Inverting Gains



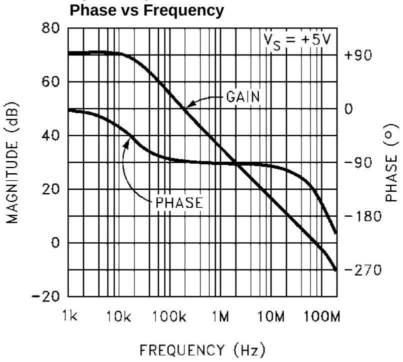
Frequency Response for Various Supply Voltages, $A_V = +2$



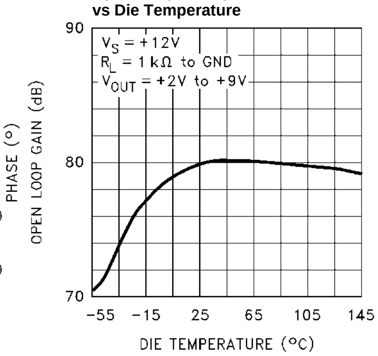
PSRR and CMRR vs Die Temperature



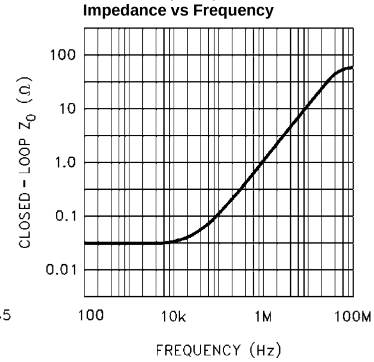
Open Loop Gain and Phase vs Frequency



Open Loop Voltage Gain vs Die Temperature

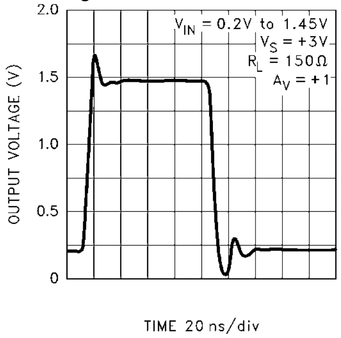


Closed Loop Output Impedance vs Frequency

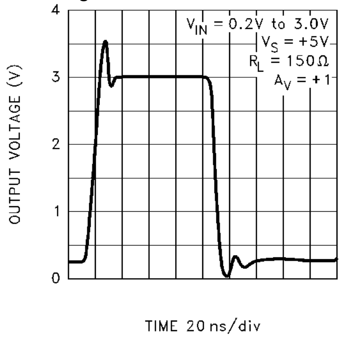


Typical Performance Curves (Continued)

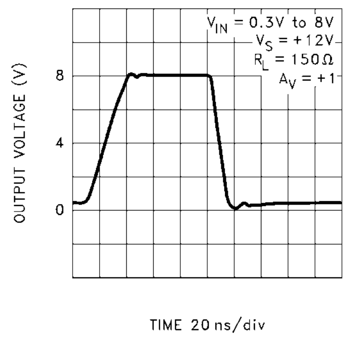
Large Signal Step Response, V_S = +3V



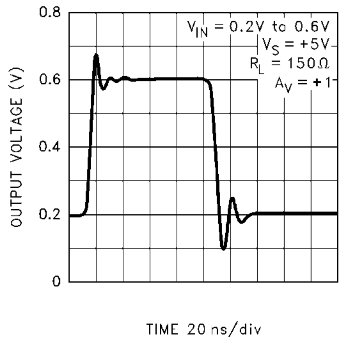
Large Signal Step Response, V_S = +5V



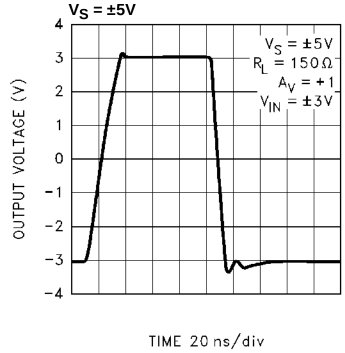
Large Signal Step Response, V_S = +12V



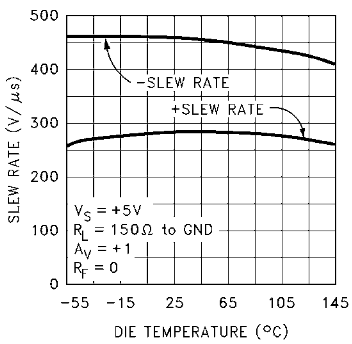
Small Signal Step Response



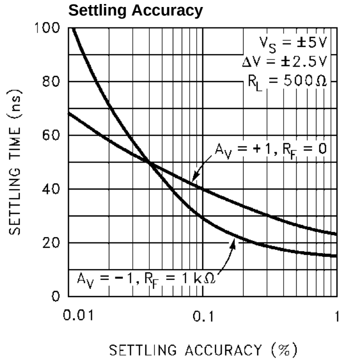
Large Signal Step Response, V_S = ±5V



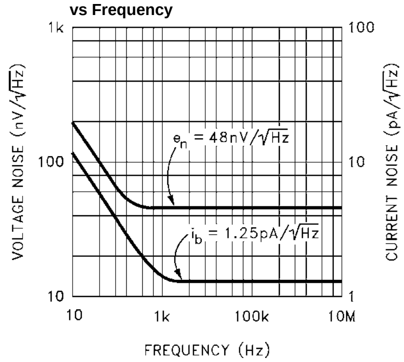
Slew Rate vs Temperature



Settling Time vs Settling Accuracy

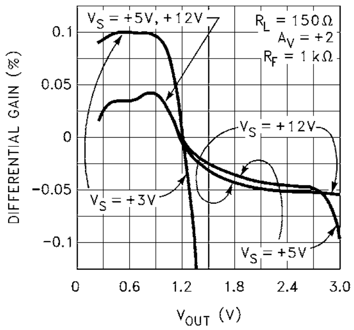


Voltage and Current Noise vs Frequency

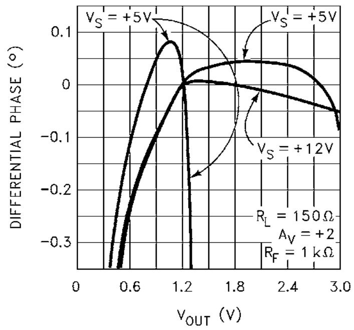


Typical Performance Curves (Continued)

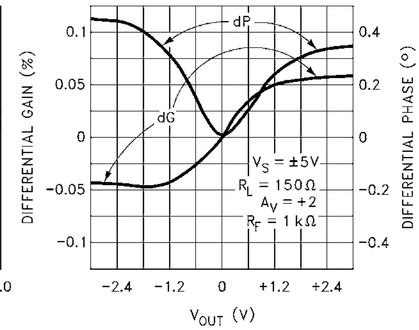
Differential Gain for Single Supply Operation



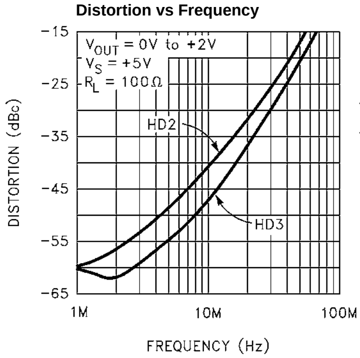
Differential Phase for Single Supply Operation



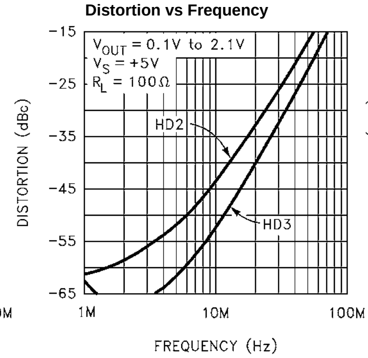
Differential Gain and Phase for Dual Supply Operation



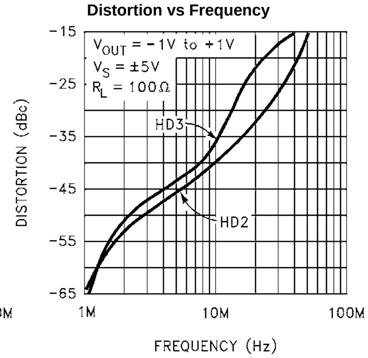
2nd and 3rd Harmonic Distortion vs Frequency



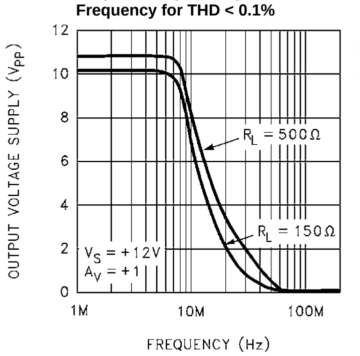
2nd and 3rd Harmonic Distortion vs Frequency



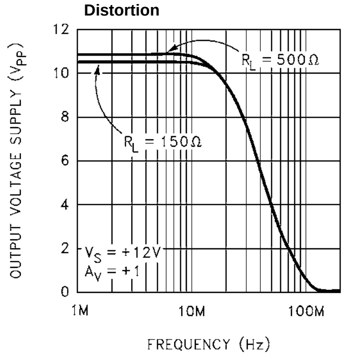
2nd and 3rd Harmonic Distortion vs Frequency



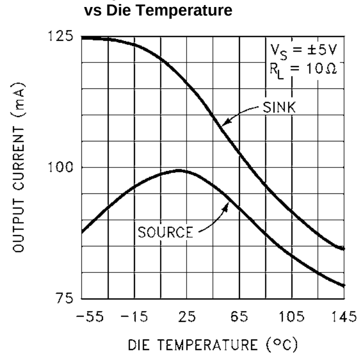
Output Voltage Swing vs Frequency for THD < 0.1%



Output Voltage Swing vs Frequency for Unlimited Distortion

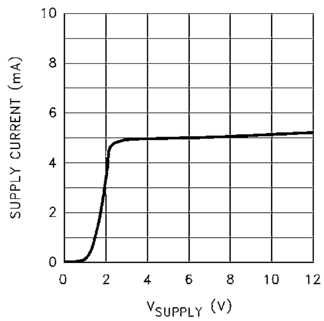


Output Current vs Die Temperature

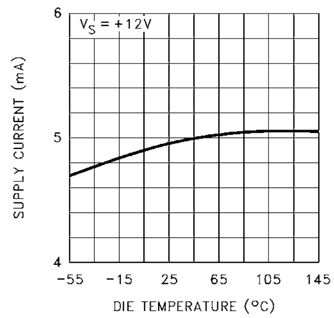


Typical Performance Curves **(Continued)**

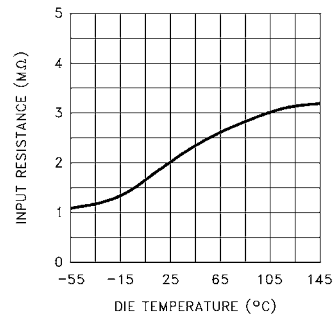
Supply Current vs Supply Voltage



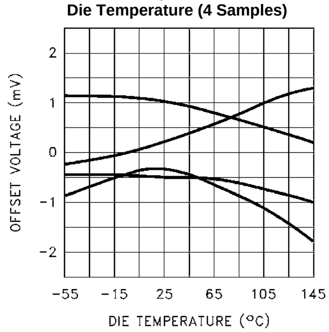
Supply Current vs Die Temperature



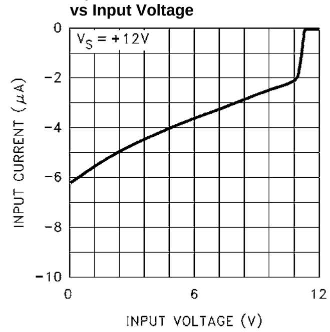
Input Resistance vs Die Temperature



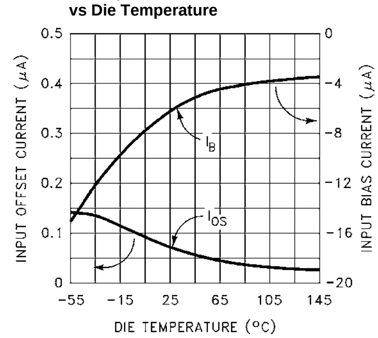
Offset Voltage vs Die Temperature (4 Samples)



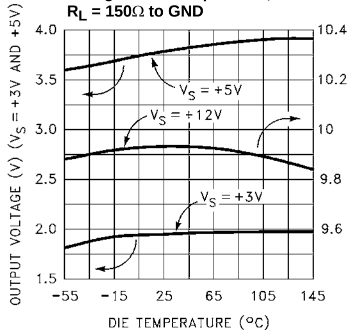
Input Bias Current vs Input Voltage



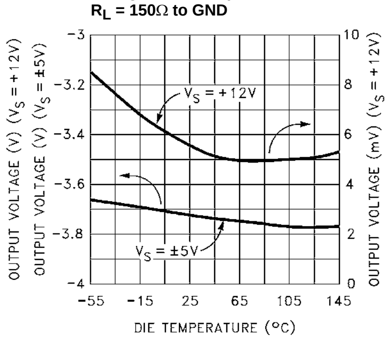
Input Offset Current and Input Bias Current vs Die Temperature



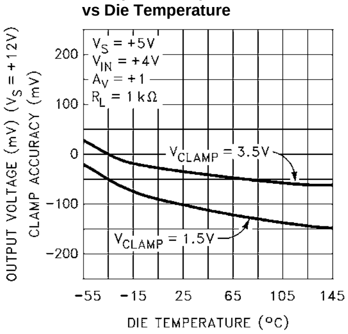
Positive Output Voltage Swing vs Die Temperature, R_L = 150Ω to GND



Negative Output Voltage Swing vs Die Temperature, R_L = 150Ω to GND

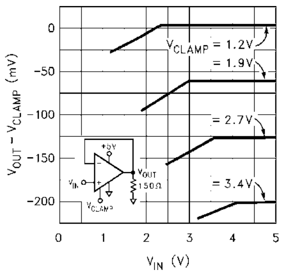


Clamp Accuracy vs Die Temperature

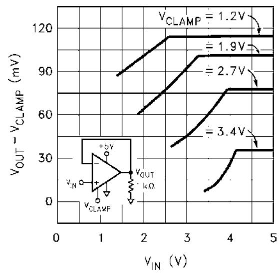


Typical Performance Curves (Continued)

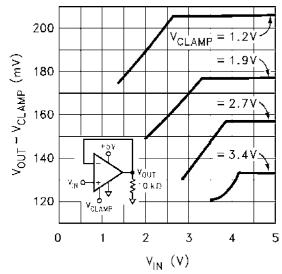
Clamp Accuracy
$R_L = 150\Omega$



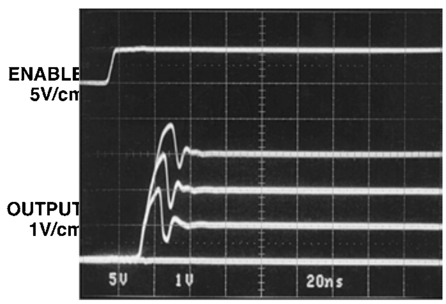
Clamp Accuracy
$R_L = 1k\Omega$



Clamp Accuracy
$R_L = 10k\Omega$

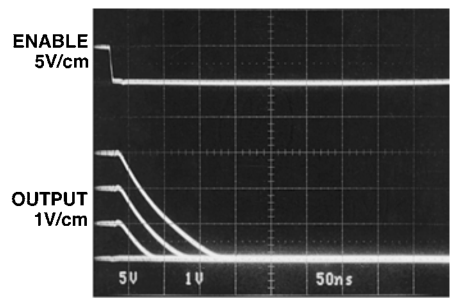


Enable Response for a Family of DC Inputs



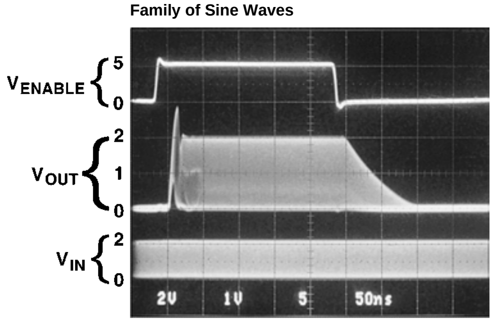
$A_V = +1, R_L = 150\Omega, V_S = +5V$

Disable Response for a Family of DC Inputs



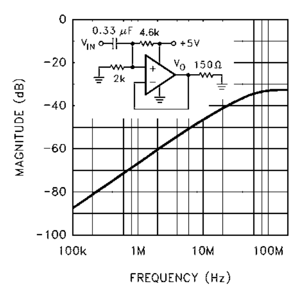
$A_V = +1, R_L = 150\Omega, V_S = +5V$

Disable/Enable Response for a Family of Sine Waves

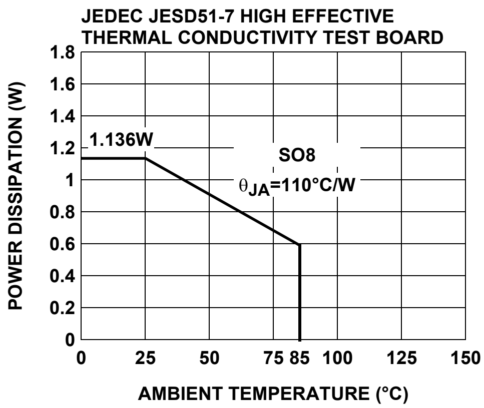


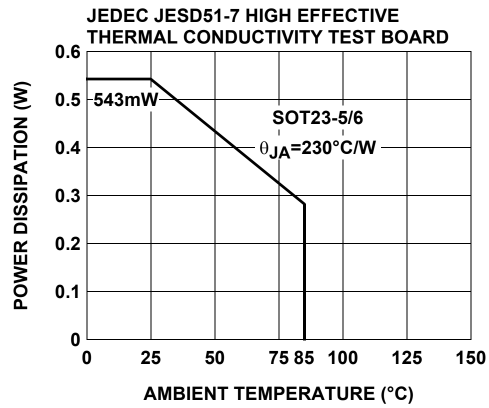
50 ns/div

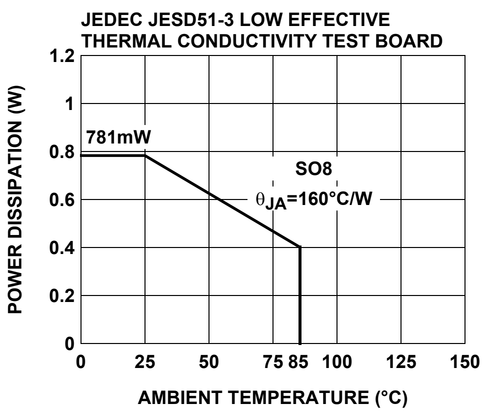
OFF Isolation

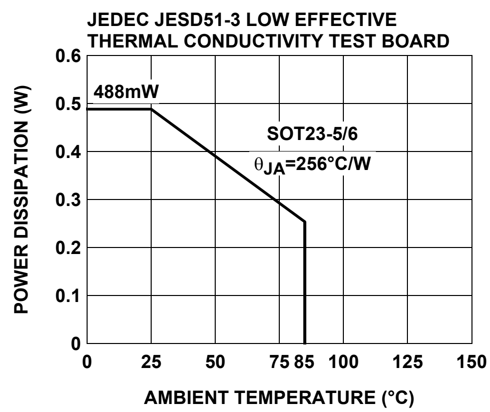


Typical Performance Curves (Continued)

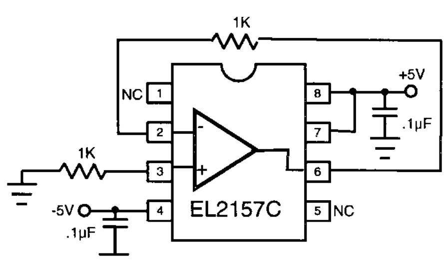




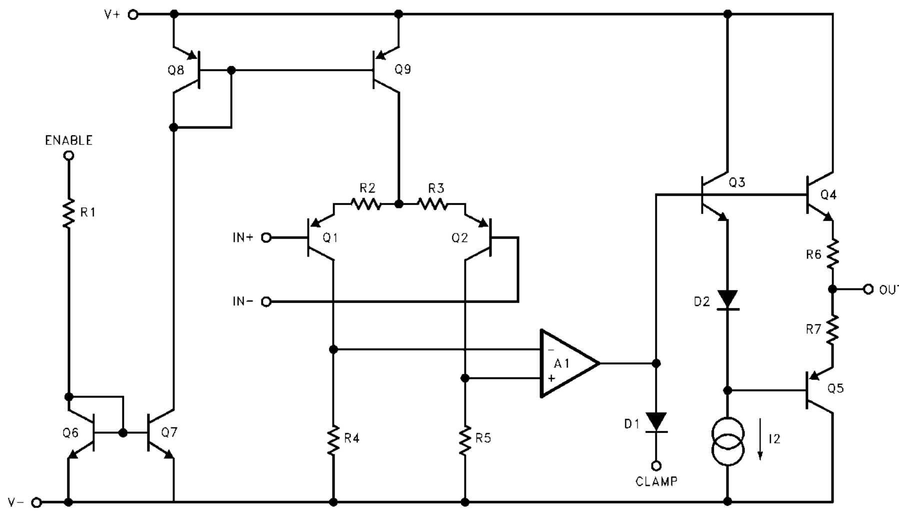




Burn-In Circuit



Simplified Schematic



Applications Information

Product Description

The EL2150 and EL2157 are the industry's fastest single supply operational amplifiers. Connected in voltage follower mode, their -3dB bandwidth is 125MHz while maintaining a 275V/µs slew rate. With an input and output common mode range that includes ground, these amplifiers were optimized for single supply operation, but will also accept dual supplies. They operate on a total supply voltage range as low as +2.7V or up to +12V. This makes them ideal for +3V applications, especially portable computers.

While many amplifiers claim to operate on a single supply, and some can sense ground at their inputs, most fail to truly drive their outputs to ground. If they do succeed in driving to ground, the amplifier often saturates, causing distortion and recovery delays. However, special circuitry built into the EL2150 and EL2157 allows the output to follow the input signal to ground without recovery delays.

Power Supply Bypassing And Printed Circuit Board Layout

As with any high-frequency device, good printed circuit board layout is necessary for optimum performance. Ground plane construction is highly recommended. Lead lengths should be as short as possible. The power supply pins must be well bypassed to reduce the risk of oscillation. The combination of a 4.7µF tantalum capacitor in parallel with a 0.1µF ceramic capacitor has been shown to work well when placed at each supply pin. For single supply operation, where pin 4 (V_S-) is connected to the ground plane, a single 4.7µF tantalum capacitor in parallel with a 0.1µF ceramic capacitor across pins 7 and 4 will suffice.

For good AC performance, parasitic capacitance should be kept to a minimum. Ground plane construction should be used. Carbon or Metal-Film resistors are acceptable with the Metal-Film resistors giving slightly less peaking and bandwidth because of their additional series inductance. Use of sockets, particularly for the SO package should be avoided if possible. Sockets add parasitic inductance and capacitance which will result in some additional peaking and overshoot.

Supply Voltage Range and Single-Supply Operation

The EL2150 and EL2157 have been designed to operate with supply voltages having a span of greater than 2.7V, and less than 12V. In practical terms, this means that the EL2150 and EL2157 will operate on dual supplies ranging from ±1.35V to ±6V. With a single-supply, the EL2150 and EL2157 will operate from +2.7V to +12V. Performance has been optimized for a single +5V supply.

Pins 7 and 4 are the power supply pins. The positive power supply is connected to pin 7. When used in single supply mode, pin 4 is connected to ground. When used in dual supply mode, the negative power supply is connected to pin 4.

As supply voltages continue to decrease, it becomes necessary to provide input and output voltage ranges that can get as close as possible to the supply voltages. The EL2150 and EL2157 have an input voltage range that includes the negative supply and extends to within 1.2V of the positive supply. So, for example, on a single +5V supply, the EL2150 and EL2157 have an input range which spans from 0V to 3.8V.

The output range of the EL2150 and EL2157 is also quite large. It includes the negative rail, and extends to within 1V of the top supply rail. On a +5V supply, the output is therefore capable of swinging from 0V to +4V. On split supplies, the output will swing ±4V. If the load resistor is tied to the negative rail and split supplies are used, the output range is extended to the negative rail.

Choice Of Feedback Resistor, R_F

The feedback resistor forms a pole with the input capacitance. As this pole becomes larger, phase margin is reduced. This increases ringing in the time domain and peaking in the frequency domain. Therefore, R_F has some maximum value which should not be exceeded for optimum performance. If a large value of R_F must be used, a small capacitor in the few picofarad range in parallel with R_F can help to reduce this ringing and peaking at the expense of reducing the bandwidth.

As far as the output stage of the amplifier is concerned, R_F+ R_G appear in parallel with R_L for gains other than +1. As this combination gets smaller, the bandwidth falls off. Consequently, R_F has a minimum value that should not be exceeded for optimum performance.

For A_V = +1, R_F = 0Ω is optimum. For A_V = -1 or +2 (noise gain of 2), optimum response is obtained with R_F between 500Ω and 1kΩ. For A_V = -4 or +5 (noise gain of 5), keep R_F between 2kΩ and 10kΩ.

Video Performance

For good video performance, an amplifier is required to maintain the same output impedance and the same frequency response as DC levels are changed at the output. This can be difficult when driving a standard video load of 150Ω, because of the change in output current with DC level. Differential Gain and Differential Phase for the EL2150 and EL2157 are specified with the black level of the output video signal set to +1.2V. This allows ample room for the sync pulse even in a gain of +2 configuration. This results in dG and dP specifications of 0.05% and 0.05° while driving 150Ω at a gain of +2. Setting the black level to other values, although acceptable, will compromise peak performance. For example, looking at the single supply dG and dP curves for R_L=150Ω, if the output black level clamp is reduced from 1.2V to 0.6V dG/dP will increase from 0.05%/0.05° to 0.08%/0.25° Note that in a gain of +2 configuration, this is the lowest black level allowed such that the sync tip doesn't go below 0V.

If your application requires that the output goes to ground, then the output stage of the EL2150 and EL2157, like all other single supply op amps, requires an external pull down resistor tied to ground. As mentioned above, the current flowing through this resistor becomes the DC bias current for the output stage NPN transistor. As this current approaches zero, the NPN turns off, and dG and dP will increase. This becomes more critical as the load resistor is increased in value. While driving a light load, such as 1kΩ, if the input black level is kept above 1.25V, dG and dP are a respectable 0.03% and 0.03°.

For other biasing conditions see the Differential Gain and Differential Phase vs Input Voltage curves.

Output Drive Capability

In spite of their moderately low 5mA of supply current, the EL2150 and EL2157 are capable of providing ±100mA of output current into a 10Ω load, or ±60mA into 50Ω. With this large output current capability, a 50Ω load can be driven to ±3V with V_S = ±5V, making it an excellent choice for driving isolation transformers in telecommunications applications.

Driving Cables and Capacitive Loads

When used as a cable driver, double termination is always recommended for reflection-free performance. For those applications, the back-termination series resistor will decouple the EL2150 and EL2157 from the cable and allow extensive capacitive drive. However, other applications may have high capacitive loads without a back-termination resistor. In these applications, a small series resistor (usually between 5Ω and 50Ω) can be placed in series with the output to eliminate most peaking. The gain resistor (R_G) can then be chosen to make up for any gain loss which may be created by this additional resistor at the output.

Disable/Power-Down

The EL2157 amplifier can be disabled, placing its output in a high-impedance state. The disable or enable action takes only about 40ns. When disabled, the amplifier's supply current is reduced to 0mA, thereby eliminating all power consumption by the EL2157. The EL2157 amplifier's power down can be controlled by standard CMOS signal levels at the ENABLE pin. The applied CMOS signal is relative to the GND pin. For example, if a single +5V supply is used, the logic voltage levels will be +0.5V and +2.0V. If using dual ±5V supplies, the logic levels will be -4.5V and -3.0V. Letting the ENABLE pin float will disable the EL2157. If the power-down feature is not desired, connect the ENABLE pin to the V_S+ pin. The guaranteed logic levels of +0.5V and +2.0V are not standard TTL levels of +0.8V and +2.0V, so care must be taken if standard TTL will be used to drive the ENABLE pin.

Output Voltage Clamp

The EL2157 amplifier has an output voltage clamp. This clamping action is fast, being activated almost instantaneously, and being deactivated in <7ns, and prevents the output voltage from going above the preset clamp voltage. This can be very helpful when the EL2157 is used to drive an A/D converter, as some converters can require long times to recover if overdriven. The output voltage remains at the clamp voltage level as long as the product of the input voltage and the gain setting exceeds the clamp voltage. If the EL2157 is connected in a gain of 2, for example, and +3V DC is applied to the CLAMP pin, any voltage higher than +1.5V at the inputs will be clamped and +3V will be seen at the output.

Figure 1 below is a unity gain connected EL2157 being driven by a $3V_{P-P}$ sinewave, with 2.25V applied to the CLAMP pin. The resulting output waveform, with its output being clamped to 2.25V, is shown in Figure 2.

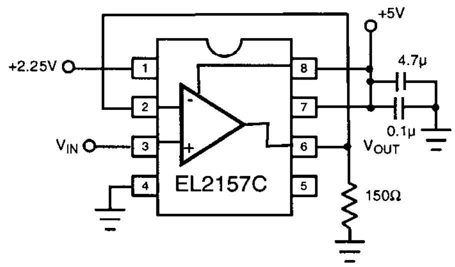


FIGURE 1.

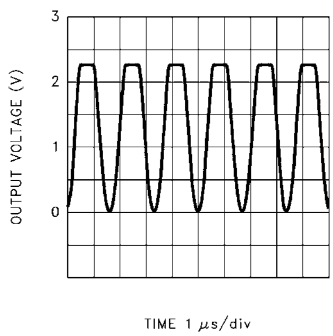


FIGURE 2.

Figure 3 shows the output of the same circuit being driven by a 0.5V to 2.75V square wave, as the clamp voltage is varied from 1.0V to 2.5V, as well as the unclamped output signal. The rising edge of the signal is clamped to the voltage applied to the CLAMP pin almost instantaneously. The output recovers from the clamped mode within 5ns - 7ns, depending on the clamp voltage. Even when the CLAMP pin is taken 0.2V below the minimum 1.2V specified, the output is still clamped and recovers in about 11ns.

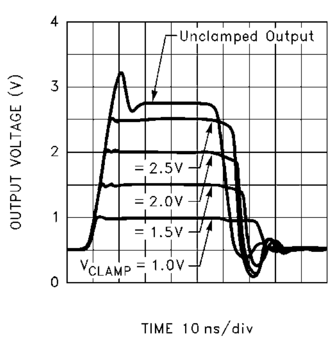


FIGURE 3.

The clamp accuracy is affected by 1) the CLAMP pin voltage, 2) the input voltage, and 3) the load resistor. Depending upon the application, the accuracy may be as little as a few tens of millivolts to a few hundred millivolts. Be sure to allow for these inaccuracies when choosing the clamp voltage. Curves of Clamp Accuracy vs V_{CLAMP}, and V_{IN} for 3 values of R_L are included in the Typical Performance Curves Section.

Unlike amplifiers that clamp at the input and are therefore limited to non-inverting applications only, the EL2157 output clamp architecture works for both inverting and non-inverting gain applications. There is also no maximum voltage difference limitation between V_{IN} and V_{CLAMP} which is common on input clamped architectures.

The voltage clamp operates for any voltage between +1.2V above the GND pin, and the minimum output voltage swing, V_{OP}. Forcing the CLAMP pin much below +1.2V can saturate transistors and should therefore be avoided.

Forcing the CLAMP pin above V_{OP} simply de-activates the CLAMP feature. In other words, one cannot expect to clamp any voltage higher than what the EL2157 can drive to in the first place. If the clamp feature is not desired, either let the CLAMP pin float or connect it to the V_S+ pin.

EL2157 Comparator Application

The EL2157 can be used as a very fast, single supply comparator by utilizing the clamp feature. Most op amps used as comparators allow only slow speed operation because of output saturation issues. However, by applying a DC voltage to the CLAMP pin of the EL2157, the maximum output voltage can be clamped, thus preventing saturation. Figure 4 below is the EL2157 implemented as a comparator. 2.5V DC is applied to the CLAMP pin, as well as the IN- pin. A differential signal is then applied between the inputs. Figure 5 shows the output square wave that results when a ±1V, 10MHz triangular wave is applied, while Figure 6 is a graph of propagation delay vs. overdrive as a square wave is presented at the input.

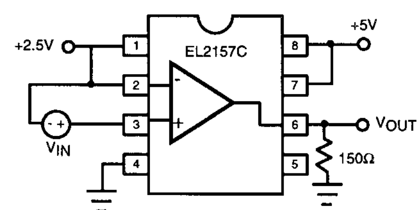


FIGURE 4.

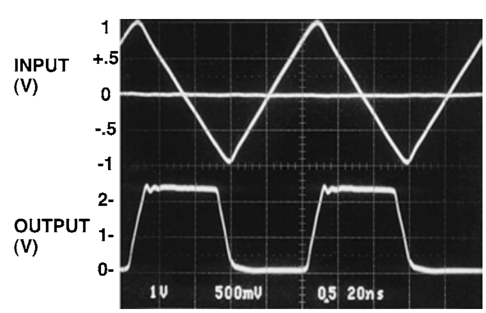


FIGURE 5.

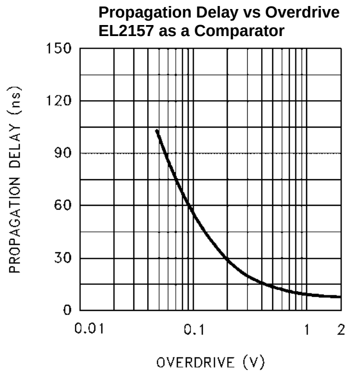


FIGURE 6.

Video Sync Pulse Remover Application

All CMOS Analog to Digital Converters (A/Ds) have a parasitic latch-up problem when subjected to negative input voltage levels. Since the sync tip contains no useful video information and it is a negative going pulse, we can chop it off. Figure 7 shows a unity gain connected EL2150 and EL2157. Figure 8 shows the complete input video signal applied at the input, as well as the output signal with the negative going sync pulse removed.

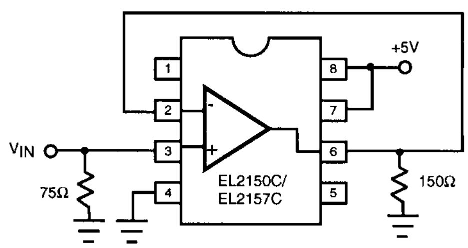


FIGURE 7.

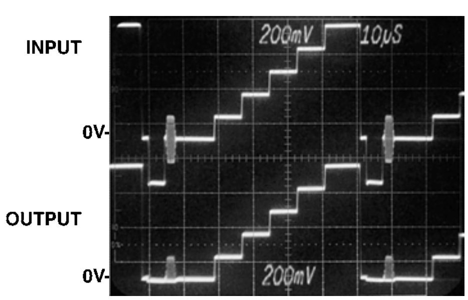


FIGURE 8.

Multiplexing with the EL2157

The ENABLE pin on the EL2157 allows for multiplexing applications. Figure 9 shows two EL2157s with their outputs tied together, driving a back terminated 75Ω video load. A $2V_{P-P}$ 10MHz sinewave is applied at one input, and a $1V_{P-P}$ 5MHz sinewave to the other. Figure 10 shows the CLOCK signal which is applied, and the resulting output waveform at V_{OUT}. Switching is complete in about 50ns. Notice the outputs are tied directly together. Decoupling resistors at each output are not necessary. In fact, adding them approximately doubles the switching time to 100ns.

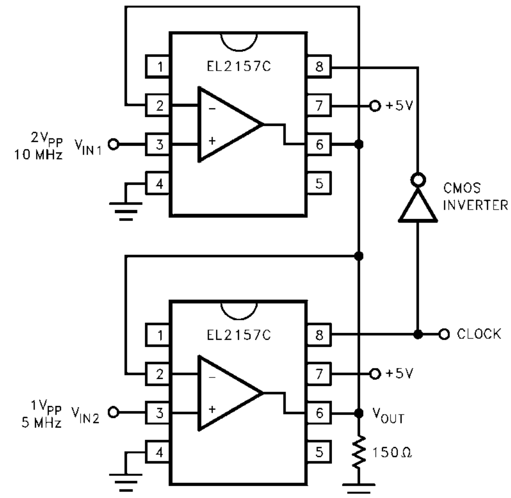


FIGURE 9.

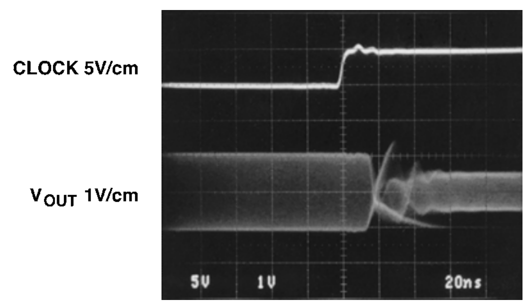


FIGURE 10.

Short Circuit Current Limit

The EL2150 and EL2157 have internal short circuit protection circuitry that protect it in the event of its output being shorted to either supply rail. This limit is set to around 100mA nominally and reduces with increasing junction temperature. It is intended to handle temporary shorts. If an output is shorted indefinitely, the power dissipation could easily increase such that the part will be destroyed. Maximum reliability is maintained if the output current never exceeds ±90mA. A heat sink may be required to keep the junction temperature below absolute maximum when an output is shorted indefinitely.

Power Dissipation

With the high output drive capability of the EL2150 and EL2157, it is possible to exceed the 150°C Absolute Maximum junction temperature under certain load current conditions. Therefore, it is important to calculate the maximum junction temperature for the application to determine if power-supply voltages, load conditions, or package type need to be modified for the EL2150 and EL2157 to remain in the safe operating area.

The maximum power dissipation allowed in a package is determined according to [1]:

$$PD_{MAX} = \frac{T_{JMAX} - T_{AMAX}}{\theta_{JA}}$$

where:

T_{JMAX} = Maximum junction temperature

T_{AMAX} = Maximum ambient temperature

θ_{JA} = Thermal resistance of the package

PD_{MAX} = Maximum power dissipation in the package

The maximum power dissipation actually produced by an IC is the total quiescent supply current times the total power supply voltage, plus the power in the IC due to the load, or [2]

$$PD_{MAX} = V_S \times I_{SMAX} + (V_s - V_{OUT}) \times \frac{V_{OUT}}{R_L}$$

where:

V_S = Total supply voltage

I_{SMAX} = Maximum supply current

V_{OUT} = Maximum output voltage of the application

R_L = Load resistance tied to ground

If we set the two PD_{MAX} equations, [1] & [2], equal to each other, and solve for V_S, we can get a family of curves for various loads and output voltages according to [3]:

$$V_S = \frac{\frac{R_L \times (T_{AMAX} - T_{AMAX})}{\theta_{JA}} + (V_{OUT})^2}{(I_s \times R_L) + V_{OUT}}$$

Figures 11 and 12 show total single supply voltage V_S vs R_L for various output voltage swings for the SO package. The curves assume WORST CASE conditions of T_A = +85°C and I_S = 6.5mA.

Single Supply Voltage vs R_{LOAD} for Various V_{OUT} (SO Package)

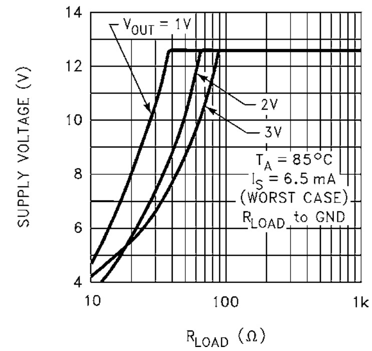


FIGURE 11.

Single Supply Voltage vs R_{LOAD} for Various V_{OUT} (SOT-23 Package)

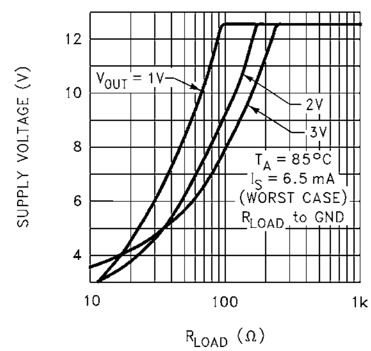


FIGURE 12.

EL2157 Macromodel

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* Revision A, July 1995
* When not being used, the clamp pin, pin 1,
* should be connected to +Vsupply, pin 7
* Connections:   +input
*                  |   -input
*                  |     |   +Vsupply
*                  |     |     |   -Vsupply
*                  |     |     |     |   output
*                  |     |     |     |     |   clamp
*                  |     |     |     |     |     |
.subckt EL2157/el  3     2     7     4     6     1
*
* Input Stage
*
i1 7 10 250uA
i2 7 11 250uA
r1 10 11 4k
q1 12 2 10 qp
q2 13 3 11 qpa
r2 12 4 100
r3 13 4 100
*
* Second Stage & Compensation
*
gm 15 4 13 12 4.6m
r4 15 4 15Meg
c1 15 4 0.36pF
*
* Poles
*
e1 17 4 15 4 1.0
r6 17 25 400
c3 25 4 1pF
r7 25 18 500
c4 18 4 1pF
*
* Output Stage & Clamp
*
i3 20 4 1.0mA
q3 7 23 20 qn
q4 7 18 19 qn
q5 7 18 21 qn
q6 4 20 22 qp
q7 7 23 18 qn
d1 19 20 da
d2 18 1 da
r8 21 6 2
r9 22 6 2
r10 18 21 10k
r11 7 23 100k
d3 23 24 da
d4 24 4 da
d5 23 18 da
*
* Power Supply Current
*
ips 7 4 3.2mA
*
* Models
```

```
*
.model qn npn(is=800e-18 bf=150 tf=0.02nS)
.model qpa pnp(is=810e-18 bf=50 tf=0.02nS)
.model qp pnp(is=800e-18 bf=54 tf=0.02nS)
.model da d(tt=0nS)
.ends
```

EL2157 Macromodel