HI3026A

August 1997

8-Bit, 140 MSPS, Flash A/D Converter

Features

- **Differential Linearity Error . . . . . ±0.5 LSB**
- **Integral Linearity Error . . . . . ±0.5 LSB**
- **Integral Linearity Compensation Circuit**
- **Low Input Capacitance 21pF**
- **Wide Analog Input Bandwidth 150MHz**
- **Low Power Consumption 790mW**
- **Internal $^1/_2$ Frequency Divider Circuit (With Reset Function)**
- **CLK/2 Clock Output Pin**
- **Compatible with ECL, PECL and TTL Digital Input Levels**
- **1:2 Demultiplexed Output**
- **Direct Replacement for Sony CXA3026A**

Applications

- **RGB Graphics Processing (LCD, PDP)**
- **Digital Oscilloscopes**
- **Digital Communications (QPSK, QAM)**
- **Magnetic Recording (PRML)**

Description

The HI3026A is an 8-bit, high-speed, flash analog-to-digital converter optimized for high speed, low power, and ease of use. With a 140 MSPS encode rate capability and full-power analog bandwidth of 150MHz, this component is ideal for applications requiring the highest possible dynamic performance.

To minimize system cost and power dissipation, only a +5V power supply is required. The HI3026A's clock input interfaces directly to TTL, ECL, or PECL logic and will operate with single-ended inputs. The user may select 16-bit demultiplexed output or 8-bit single-channel digital outputs. The demultiplexed mode interleaves the data through two 8-bit channels at $^1/_2$ the clock rate. Operation in demultiplexed mode reduces the speed and cost of external digital interfaces, while allowing the A/D converter to be clocked to the full 140 MSPS conversion rate.

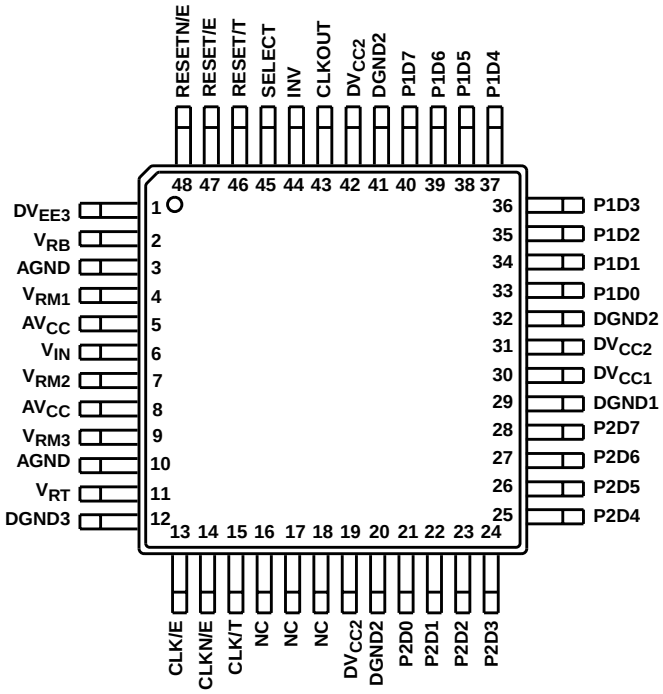
Fabricated with an advanced bipolar process, the HI3026A is provided in a space-saving 48-lead MQFP surface mount plastic package and is specified over the -20^{o}C to 75^{o}C temperature range.

Ordering Information

PART NUMBER	TEMPT. RANGE (^{o}C)	PACKAGE	PKG. NO.
HI3026AJCQ	-20 to 75	48 Ld MQFP	Q48.12x12-S
HI3026AEVAL	25	Evaluation Board	

Pinout

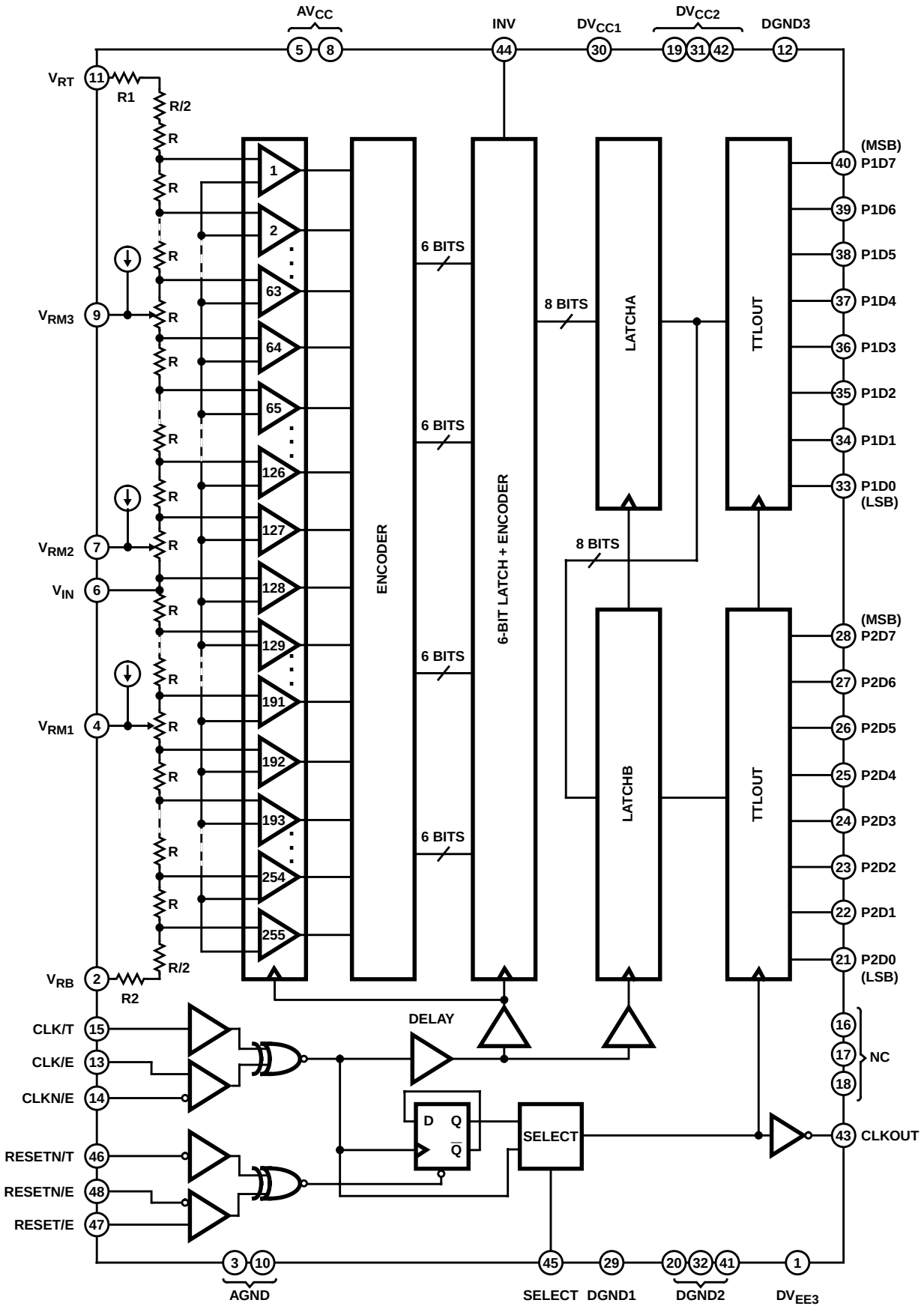
HI3026A (MQFP)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.

File Number **4246**

Block Diagram



Absolute Maximum Ratings $T_A = 25^oC$

Supply Voltage
- AV_{CC}, DV_{CC1}, DV_{CC2} . . . . . -0.5V to 7.0V
- DGND3 . . . . . -0.5V to 7.0V
- DV_{EE3} . . . . . -7.0V to 0.5V
- DGND3 - DV_{EE3} . . . . . -0.5V to 7.0V

Analog Input Voltage (V_{IN}) . . . . . V_{RT} - 2.7V to AV_{CC}

Reference Input Voltage
- V_{RT} . . . . . 2.7V to AV_{CC}
- V_{RB} . . . . . V_{IN} - 2.7V to AV_{CC}
- $|V_{RT} - V_{RB}|$ 2.5V

Digital Input Voltage
- ECL (***/E (Note 2)) . . . . . DV_{EE3} to 0.5V
- PECL (***/E) . . . . . -0.5V to DGND3
- TTL (***/T, INV) . . . . . -0.5V to DV_{CC1}
- Other (SELECT) . . . . . -0.5V to DV_{CC1}
- V_{ID} (|***/E - ***N/E| (Note 3)) 2.7V

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^oC/W$)
MQFP Package	63

Maximum Junction Temperature . . . . . 150^oC

Maximum Storage Temperature Range . . . . . -65^oC to 150^oC

Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(MQFP - Lead Tips Only)

Recommended Operating Conditions

WITH A SINGLE POWER SUPPLY	MIN	TYP	MAX
Supply Voltage			
DV_{CC1}, DV_{CC2}, AV_{CC}	+4.75	+5.0	+5.25V
DGND1, DGND2, AGND	-0.05	0	+0.05V
DGND3	+4.75	+5.0	+5.25V
DV_{EE3}	-0.05	0	+0.05V
Analog Input Voltage (V_{IN})	V_{RB}	-	V_{RT}
Reference Input Voltage			
V_{RT}	+2.9	-	+4.1V
V_{RB}	1.4	-	+2.6V
$\|V_{RT} - V_{RB}\|$	1.5	-	2.1V
Digital Input Voltage			
PECL (***/E) V_{IH}	DGND3 - 1.05		DGND3 - 1.4V
PECL (***/E) V_{IL}	DGND3 - 3.2		DGND3 - 1.4V
TTL (***/T, INV) V_{IH}	2.0V	-	-
TTL (***/T, INV) V_{IL}	-	-	0.8V
Other (SELECT) V_{IH}	-	DV_{CC1}	-
Other (SELECT) V_{IL}	-	DGND1	-
V_{ID} (Note 3) (|***/E- ***N/E|)	0.4	0.8	-
Max Conversion Rate (f_C, Straight Mode)	100	-	-
MSPS			
Max Conversion Rate (f_C, DMUX Mode)	140	-	-
MSPS			
Ambient Temperature (T_A)	-20^oC to 75^oC		

WITH DUAL POWER SUPPLIES	MIN	TYP	MAX
Supply Voltage			
DV_{CC1}, DV_{CC2}, AV_{CC}	+4.75	+5.0	+5.25V
DGND1, DGND2, AGND	-0.05	0	+0.05V
DGND3	-0.05	0	+0.05V
DV_{EE3}	-5.5	-5.0	-4.75V
Analog Input Voltage (V_{IN})	V_{RB}	-	V_{RT}
Reference Input Voltage			
V_{RT}	+2.9	-	+4.1V
V_{RB}	1.4	-	+2.6V
$\|V_{RT} - V_{RB}\|$	1.5	-	2.1V
Digital Input Voltage			
ECL (***/E) V_{IH} DGND3	DGND3 - 1.05		DGND3 - 0.5V
ECL (***/E) V_{IL} DGND3	DGND3 - 3.2		DGND3 - 1.4V
TTL (***/T, INV) V_{IH}	2.0V	-	-
TTL (***/T, INV) V_{IL}	-	-	0.8V
Other (SELECT) V_{IH}	-	DV_{CC1}	-
Other (SELECT) V_{IL}	-	DGND1	-
V_{ID} (Note 3) (|***/E- ***N/E|)	0.4	0.8	-
Max Conversion Rate (f_C, Straight Mode)	100	-	-
MSPS			
Max Conversion Rate (f_C, DMUX Mode)	140	-	-
MSPS			
Ambient Temperature (T_A)	-20^oC to 75^oC		

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.
2. ***/E and ***T indicate CLK/E and CLK/T, etc. for the pin name.
3. V_{ID}: Input Voltage Differential.

Electrical Specifications

$DV_{CC1, 2}$, AV_{CC}, DGND3 = +5V, DGND1, 2, AGND, DV_{EE3} = 0V, V_{RT} = 4V, V_{RB} = 2V, $T_A = 25^oC$

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Resolution			-	8	-	Bits
DC CHARACTERISTICS						
Integral Linearity Error	E_{IL}	$V_{IN} = 2V_{P-P}$, f_C = 5 MSPS	-	-	±0.5	LSB
Differential Linearity Error	E_{DL}		-	-	±0.5	LSB

Electrical Specifications $DV_{CC1, 2}$, AV_{CC}, DGND3 = +5V, DGND1, 2, AGND, DV_{EE3} = 0V, V_{RT} = 4V, V_{RB} = 2V, $T_A = 25^oC$ **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
ANALOG INPUT						
Analog Input Capacitance	C_{IN}	V_{IN} = +3.0V + 0.07V_{RMS}	-	21	-	pF
Analog Input Resistance	R_{IN}		4	-	50	kΩ
Analog Input Current	I_{IN}		0	-	500	µA
REFERENCE INPUT						
Reference Resistance (Note 4)	R_{REF}		75	115	155	Ω
Reference Current (Note 5)	I_{REF}		9.7	17.4	28	mA
Offset Voltage, V_{RT} Side	EOT		2	-	15	mV
Offset Voltage, V_{RB} Side	EOB		2	-	10	mV
DIGITAL INPUT (ECL, PECL)						
Digital Input Voltage: High	V_{IH}		DGND3 - 1.05	-	DGND3 - 0.5	V
Digital Input Voltage: Low	V_{IL}		DGND3 - 3.2	-	DGND3 - 1.4	V
Threshold Voltage	V_{TH}		-	DGND3 - 1.2	-	V
Digital Input Current: High	I_{IH}	V_{IH} = DGND3 - 0.8V	-50	-	+50	µA
Digital Input Current: Low	I_{IL}	V_{IL} = DGND3 - 1.6V	-75	-	0	µA
Digital Input Capacitance			-	-	5	pF
DIGITAL INPUT (TTL)						
Digital Input Voltage: High	V_{IH}		2.0	-	-	V
Digital Input Voltage: Low	V_{IL}		-	-	0.8	V
Threshold Voltage	V_{TH}		-	1.5	-	V
Digital Input Current: High	I_{IH}	V_{IH} = 3.5V	-50	-	0	µA
Digital Input Current: Low	I_{IL}	V_{IL} = 0.2V	-500	-	0	µA
Digital Input Capacitance			-	-	5	pF
DIGITAL OUTPUT (TTL)						
Digital Output Voltage: High	V_{OH}	I_{OH} = -2mA	2.4	-	-	V
Digital Output Voltage: Low	V_{OL}	I_{OL} = 1mA	-	-	0.5	V
SWITCHING CHARACTERISTICS						
Maximum Conversion Rate	f_C	DMUX Mode	140	-	-	MSPS
Aperture Jitter	t_{AJ}		-	10	-	ps
Sampling Delay	t_{DS}		3	4.5	6	ns
Clock High Pulse Width	t_{PW1}	CLK	2.8	-	-	ns
Clock Low Pulse Width	t_{PW0}	CLK	2.8	-	-	ns
Reset Pulse Width (Note 6)	t_{PWR}	RESETN	t x 2	-	-	ns
RESETN_CLK Setup	$t_{\_RST}$	RESETN-CLK	3.5	-	-	ns
CLKOUT Output Delay	t_{DCLK}	(CL = 5pF)	3.5	7	9	ns
Data Output Delay (Note 6)	t_{DO1}	DMUX Mode (C_L = 5pF)	t	t + 1	t + 2	ns
	t_{DO2}	(C_L = 5pF)	4.5	8	10	ns
Output Rise Time	t_r	0.8V to 2.0V (C_L = 5pF)	-	2	-	ns
Output Fall Time	t_f	0.8V to 2.0V (C_L = 5pF)	-	2	-	ns
DYNAMIC CHARACTERISTICS						
Input Bandwidth		V_{IN} = 2V_{P-P}, -3dB	150	-	-	MHz
S/N Ratio		f_C = 140 MSPS, f_{IN} = 1kHz Full Scale, DMUX Mode	-	46	-	dB
		f_C = 140 MSPS, f_{IN} = 34.999MHz Full Scale, DMUX Mode	-	40	-	dB

Electrical Specifications $DV_{CC1, 2}$, AV_{CC}, DGND3 = +5V, DGND1, 2, AGND, DV_{EE3} = 0V, V_{RT} = 4V, V_{RB} = 2V, $T_A = 25^oC$ **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Error Rate		f_C = 140 MSPS, f_{IN} = 1kHz Full Scale, DMUX Mode, Error > 16 LSB	-	-	10^{-12}	TPS
		f_C = 140 MSPS, f_{IN} = 34.999MHz Full Scale, DMUX Mode, Error > 16 LSB	-	-	10^{-9}	TPS
		f_C = 100 MSPS, f_{IN} = 24.999MHz Full Scale, Straight Mode, Error > 16 LSB	-	-	10^{-9}	TPS (Note 7)
POWER SUPPLY						
Supply Current	I_{CC}		130	150	190	mA
Supply Current	I_{EE}		0.4	0.6	0.8	mA
Power Consumption (Note 8)	P_D		690	790	990	mW

NOTES:

4. R_{REF}: Resistance value between V_{RT} and V_{RB}.
5. $I_{REF} = \frac{V_{RT} - V_{RB}}{R_{REF}}$.
6. $t = \frac{1}{f_C}$.
7. TPS = Times Per Sample.
8. $P_D = (I_{CC} + I_{EE}) \bullet V_{CC} + \frac{(V_{RT} - V_{RB})^2}{V_{REF}}$.

Timing Waveforms

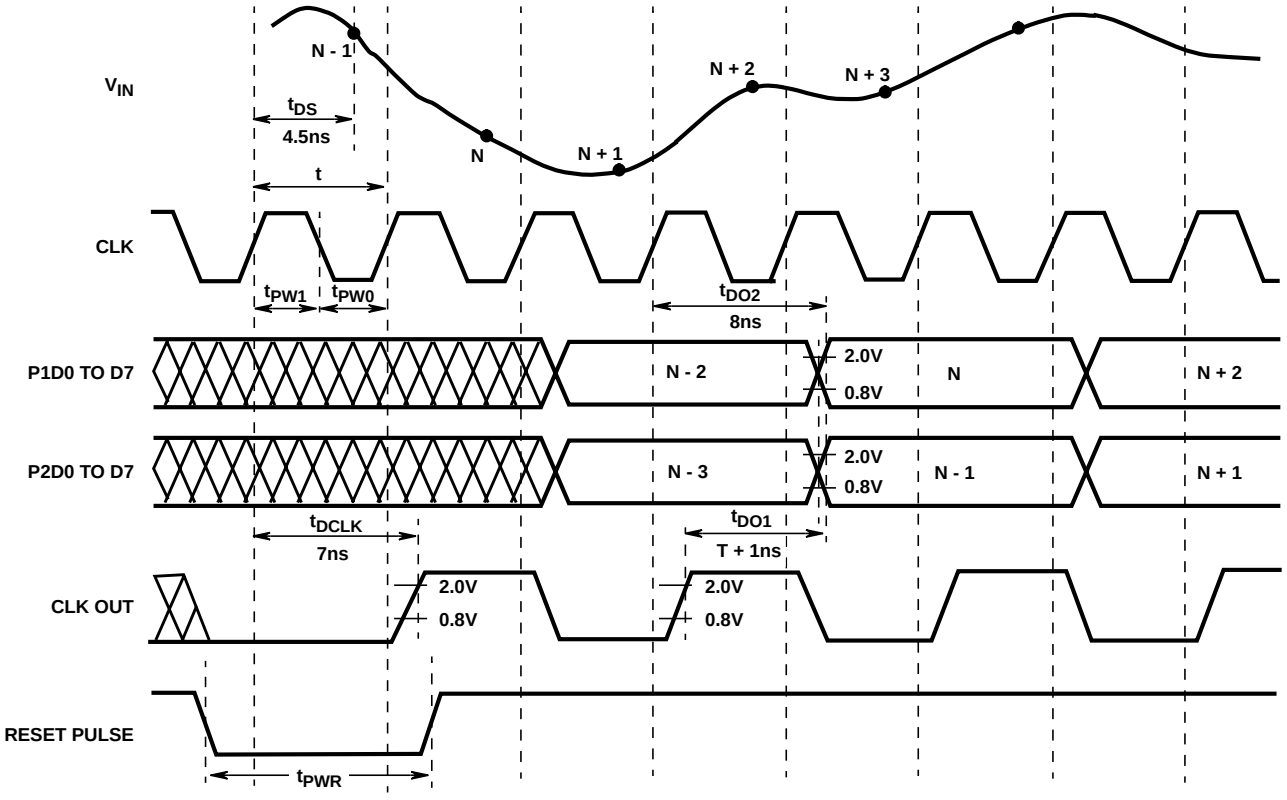


FIGURE 1. DEMUX MODE TIMING CHART (SELECT = V_{CC})

Timing Waveforms (Continued)

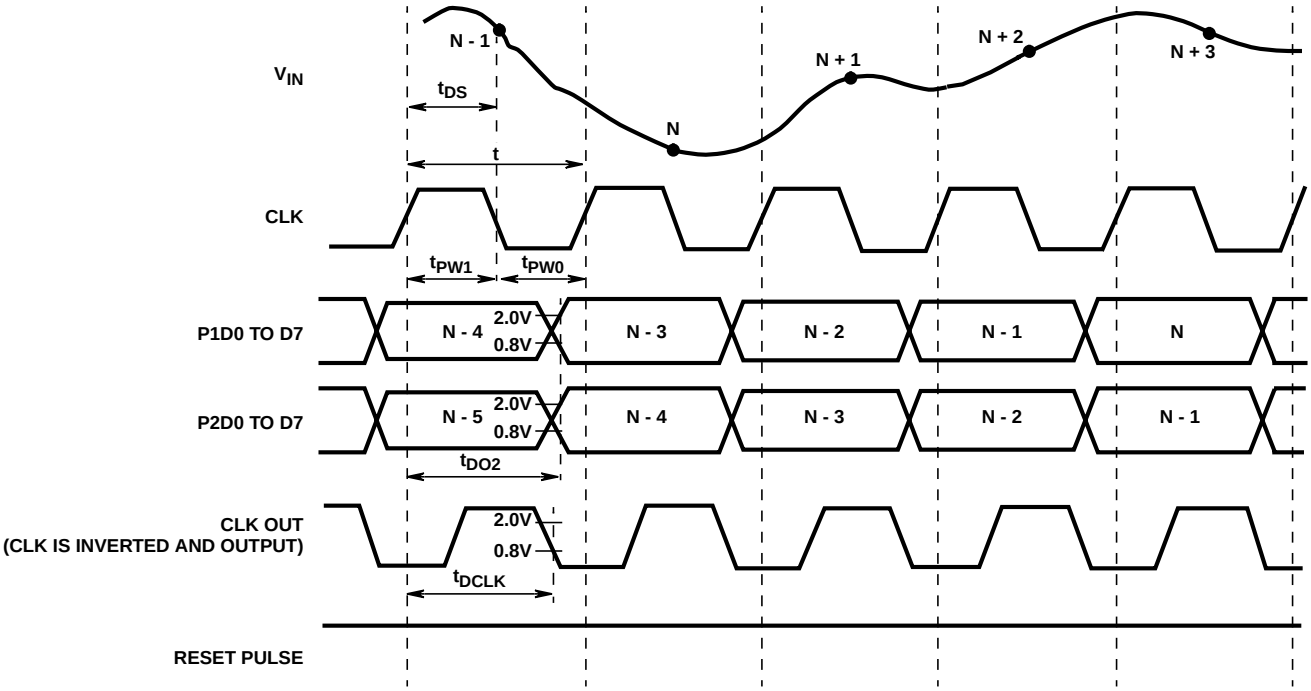


FIGURE 2. STRAIGHT MODE TIMING CHART (SELECT = GND)

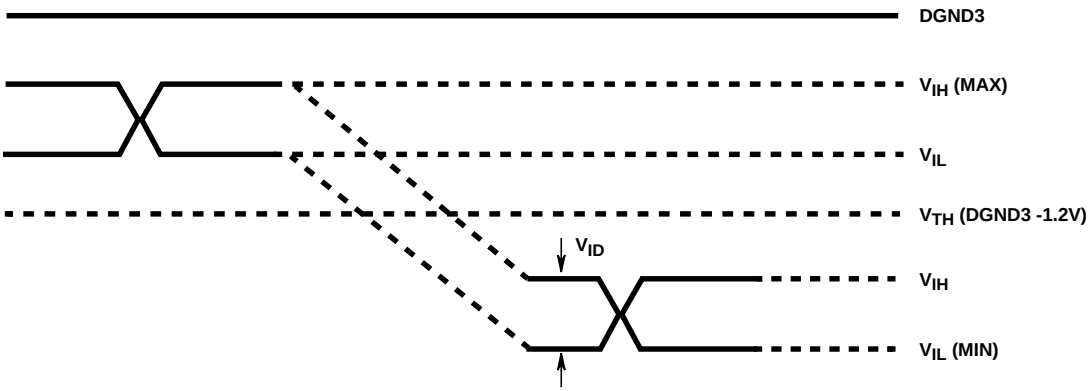
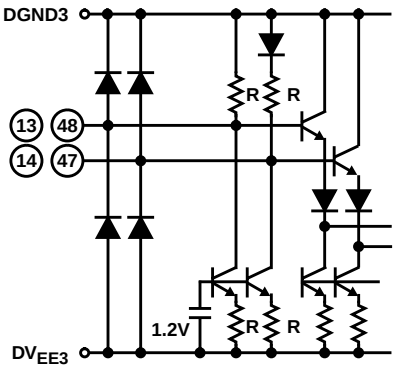
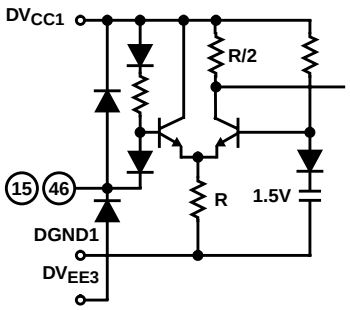
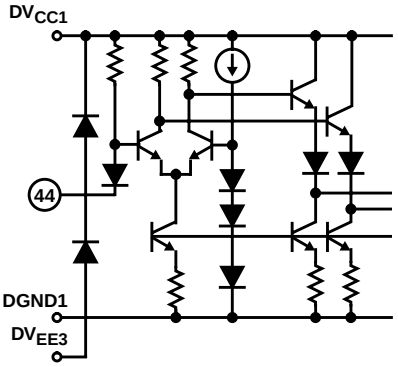


FIGURE 3. ECL AND PECL SWITCHING LEVEL

Pin Descriptions

PIN NO	SYMBOL	I/O	TYPICAL VOLTAGE LEVEL	EQUIVALENT CIRCUIT	DESCRIPTION
3, 10	AGND		GND		Analog Ground. Separated from the digital ground.
5, 8	AV_{CC}		+5V (Typ)		Analog Power Supply. Separated from the digital power supply.
20, 29 32, 41	DGND1 DGND2		GND		Digital Ground.
19, 30 31, 42	DV_{CC1} DV_{CC2}		+5V (Typ)		Digital Power Supply.

Pin Descriptions (Continued)

PIN NO	SYMBOL	I/O	TYPICAL VOLTAGE LEVEL	EQUIVALENT CIRCUIT	DESCRIPTION
12	DGND3		+5V (Typ) (With a Single Power Supply) GND (With Dual Power Supplies)		Digital Power Supply. Ground for ECL input. +5V for PECL and TTL input.
1	DV_{EE3}		GND (With a Single Power Supply) -5V (Typ) (With Dual Power Supplies)		Digital Power Supply. -5V for ECL input. Ground for PECL and TTL Input
16, 17, 18	NC				No Connect pin. Not connected with the internal circuits.
13	CLK/E	I	ECL/PECL		Clock Input.
14	CLKN/E	I			CLK/E Complementary Input. When left open, this pin goes to the threshold potential. Only CLK/E can be used for operation, but complementary input is recommended to attain fast and stable operation.
48	RESETN/E	I			Reset Input. When the input is set to low level, the built-in CLK frequency divider circuit can be reset.
47	RESET/E	I			RESETN/E Complementary Input. When left open, this pin goes to the threshold voltage. Only RESETN/E can be used for operation.
15	CLK/T	I	TTL		Clock Input.
46	RESETN/T	I			Reset Input. When left open, this input goes to high level. When the input is set to low level, the built-in CLK frequency divider circuit can be reset.
44	INV	I	TTL		Data Output Polarity Inversion Input. When left open, this input goes to high level. (See Table 1, I/O Correspondence Table.)

Pin Descriptions (Continued)

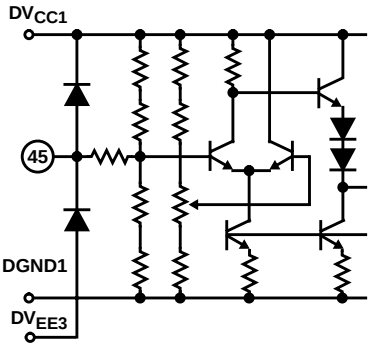
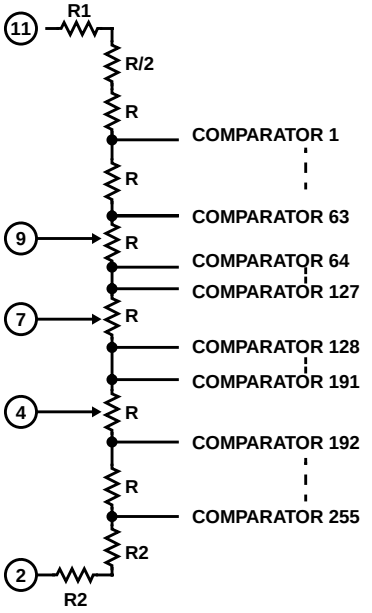
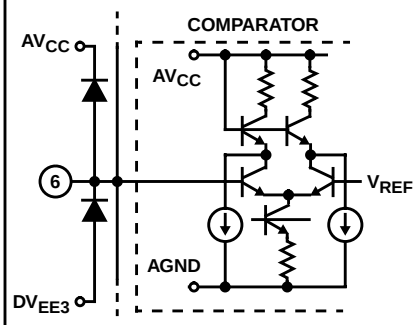
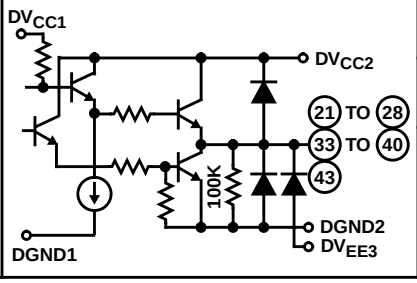
PIN NO	SYMBOL	I/O	TYPICAL VOLTAGE LEVEL	EQUIVALENT CIRCUIT	DESCRIPTION
45	SELECT		V_{CC} or GND		Data Output Mode Selection. (See Table 2, Operating Mode Table.)
11	V_{RT}	I	4.0V (Typ)		Top Reference Voltage. By-pass to AGND with a 1µF tantal capacitor and a 0.1µF chip capacitor.
9	V_{RM3}		$V_{RB} + \frac{3}{4}(V_{RT} - V_{RB})$		Reference Voltage Mid Point. Bypass to AGND with a 0.1µF chip capacitor.
7	V_{RM2}		$V_{RB} + \frac{2}{4}(V_{RT} - V_{RB})$		Reference Voltage Mid Point. Bypass to AGND with a 0.1µF chip capacitor.
4	V_{RM1}		$V_{RB} + \frac{1}{4}(V_{RT} - V_{RB})$		Reference Voltage Mid Point. Bypass to AGND with a 0.1µF chip capacitor.
2	V_{RB}	I	2.0V (Typ)		Bottom Reference Voltage. Bypass to AGND with a 1µF tantal capacitor and a 0.1µF chip capacitor.
6	V_{IN}	I	V_{RT} to V_{RB}		Analog Input.
33 to 40	P1D0 to P1D7	O	TTL		Port 1 Side Data Output.
21 to 28	P2D0 to P2D7	O			Port 2 Side Data Output.
43	CLKOUT	O			Clock Output. (See Table 2, Operating Mode Table.)

TABLE 1. A/D CODE TABLE

V_{IN}	STEP	INV															
		1								0							
		D7							D0	D7							D0
V_{RT}	255	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	254	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1
	•				•								•				
	•				•								•				
	•				•								•				
V_{RM2}	128	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1
	127	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0
	•				•								•				
	•				•								•				
	•				•								•				
	1	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0
V_{RB}	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Notes On Operation

- The HI3026A is a high-speed A/D converter which is capable of TTL, ECL and PECL level clock input. Characteristic impedance should be properly matched to ensure optimum performance during high-speed operation.
- The power supply and grounding have a profound influence on converter performance. The power supply and grounding method are particularly important during high-speed operation. General points for caution are as follows:
  - The ground pattern should be as large as possible. It is recommended to make the power supply and ground patterns wider at an inner layer using a multi-layer board.
  - To prevent interference between AGND and DGND and between AV_{CC} and DV_{CC}, make sure the respective patterns are separated. To prevent a DC offset in the power supply pattern, connect the AV_{CC} and DV_{CC} lines at one point each via a ferrite-bead filter. Shorting the AGND and DGND patterns in one place immediately under the A/D converter improves A/D converter performance.
  - Ground the power supply pins (AV_{CC}, DV_{CC1}, DV_{CC2}, DV_{EE3}) as close to each pin as possible with a 0.1µF or larger ceramic chip capacitor. (Connect the AV_{CC} pin to the AGND pattern and the DV_{CC1}, DV_{CC2}, DV_{EE3} pins to the DGND pattern.)
  - The digital output wiring should be as short as possible. If the digital output wiring is long, the wiring capacitance will increase, deteriorating the output slew rate and resulting in reflection to the output waveform since the original output slew rate is quite fast.
- The analog input pin V_{IN} has an input capacitance of approximately 21pF. To drive the A/D converter with proper frequency response, it is necessary to prevent performance deterioration due to parasitic capacitance or parasitic inductance by using a large capacity drive circuit, keeping wiring as short as possible, and using chip parts for resistors and capacitors, etc.
- The V_{RT} and V_{RB} pins must have adequate bypass to protect them from high-frequency noise. Bypass them to AGND with approximately 1µF tantal capacitor and, 0.1µF capacitor as short as possible.
- When the digital input level is ECL or PECL level, ***/E pins should be used and ***/T pins left open. When the digital input level is TTL, ***/T pins should be used and III/E pins left open.

Test Circuits

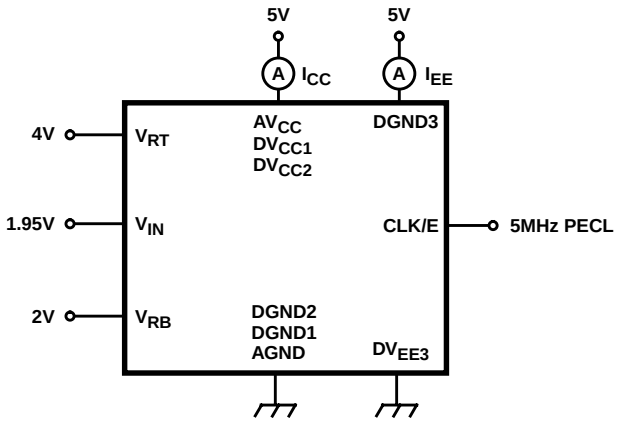


FIGURE 4. CURRENT CONSUMPTION MEASUREMENT CIRCUIT

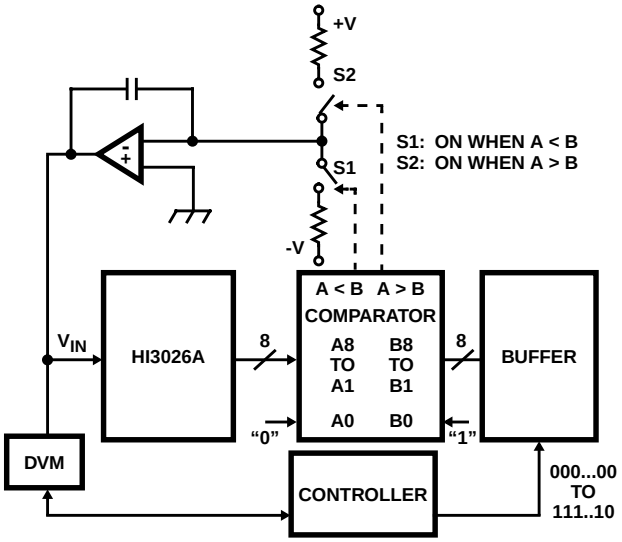


FIGURE 5. INTEGRAL LINEARITY ERROR/DIFFERENTIAL LINEARITY ERROR MEASUREMENT CIRCUIT

Test Circuits (Continued)

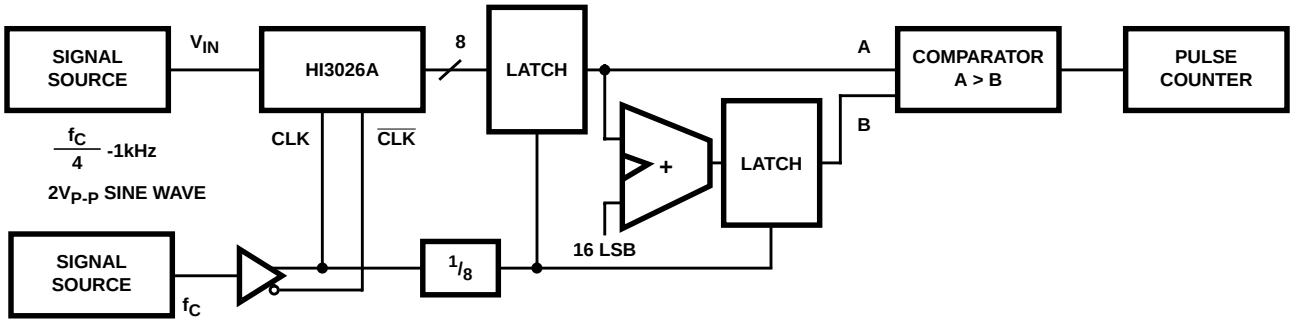


FIGURE 6. ERROR RATE MEASUREMENT CIRCUIT

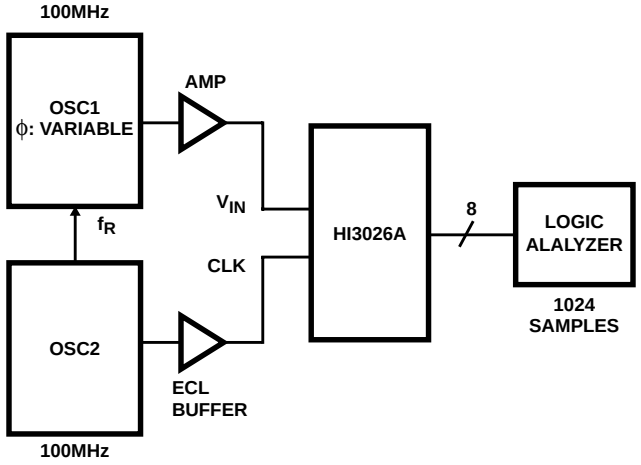
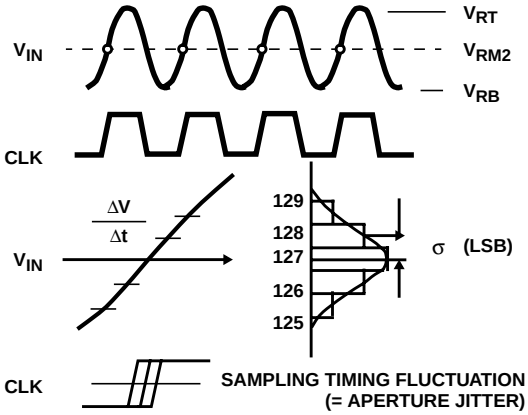


FIGURE 7. SAMPLING DELAY/APERTURE JITTER MEASUREMENT CIRCUIT



NOTE: Where σ (LSB) is the deviation of the output codes when the largest slew rate point is sampled at the clock which has exactly the same frequency as the analog input signal, the aperture jitter, t_{AJ} is:

$$t_{AJ} = \left(\frac{\sigma/\Delta V}{\Delta t}\right) = \sigma/\left(\frac{256}{2} \times 2\pi f\right).$$

FIGURE 8. APERTURE JITTER MEASUREMENT METHOD

Operating Modes

The HI3026A has two types of operating modes which are selected with Pin 45 (SELECT).

TABLE 2. OPERATING MODE TABLE

OPERATING MODE	SELECT	MAXIMUM CONVERSION RATE	DATA OUTPUT	CLOCK OUTPUT
DMUX Mode	V_{CC}	140 MSPS	Demultiplexed Output 70 Mbps	The input clock is $^1/_2$ frequency divided and output at 70MHz.
Straight Mode	GND	100 MSPS	Straight Output 100 Mbps	The input clock is inverted and output at 100MHz.

DMUX Mode (See Application Circuits, Figures 18, 19, 20)

Set the SELECT pin to V_{CC} for this mode. In this mode, the clock frequency is divided by 2 in the IC, and the data is output after being demultiplexed by this $^1/_2$ frequency divided clock. The $^1/_2$ frequency divided clock, which has adequate setup time and hold time for the output data, is output from the CLKOUT pin.

When using multiple HI3026A units in parallel in this mode, differences in the start timing of the $^1/_2$ frequency divided clock may cause operation as shown in the figure below. As a countermeasure, the HI3026A is equipped with a function which resets the $^1/_2$ frequency divided clock. When resetting this clock, the RESET pulse must be input to the RESET pin. See the Timing Charts for the RESET pulse input timing. The A/D converter can operate at f_C (Min) = 140 MSPS in this mode.

Straight Mode (See Application Circuits, Figures 21, 22, 23)

Set the SELECT pin to GND for this mode. In this mode, data output can be obtained in accordance with the clock frequency applied to the A/D converter for applications which use the clock applied to the A/D converter as the system clock.

The A/D converter can operate at f_C (Min) = 100 MSPS in this mode.

Digital Input Level and Supply Voltage Settings

The logic input level for the HI3026A supports ECL, PECL and TTL levels.

The power supplies (DV_{EE3}, DGND3) for the logic input block must be set to match the logic input (CLK and RESET signals) level.

TABLE 3. LOGIC INPUT LEVEL AND POWER SUPPLY SETTINGS

DIGITAL INPUT LEVEL	DV_{EE3}	DGND3	SUPPLY VOLTAGE	APPLICATION CIRCUITS (FIGURE)	
ECL	-5V	0V	±5V	(18)	(21)
PECL	0V	+5V	+5V	(19)	(22)
TTL	0V	+5V	+5V	(20)	(23)

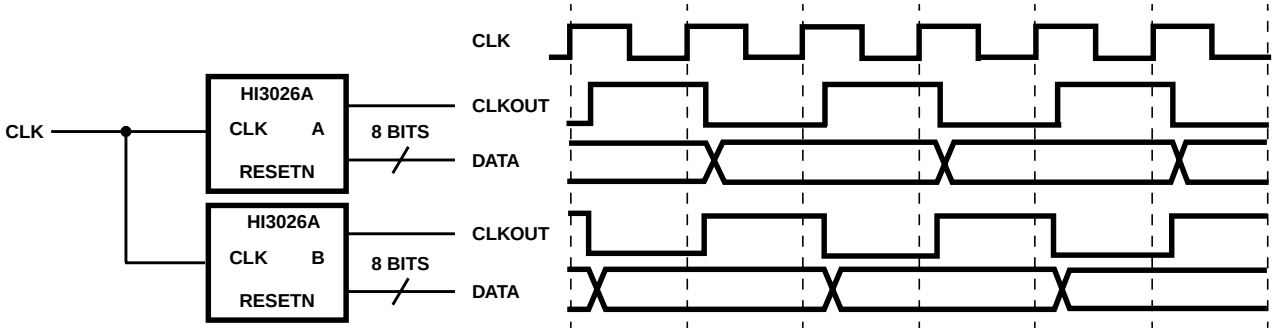


FIGURE 9. WHEN THE RESET PULSE IS NOT USED

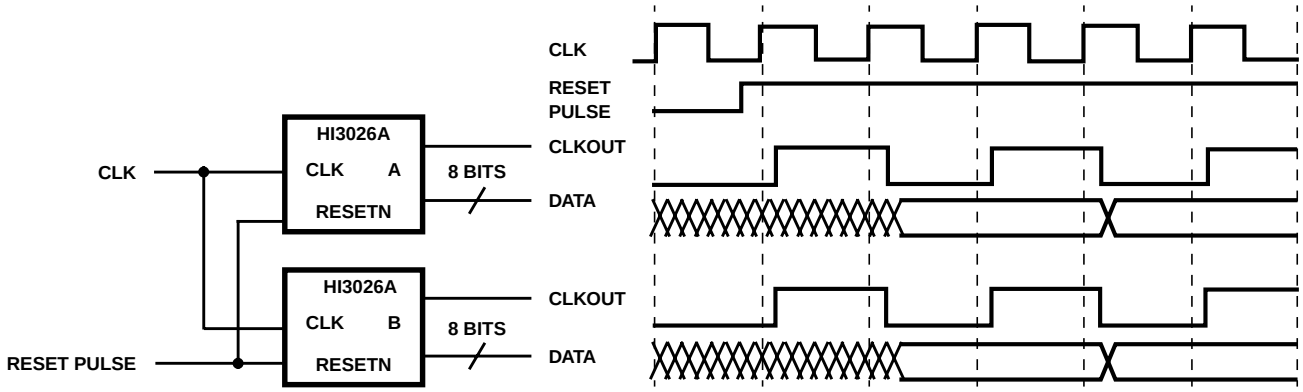


FIGURE 10. WHEN THE RESET PULSE IS USED

Typical Performance Curves

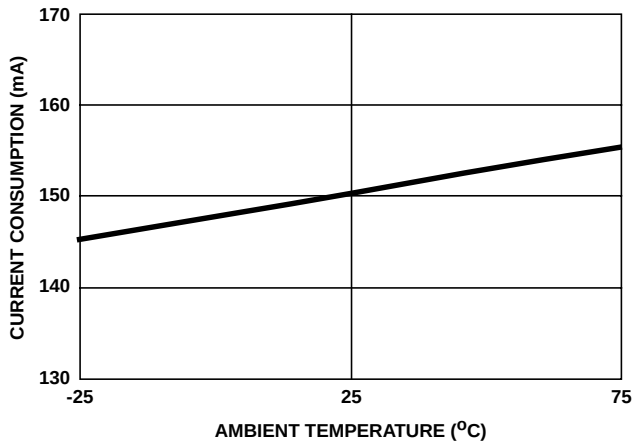


FIGURE 11. CURRENT CONSUMPTION vs AMBIENT TEMPERATURE CHARACTERISTICS

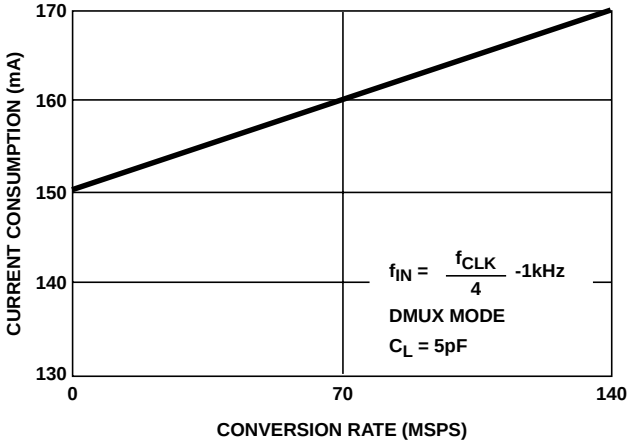


FIGURE 12. CURRENT CONSUMPTION vs CONVERSION RATE CHARACTERISTICS RESPONSE

Typical Performance Curves (Continued)

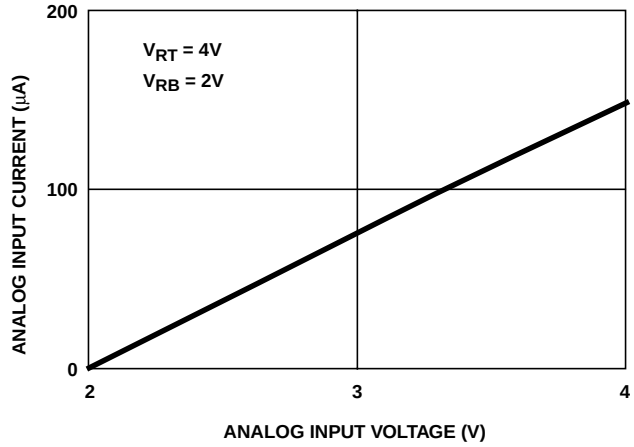


FIGURE 13. ANALOG INPUT CURRENT vs ANALOG INPUT VOLTAGE CHARACTERISTICS

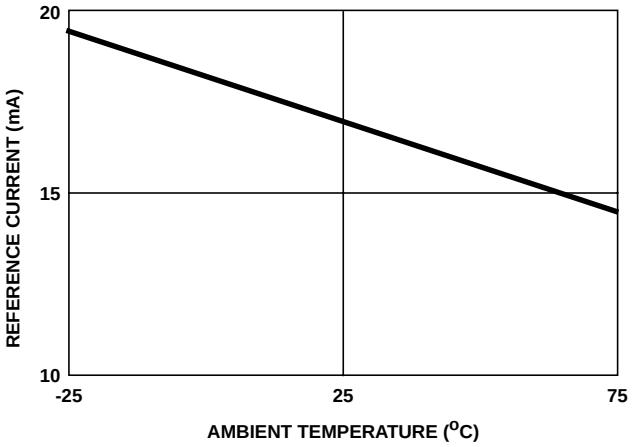


FIGURE 14. REFERENCE CURRENT vs AMBIENT TEMPERATURE CHARACTERISTICS

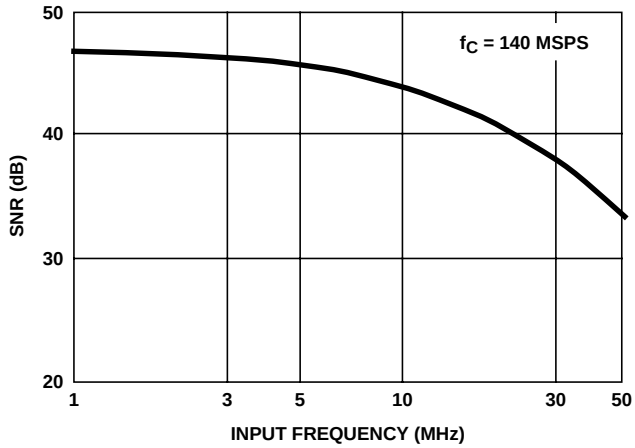


FIGURE 15. SNR vs INPUT FREQUENCY RESPONSE

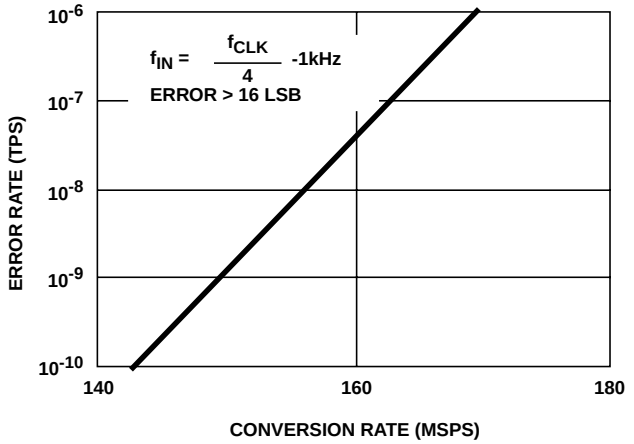


FIGURE 16. ERROR RATE vs CONVERSION RATE CHARACTERISTICS

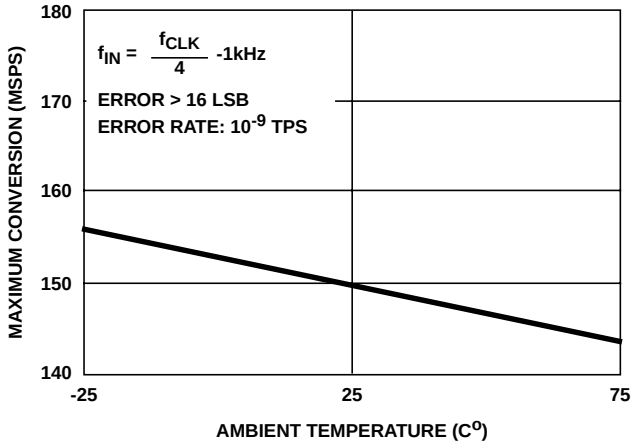


FIGURE 17. MAXIMUM CONVERSION RATE vs AMBIENT TEMPERATURE CHARACTERISTICS

Typical Application Circuits

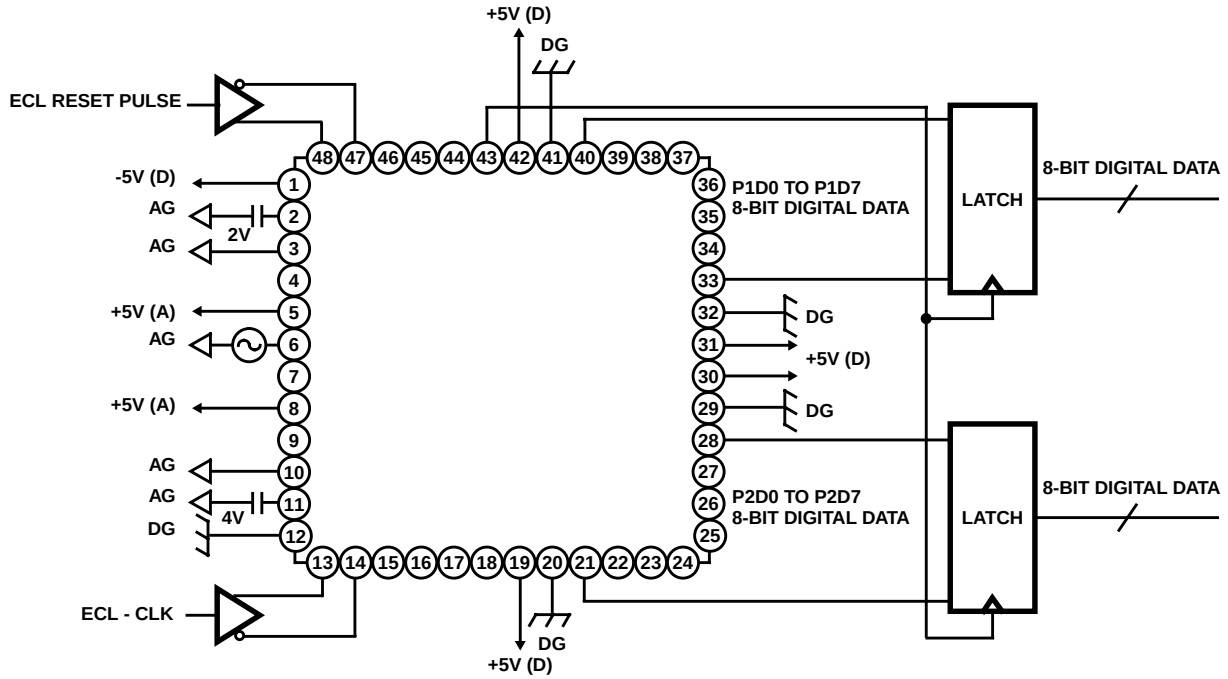


FIGURE 18. DMUX ECL INPUT

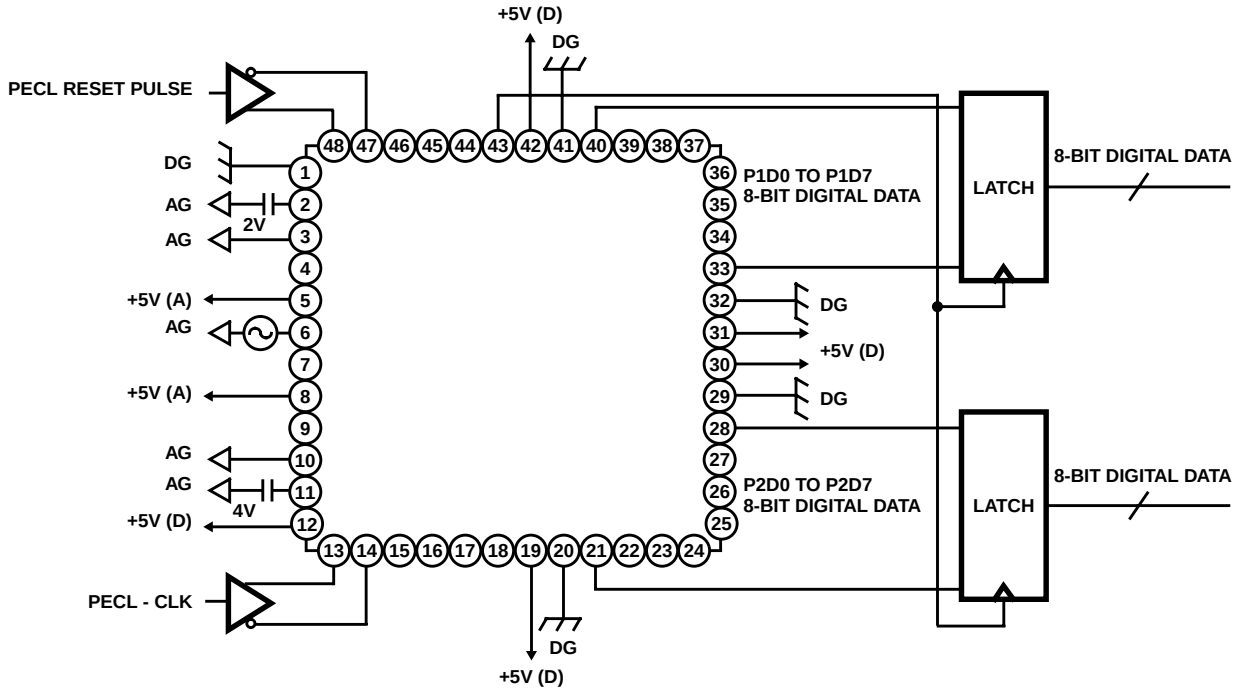


FIGURE 19. DMUX PECL INPUT

Typical Application Circuits (Continued)

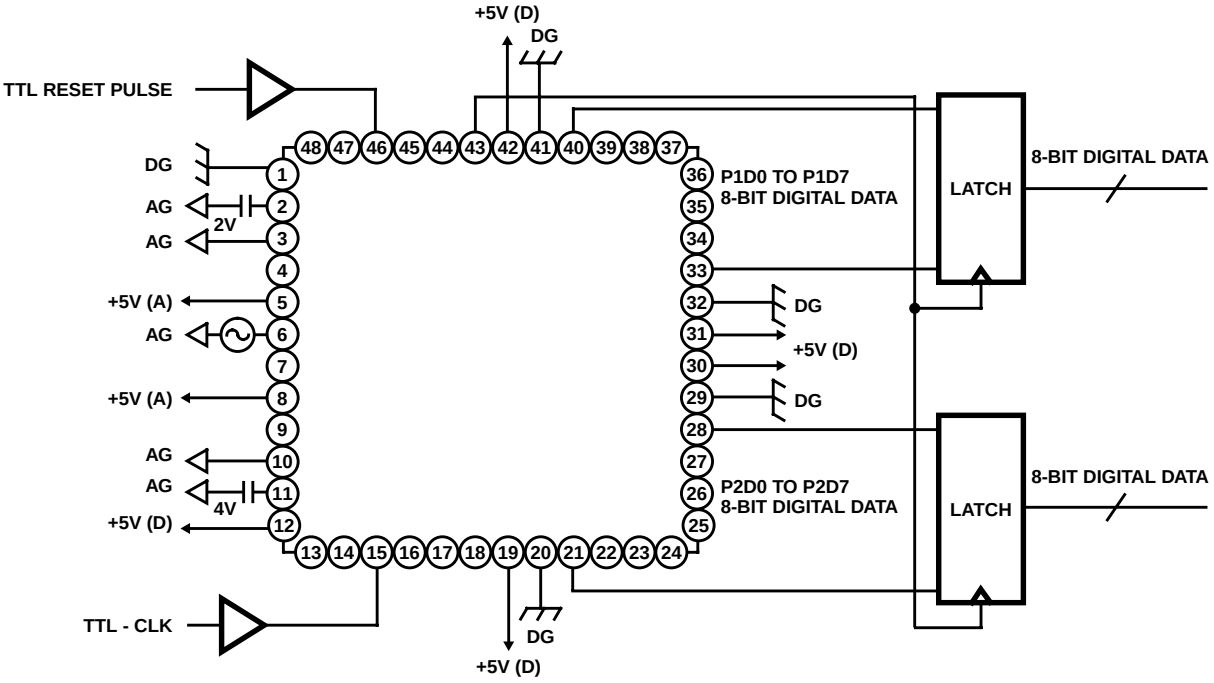


FIGURE 20. DMUX TTL INPUT

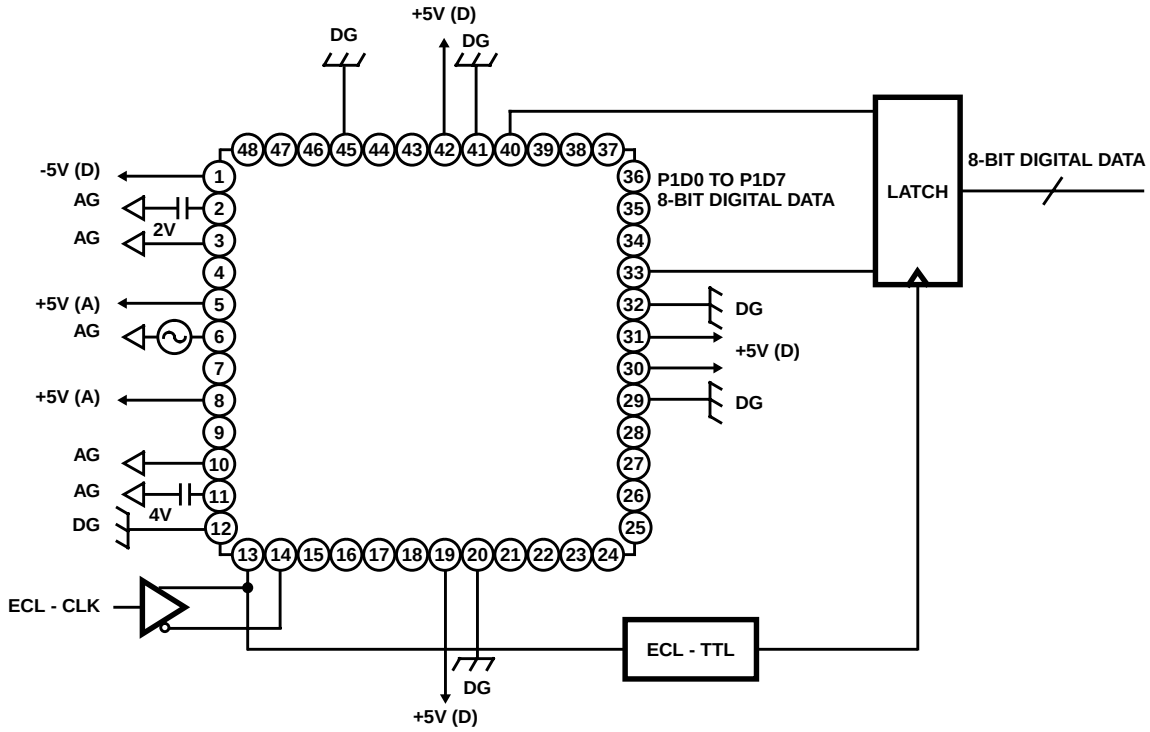


FIGURE 21. STRAIGHT ECL INPUT

Typical Application Circuits (Continued)

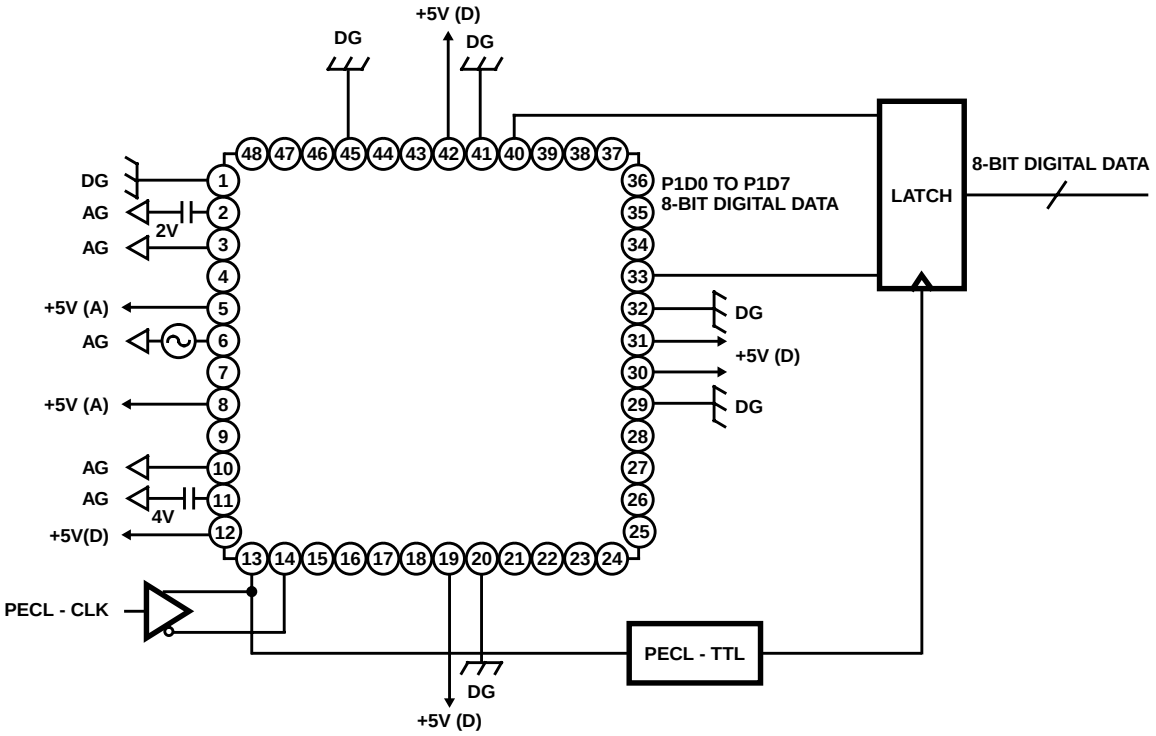


FIGURE 22. STRAIGHT PECL INPUT

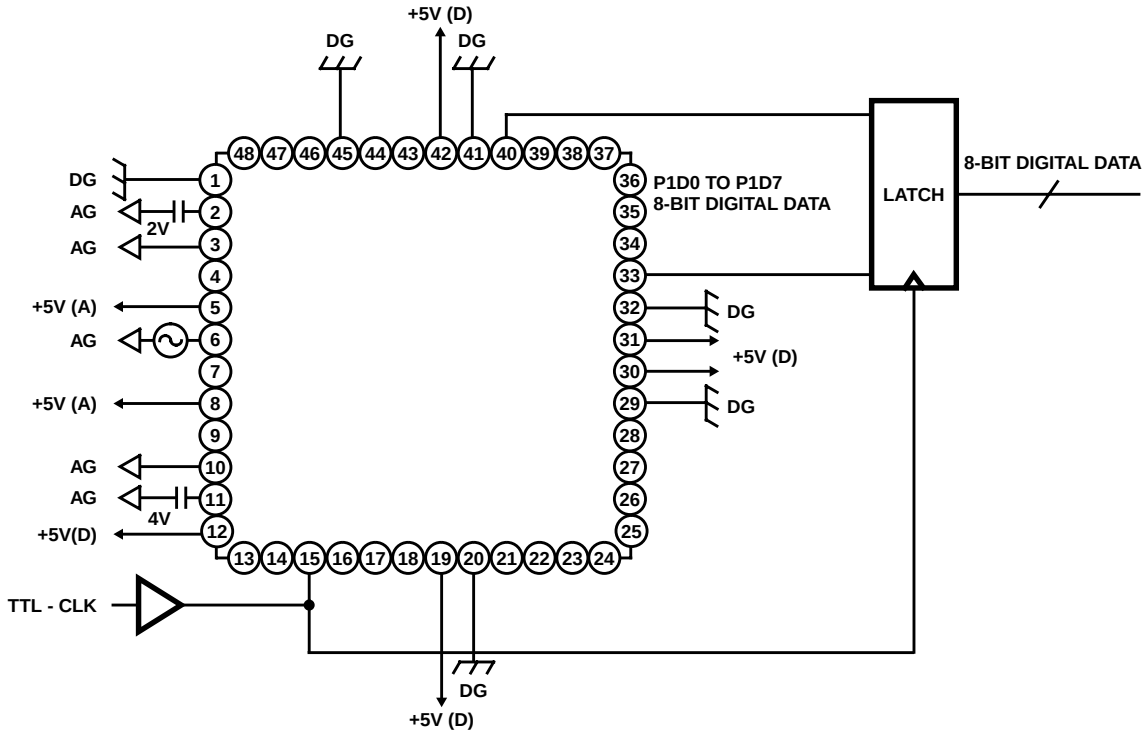


FIGURE 23. STRAIGHT TTL INPUT

Typical Application Circuits (Continued)

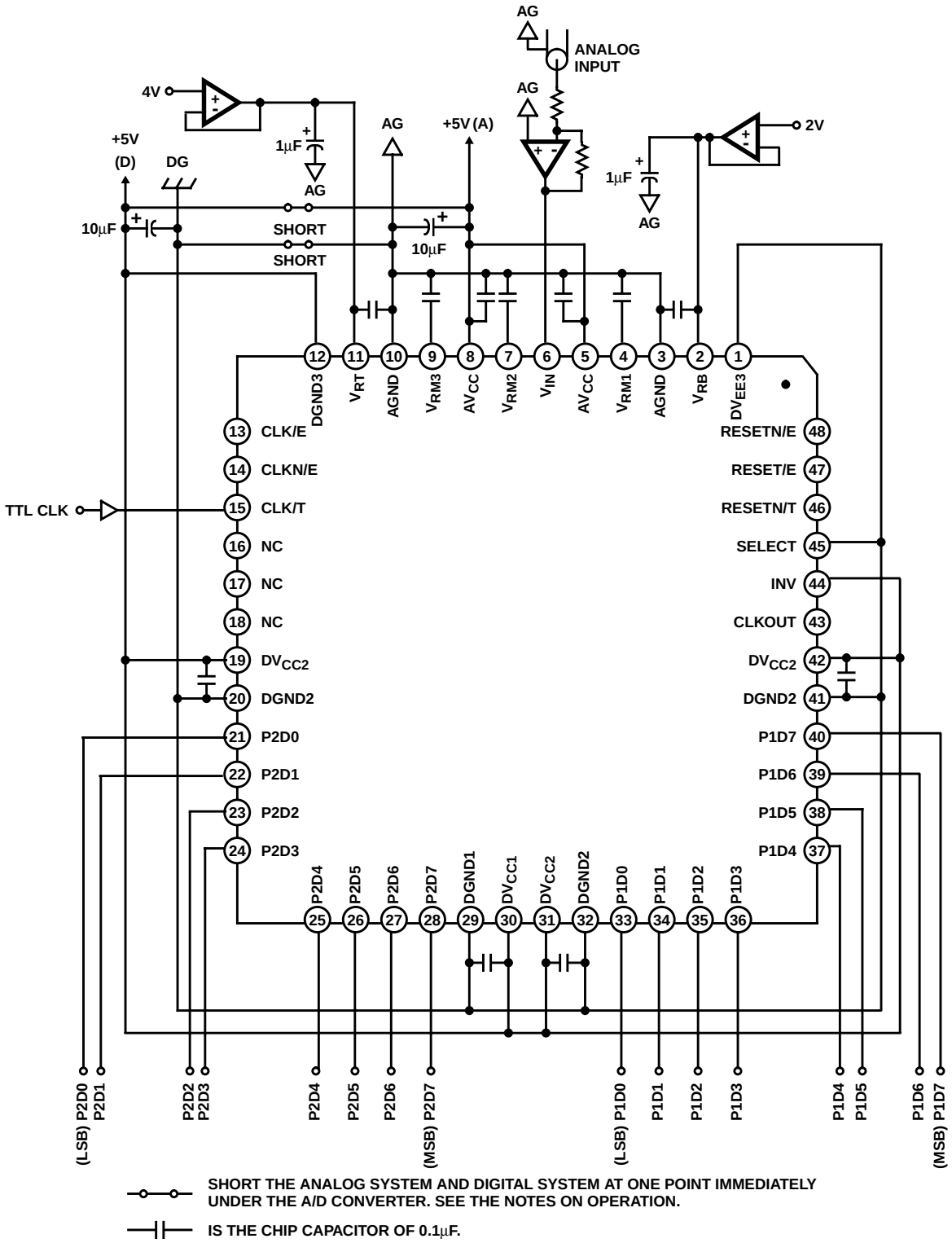


FIGURE 24. STRAIGHT MODE TTL I/O (WHEN A SINGLE POWER SUPPLY IS USED)

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