

**+/-15kV, ESD-Protected, +5V Powered,  
RS-232 Transmitters/Receivers**

The HIN202E, HIN206E, HIN207E, HIN208E, HIN211E, HIN213E, HIN232E family of RS-232 transmitters/receivers interface circuits meet all EIA high-speed RS-232E and V.28 specifications, and are particularly suited for those applications where  $\pm 12V$  is not available. A redesigned transmitter circuit improves data rate and slew rate, which makes this suitable for ISDN and high speed modems. The transmitter outputs and receiver inputs are protected to  $\pm 15kV$  ESD (Electrostatic Discharge). They require a single +5V power supply and feature onboard charge pump voltage converters which generate +10V and -10V supplies from the 5V supply. The family of devices offers a wide variety of high-speed RS-232 transmitter/receiver combinations to accommodate various applications (see Selection Table).

The HIN206E, HIN211E and HIN213E feature a low power shutdown mode to conserve energy in battery powered applications. In addition, the HIN213E provides two active receivers in shutdown mode allowing for easy "wake-up" capability.

The drivers feature true TTL/CMOS input compatibility, slew rate-limited output, and  $300\Omega$  power-off source impedance. The receivers can handle up to  $\pm 30V$  input, and have a  $3k\Omega$  to  $7k\Omega$  input impedance. The receivers also feature hysteresis to greatly improve noise rejection.

**Features**

- Pb-Free Available as an Option (See Ordering Info)
- High Speed ISDN Compatible . . . . . 230kbits/s
- ESD Protection for RS-232 I/O Pins to  $\pm 15kV$  (IEC1000)
- Meets All RS-232E and V.28 Specifications
- Requires Only 0.1 $\mu F$  or Greater External Capacitors
- Two Receivers Active in Shutdown Mode (HIN213E)
- Requires Only Single +5V Power Supply
- Onboard Voltage Doubler/Inverter
- Low Power Consumption (Typ) . . . . . 5mA
- Low Power Shutdown Function (Typ) . . . . . 1 $\mu A$
- Three-State TTL/CMOS Receiver Outputs
- Multiple Drivers
  - $\pm 10V$  Output Swing for +5V Input
  - $300\Omega$  Power-Off Source Impedance
  - Output Current Limiting
  - TTL/CMOS Compatible
- Multiple Receivers
  - $\pm 30V$  Input Voltage Range
  - $3k\Omega$  to  $7k\Omega$  Input Impedance
  - 0.5V Hysteresis to Improve Noise Rejection

**Applications**

- Any System Requiring High-Speed RS-232 Communications Port
  - Computer - Portable, Mainframe, Laptop
  - Peripheral - Printers and Terminals
  - Instrumentation, UPS
  - Modems, ISDN Terminal Adaptors

**Selection Table**

PART NUMBER	POWER SUPPLY VOLTAGE	NUMBER OF RS-232 DRIVERS	NUMBER OF RS-232 RECEIVERS	NUMBER OF 0.1 $\mu F$ EXTERNAL CAPACITORS	LOW POWER SHUTDOWN/TTL THREE-STATE	NUMBER OF RECEIVERS ACTIVE IN SHUTDOWN
HIN202E	+5V	2	2	4 Capacitors	No/No	0
HIN206E	+5V	4	3	4 Capacitors	Yes/Yes	0
HIN207E	+5V	5	3	4 Capacitors	No/No	0
HIN208E	+5V	4	4	4 Capacitors	No/No	0
HIN211E	+5V	4	5	4 Capacitors	Yes/Yes	0
HIN213E	+5V	4	5	4 Capacitors	Yes/Yes	2
HIN232E	+5V	2	2	4 Capacitors	No/No	0

**Ordering Information**

PART NO.	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
HIN202ECB	0 to 70	16 Ld SOIC (W)	M16.3
HIN202ECBN	0 to 70	16 Ld SOIC (N)	M16.15
HIN202ECBN-T	0 to 70	16 Ld SOIC (N) Tape and Reel	M16.15
HIN202ECBNZ (See Note)	0 to 70	16 Ld SOIC (N) (Pb-free)	M16.15
HIN202ECBNZ-T (See Note)	0 to 70	16 Ld SOIC (N) Tape and Reel (Pb-free)	M16.15
HIN202ECP	0 to 70	16 Ld PDIP	E16.3
HIN202EIB	-40 to 85	16 Ld SOIC (W)	M16.3
HIN202EIB-T	-40 to 85	16 Ld SOIC (W) Tape and Reel	M16.3
HIN202EIBN	-40 to 85	16 Ld SOIC (N)	M16.15
HIN202EIBN-T	-40 to 85	16 Ld SOIC (N) Tape and Reel	M16.15
HIN202EIBNZ (See Note)	-40 to 85	16 Ld SOIC (N) (Pb-free)	M16.15
HIN202EIBNZ-T (See Note)	-40 to 85	16 Ld SOIC (N) Tape and Reel (Pb-free)	M16.15
HIN206ECB-T	0 to 70	24 Ld SOIC Tape and Reel	M24.3
HIN206EIA	-40 to 85	24 Ld SSOP	M24.209
HIN207ECA-T	0 to 70	24 Ld SSOP Tape and Reel	M24.209
HIN207ECB	0 to 70	24 Ld SOIC	M24.3
HIN207ECB-T	0 to 70	24 Ld SOIC Tape and Reel	M24.3
HIN207ECBZ (See Note)	0 to 70	24 Ld SOIC (Pb-free)	M24.3
HIN207ECBZ-T (See Note)	0 to 70	24 Ld SOIC Tape and Reel (Pb-free)	M24.3
HIN207EIB	-40 to 85	24 Ld SOIC	M24.3
HIN207EIB-T	-40 to 85	24 Ld SOIC Tape and Reel	M24.3
HIN208ECA	0 to 70	24 Ld SSOP	M24.209
HIN208ECA-T	0 to 70	24 Ld SSOP Tape and Reel	M24.209
HIN208ECB	0 to 70	24 Ld SOIC	M24.3
HIN208ECB-T	0 to 70	24 Ld SOIC Tape and Reel	M24.3
HIN208EIA	-40 to 85	24 Ld SSOP	M24.209
HIN208EIB	-40 to 85	24 Ld SOIC	M24.3
HIN211ECA	0 to 70	28 Ld SSOP	M28.209

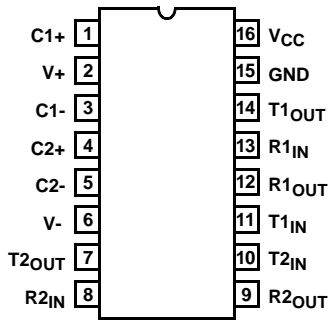
**Ordering Information (Continued)**

PART NO.	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
HIN211ECA-T	0 to 70	28 Ld SSOP Tape and Reel	M28.209
HIN211ECB	0 to 70	28 Ld SOIC	M28.3
HIN211EIA	-40 to 85	28 Ld SSOP	M28.209
HIN211EIB	-40 to 85	28 Ld SOIC	M28.3
HIN213ECA	0 to 70	28 Ld SSOP	M28.209
HIN213ECA-T	0 to 70	28 Ld SSOP Tape and Reel	M28.209
HIN213EIA	-40 to 85	28 Ld SSOP	M28.209
HIN213EIA-T	-40 to 85	28 Ld SSOP Tape and Reel	M28.209
HIN213EIB	-40 to 85	28 Ld SOIC	M28.3
HIN232ECA-T	0 to 70	16 Ld SSOP Tape and Reel	M16.209
HIN232ECB	0 to 70	16 Ld SOIC (W)	M16.3
HIN232ECB-T	0 to 70	16 Ld SOIC (W) Tape and Reel	M16.3
HIN232ECBN	0 to 70	16 Ld SOIC (N)	M16.15
HIN232ECP	0 to 70	16 Ld PDIP	E16.3

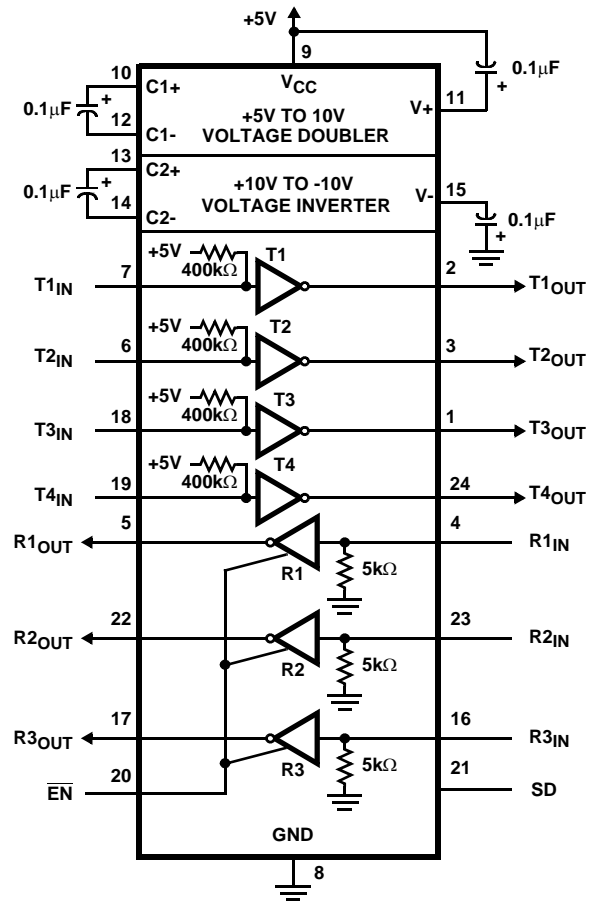
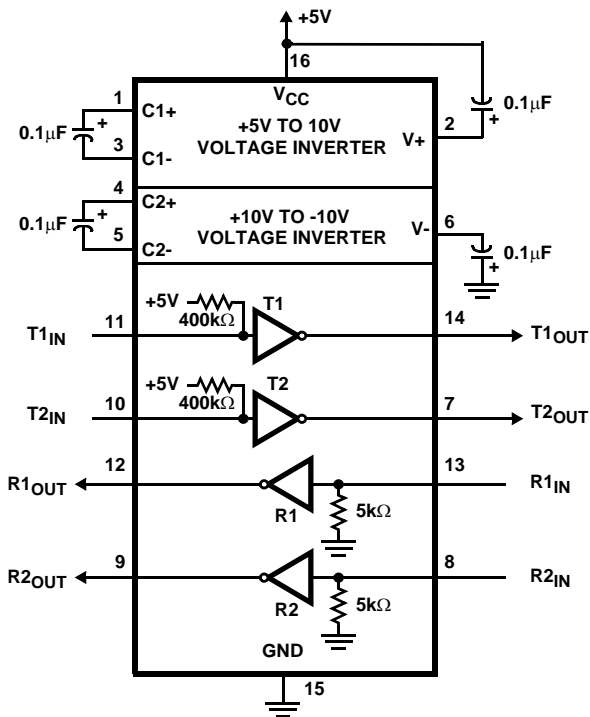
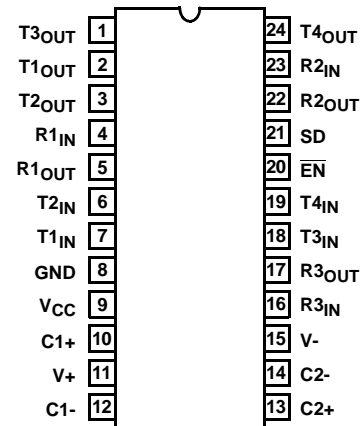
NOTE: Intersil Pb-free products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which is compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J Std-020B.

Pinouts

HIN202E (PDIP, SOIC)  
TOP VIEW

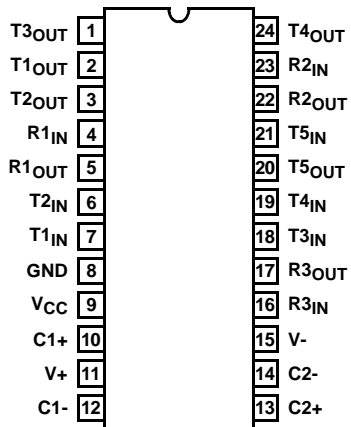


HIN206E (SOIC, SSOP)  
TOP VIEW

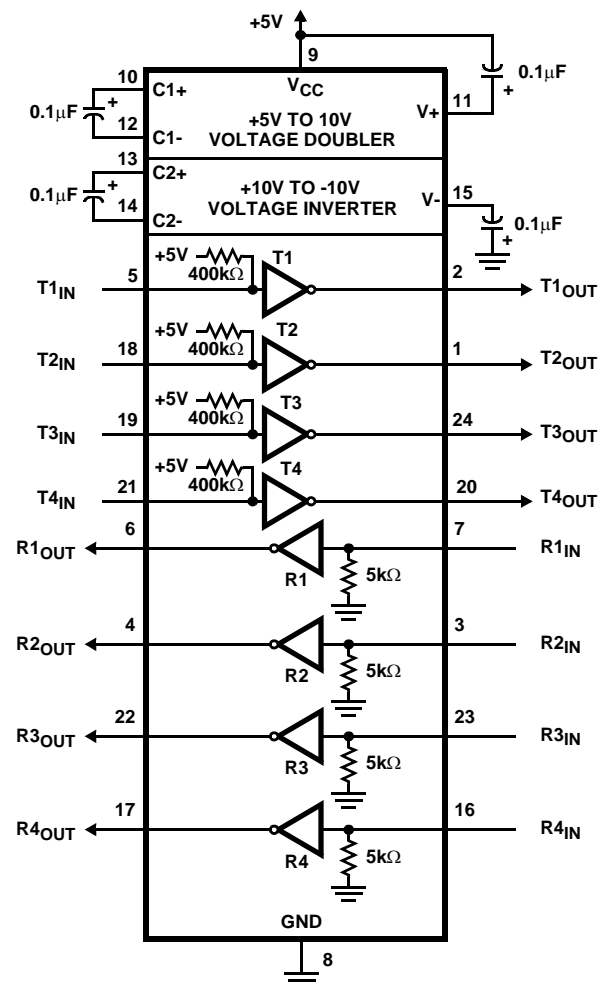
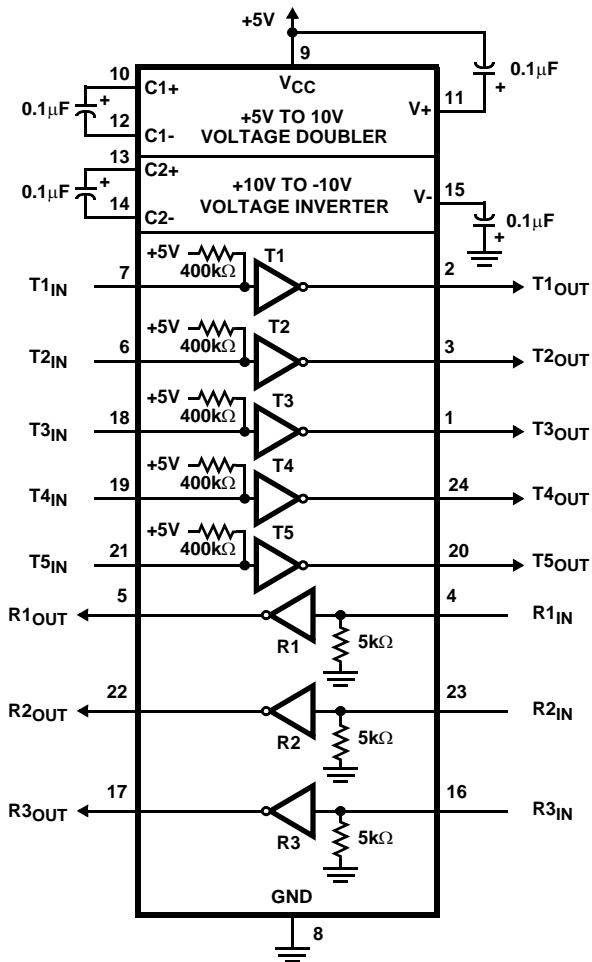
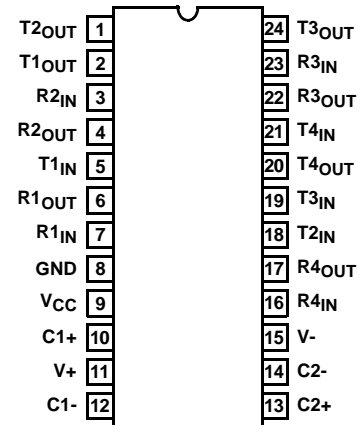


Pinouts (Continued)

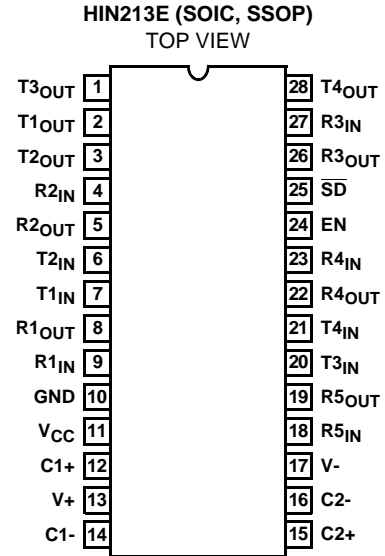
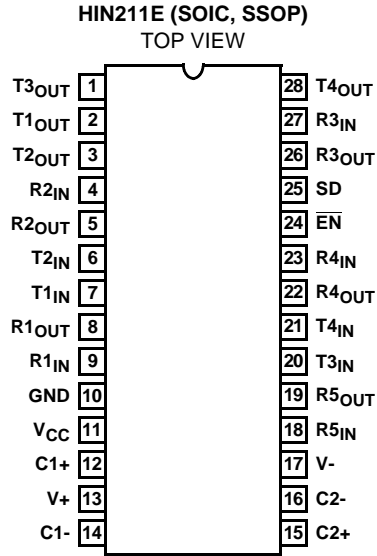
HIN207E (SOIC, SSOP)  
TOP VIEW



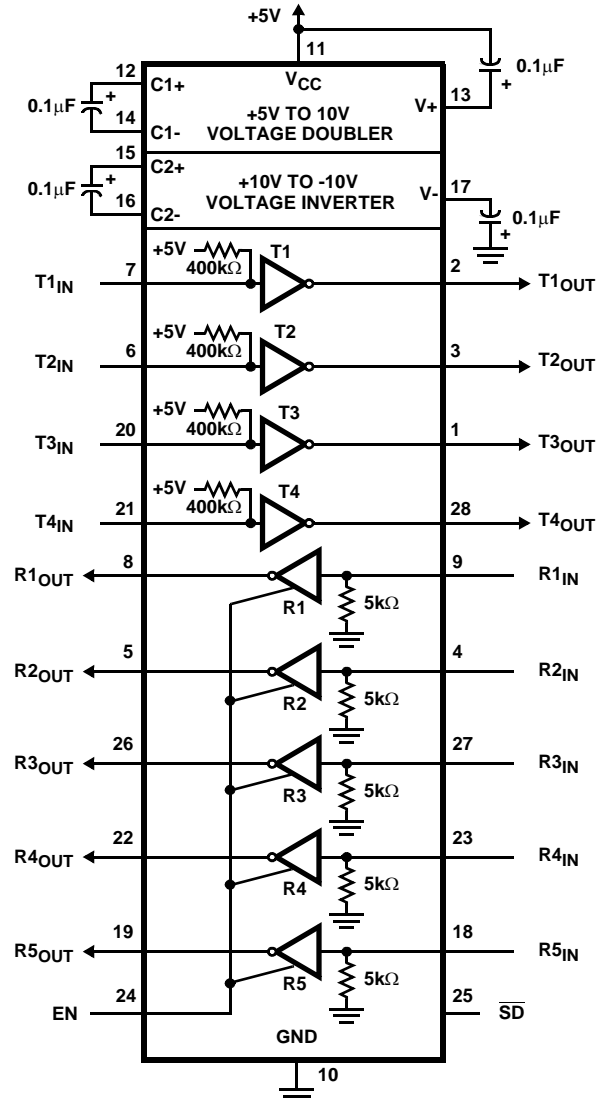
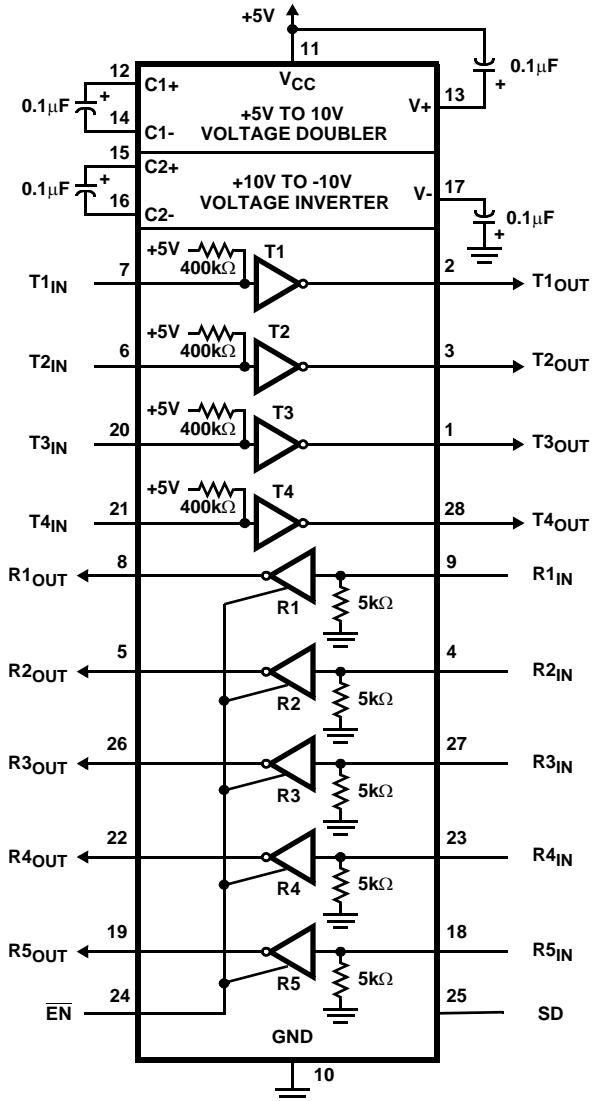
HIN208E (SOIC, SSOP)  
TOP VIEW



Pinouts (Continued)

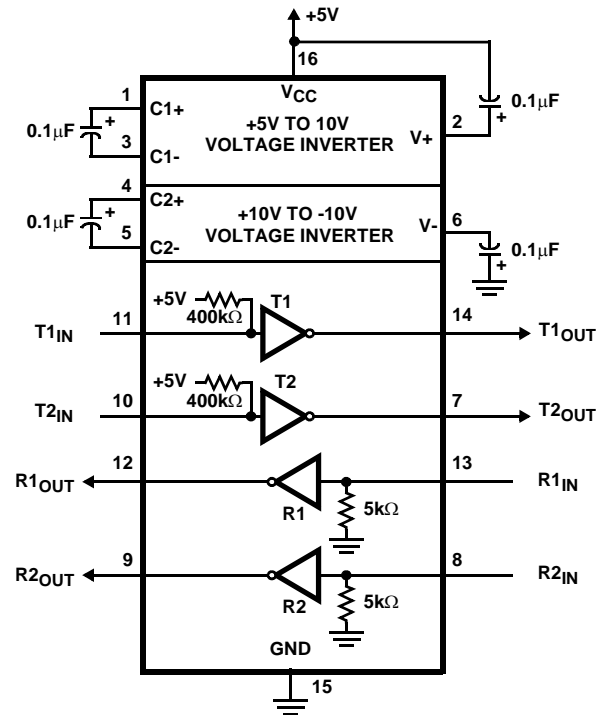
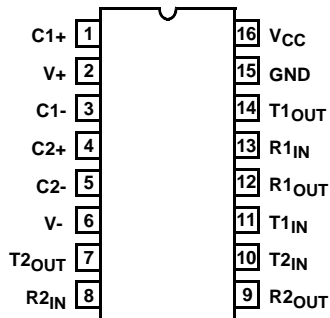


NOTE: R4 and R5 active in shutdown.



**Pinouts** (Continued)

HIN232E (PDIP, SOIC, SSOP)  
TOP VIEW



**Pin Descriptions**

PIN	FUNCTION
V <sub>CC</sub>	Power Supply Input 5V ±10%, (5V ±5% HIN207E).
V+	Internally generated positive supply (+10V nominal).
V-	Internally generated negative supply (-10V nominal).
GND	Ground Lead. Connect to 0V.
C1+	External capacitor (+ terminal) is connected to this lead.
C1-	External capacitor (- terminal) is connected to this lead.
C2+	External capacitor (+ terminal) is connected to this lead.
C2-	External capacitor (- terminal) is connected to this lead.
T <sub>IN</sub>	Transmitter Inputs. These leads accept TTL/CMOS levels. An internal 400kΩ pull-up resistor to V <sub>CC</sub> is connected to each lead.
T <sub>OUT</sub>	Transmitter Outputs. These are RS-232 levels (nominally ±10V).
R <sub>IN</sub>	Receiver Inputs. These inputs accept RS-232 input levels. An internal 5kΩ pull-down resistor to GND is connected to each input.
R <sub>OUT</sub>	Receiver Outputs. These are TTL/CMOS levels.
$\overline{EN}$ , EN	Receiver Enable Input. With $\overline{EN}$ = 5V (HIN213E EN=0V), the receiver outputs are placed in a high impedance state.
SD, $\overline{SD}$	Shutdown Input. With SD = 5V (HIN213E $\overline{SD}$ = 0V), the charge pump is disabled, the receiver outputs are in a high impedance state (except R4 and R5 of HIN213E) and the transmitters are shut off.
NC	No Connect. No connections are made to these leads.

**Absolute Maximum Ratings**

V<sub>CC</sub> to Ground . . . . . (GND -0.3V) < V<sub>CC</sub> < 6V  
 V+ to Ground . . . . . (V<sub>CC</sub> -0.3V) < V+ < 12V  
 V- to Ground . . . . . -12V < V- < (GND +0.3V)  
 Input Voltages  
 T<sub>IN</sub> . . . . . -0.3V < V<sub>IN</sub> < (V+ +0.3V)  
 R<sub>IN</sub> . . . . . ±30V  
 Output Voltages  
 T<sub>OUT</sub> . . . . . (V- -0.3V) < V<sub>TXOUT</sub> < (V+ +0.3V)  
 R<sub>OUT</sub> . . . . . (GND -0.3V) < V<sub>RXOUT</sub> < (V+ +0.3V)  
 Short Circuit Duration  
 T<sub>OUT</sub> . . . . . Continuous  
 R<sub>OUT</sub> . . . . . Continuous  
 ESD Classification . . . . . See Specification Table

**Thermal Information**

Thermal Resistance (Typical, Note 1) θ<sub>JA</sub> (°C/W)  
 16 Ld SOIC (N) Package . . . . . 110  
 16 Ld SOIC (W) Package . . . . . 100  
 16 Ld SSOP Package . . . . . 155  
 16 Ld PDIP Package . . . . . 90  
 24 Ld SOIC Package . . . . . 75  
 24 Ld SSOP Package . . . . . 135  
 28 Ld SOIC Package . . . . . 70  
 28 Ld SSOP Package . . . . . 100  
 Maximum Junction Temperature (Plastic Package) . . . . . 150°C  
 Maximum Storage Temperature Range . . . . . -65°C to 150°C  
 Maximum Lead Temperature (Soldering 10s) . . . . . 300°C  
 (SOIC and SSOP - Lead Tips Only)

**Operating Conditions**

Temperature Range  
 HIN2XXECX . . . . . 0°C to 70°C  
 HIN2XXEIX . . . . . -40°C to 85°C

*CAUTION: Stresses above those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

**NOTE:**

- θ<sub>JA</sub> is measured with the component mounted on an evaluation PC board in free air.

**Electrical Specifications** Test Conditions: V<sub>CC</sub> = +5V ±10%, (V<sub>CC</sub> = +5V ±5% HIN207E); C1-C4 = 0.1µF; T<sub>A</sub> = Operating Temperature Range

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS	
<b>SUPPLY CURRENTS</b>						
Power Supply Current, I <sub>CC</sub>	No Load, T <sub>A</sub> = 25°C	HIN202E	-	8	15	mA
		HIN206E - HIN208E, HIN211E, HIN213E	-	11	20	mA
		HIN232E	-	5	10	mA
Shutdown Supply Current, I <sub>CC</sub> (SD)	T <sub>A</sub> = 25°C	HIN206E, HIN211E	-	1	10	µA
		HIN213E	-	15	50	µA
<b>LOGIC AND TRANSMITTER INPUTS, RECEIVER OUTPUTS</b>						
Input Logic Low, V <sub>IL</sub>	T <sub>IN</sub> , $\overline{EN}$ , SD, EN, $\overline{SD}$	-	-	0.8	V	
Input Logic High, V <sub>IH</sub>	T <sub>IN</sub>	2.0	-	-	V	
	$\overline{EN}$ , SD, EN, $\overline{SD}$	2.4	-	-	V	
Transmitter Input Pullup Current, I <sub>p</sub>	T <sub>IN</sub> = 0V	-	15	200	µA	
TTL/CMOS Receiver Output Voltage Low, V <sub>OL</sub>	I <sub>OUT</sub> = 1.6mA (HIN202E, HIN232E, I <sub>OUT</sub> = 3.2mA)	-	0.1	0.4	V	
TTL/CMOS Receiver Output Voltage High, V <sub>OH</sub>	I <sub>OUT</sub> = -1mA	3.5	4.6	-	V	
TTL/CMOS Receiver Output Leakage	$\overline{EN}$ = V <sub>CC</sub> , EN = 0, 0V < R <sub>OUT</sub> < V <sub>CC</sub>	-	0.5	±10	µA	
<b>RECEIVER INPUTS</b>						
RS-232 Input Voltage Range, V <sub>IN</sub>		-30	-	+30	V	
Receiver Input Impedance, R <sub>IN</sub>	T <sub>A</sub> = 25°C, V <sub>IN</sub> = ±3V	3.0	5.0	7.0	kΩ	
Receiver Input Low Threshold, V <sub>IN</sub> (H-L)	V <sub>CC</sub> = 5V, T <sub>A</sub> = 25°C	Active Mode	-	1.2	-	V
		Shutdown Mode HIN213E R4 and R5	-	1.5	-	V
Receiver Input High Threshold, V <sub>IN</sub> (L-H)	V <sub>CC</sub> = 5V, T <sub>A</sub> = 25°C	Active Mode	-	1.7	2.4	V
		Shutdown Mode HIN213E R4 and R5	-	1.5	2.4	V
Receiver Input Hysteresis, V <sub>HYST</sub>	V <sub>CC</sub> = 5V, No Hysteresis in Shutdown Mode	0.2	0.5	1.0	V	

# HIN202E, HIN206E, HIN207E, HIN208E, HIN211E, HIN213E, HIN232E

**Electrical Specifications** Test Conditions:  $V_{CC} = +5V \pm 10\%$ , ( $V_{CC} = +5V \pm 5\%$  HIN207E);  $C1-C4 = 0.1\mu F$ ;  $T_A =$  Operating Temperature Range (Continued)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
<b>TIMING CHARACTERISTICS</b>					
Output Enable Time, $t_{EN}$	HIN206E, HIN211E, HIN213E	-	600	-	ns
Output Disable Time, $t_{DIS}$	HIN206E, HIN211E, HIN213E	-	200	-	ns
Transmitter, Receiver Propagation Delay, $t_{PD}$	HIN213E $\overline{SD} = 0V$ , R4, R5	-	4.0	40	$\mu s$
	HIN213E $\overline{SD} = V_{CC}$ , R1 - R5	-	0.5	10	$\mu s$
	All except HIN213E	-	0.5	10	$\mu s$
Transition Region Slew Rate, $SR_T$	$R_L = 3k\Omega$ , $C_L = 1000pF$ Measured from +3V to -3V or -3V to +3V, 1 Transmitter Switching (Note 2)	3	20	45	V/ $\mu s$
<b>TRANSMITTER OUTPUTS</b>					
Output Voltage Swing, $T_{OUT}$	Transmitter Outputs, $3k\Omega$ to Ground	$\pm 5$	$\pm 9$	$\pm 10$	V
Output Resistance, $T_{OUT}$	$V_{CC} = V+ = V- = 0V$ , $V_{OUT} = \pm 2V$	300	-	-	$\Omega$
RS-232 Output Short Circuit Current, $I_{SC}$	$T_{OUT}$ Shorted to GND	-	$\pm 10$	-	mA
<b>ESD PERFORMANCE</b>					
RS-232 Pins ( $T_{OUT}$ , $R_{IN}$ )	Human Body Model	-	$\pm 15$	-	kV
	IEC1000-4-2 Contact Discharge	-	$\pm 8$	-	kV
	IEC1000-4-2 Air Gap (Note 3)	-	$\pm 15$	-	kV
All Other Pins	Human Body Model	-	$\pm 2$	-	kV

NOTES:

2. Guaranteed by design.
3. Meets Level 4.

## Test Circuits (HIN232E)

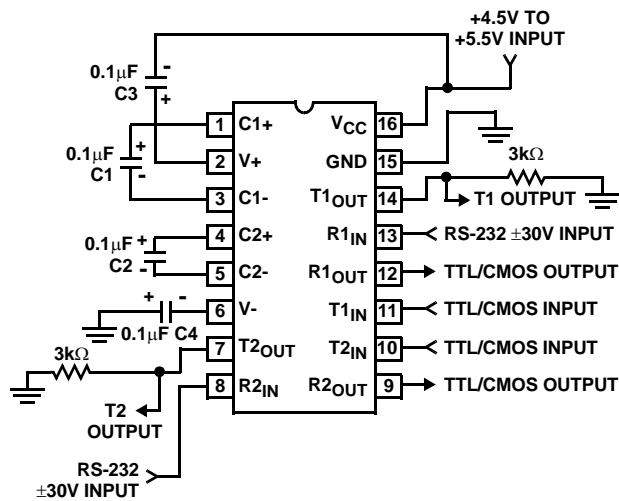


FIGURE 1. GENERAL TEST CIRCUIT

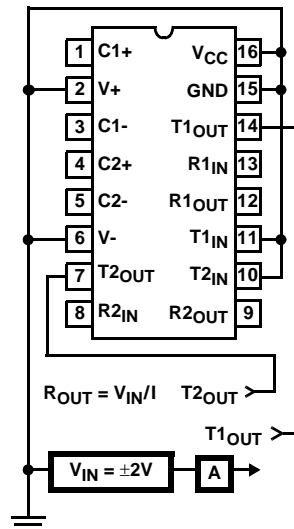


FIGURE 2. POWER-OFF SOURCE RESISTANCE CONFIGURATION



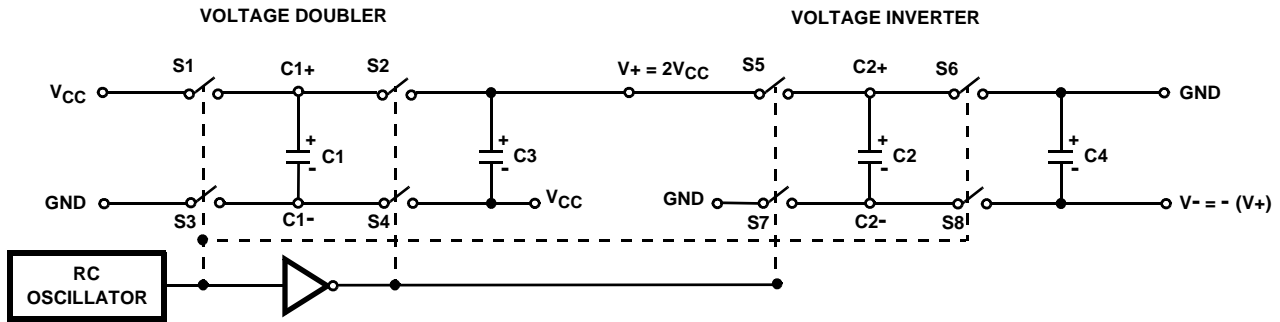


FIGURE 3. CHARGE PUMP

### Detailed Description

The HIN2XXE family of high-speed RS-232 transmitters/receivers are powered by a single +5V power supply, feature low power consumption, and meet all EIA RS232C and V.28 specifications. The circuit is divided into three sections: the charge pump, transmitter, and receiver.

#### Charge Pump

An equivalent circuit of the charge pump is illustrated in Figure 3. The charge pump contains two sections: the voltage doubler and the voltage inverter. Each section is driven by a two phase, internally generated clock to generate +10V and -10V. The nominal clock frequency is 125kHz. During phase one of the clock, capacitor C1 is charged to  $V_{CC}$ . During phase two, the voltage on C1 is added to  $V_{CC}$ , producing a signal across C3 equal to twice  $V_{CC}$ . During phase two, C2 is also charged to  $2V_{CC}$ , and then during phase one, it is inverted with respect to ground to produce a signal across C4 equal to  $-2V_{CC}$ . The charge pump accepts input voltages up to 5.5V. The output impedance of the voltage doubler section ( $V+$ ) is approximately  $200\Omega$ , and the output impedance of the voltage inverter section ( $V-$ ) is approximately  $450\Omega$ . A typical application uses  $0.1\mu\text{F}$  capacitors for C1-C4, however, the value is not critical. Increasing the values of C1 and C2 will lower the output impedance of the voltage doubler and inverter, increasing the values of the reservoir capacitors, C3 and C4, lowers the ripple on the  $V+$  and  $V-$  supplies.

During shutdown mode (HIN206E, HIN211E and HIN213E) the charge pump is turned off,  $V+$  is pulled down to  $V_{CC}$ ,  $V-$  is pulled up to GND, and the supply current is reduced to less than  $10\mu\text{A}$ . The transmitter outputs are disabled and the receiver outputs (except for HIN213E, R4 and R5) are placed in the high impedance state.

#### Transmitters

The transmitters are TTL/CMOS compatible inverters which translate the inputs to RS-232 outputs. The input logic threshold is about 26% of  $V_{CC}$ , or 1.3V for  $V_{CC} = 5\text{V}$ . A logic 1 at the input results in a voltage of between -5V and  $V-$  at the output, and a logic 0 results in a voltage between +5V

and ( $V+ - 0.6\text{V}$ ). Each transmitter input has an internal  $400\text{k}\Omega$  pullup resistor so any unused input can be left unconnected and its output remains in its low state. The output voltage swing meets the RS-232C specifications of  $\pm 5\text{V}$  minimum with the worst case conditions of: all transmitters driving  $3\text{k}\Omega$  minimum load impedance,  $V_{CC} = 4.5\text{V}$ , and maximum allowable operating temperature. The transmitters have an internally limited output slew rate which is less than  $30\text{V}/\mu\text{s}$ . The outputs are short circuit protected and can be shorted to ground indefinitely. The powered down output impedance is a minimum of  $300\Omega$  with  $\pm 2\text{V}$  applied to the outputs and  $V_{CC} = 0\text{V}$ .

#### Receivers

The receiver inputs accept up to  $\pm 30\text{V}$  while presenting the required  $3\text{k}\Omega$  to  $7\text{k}\Omega$  input impedance even if the power is off ( $V_{CC} = 0\text{V}$ ). The receivers have a typical input threshold of 1.3V which is within the  $\pm 3\text{V}$  limits, known as the transition region, of the RS-232 specifications. The receiver output is 0V to  $V_{CC}$ . The output will be low whenever the input is greater than 2.4V and high whenever the input is floating or driven between +0.8V and -30V. The receivers feature 0.5V hysteresis (except during shutdown) to improve noise rejection. The receiver Enable line  $\overline{\text{EN}}$ , (EN on HIN213E) when unasserted, disables the receiver outputs, placing them in the high impedance mode. The receiver outputs are also placed in the high impedance state when in shutdown mode (except HIN213E R4 and R5).

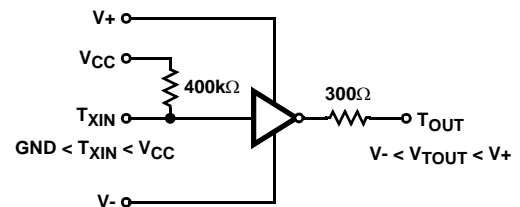


FIGURE 4. TRANSMITTER

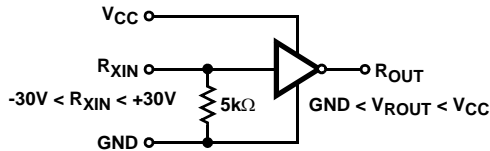


FIGURE 5. RECEIVER

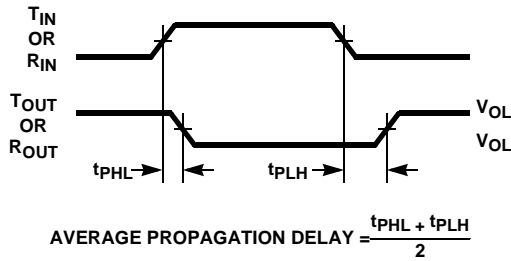


FIGURE 6. PROPAGATION DELAY DEFINITION

### HIN213E Operation in Shutdown

The HIN213E features two receivers, R4 and R5, which remain active in shutdown mode. During normal operation the receivers propagation delay is typically 0.5μs. This propagation delay may increase slightly during shutdown. When entering shut down mode, receivers R4 and R5 are not valid for 80μs after  $\overline{SD} = V_{IL}$ . When exiting shutdown mode, all receiver outputs will be invalid until the charge pump circuitry reaches normal operating voltage. This is typically less than 2ms when using 0.1μF capacitors.

### Application Information

The HIN2XXE may be used for all RS-232 data terminal and communication links. It is particularly useful in applications where ±12V power supplies are not available for conventional RS-232 interface circuits. The applications presented represent typical interface configurations.

A simple duplex RS-232 port with CTS/RTS handshaking is illustrated in Figure 7. Fixed output signals such as DTR (data terminal ready) and DSRs (data signaling rate select) is generated by driving them through a 5kΩ resistor connected to V+.

In applications requiring four RS-232 inputs and outputs (Figure 8), note that each circuit requires two charge pump capacitors (C1 and C2) but can share common reservoir capacitors (C3 and C4). The benefit of sharing common reservoir capacitors is the elimination of two capacitors and the reduction of the charge pump source impedance which effectively increases the output swing of the transmitters.

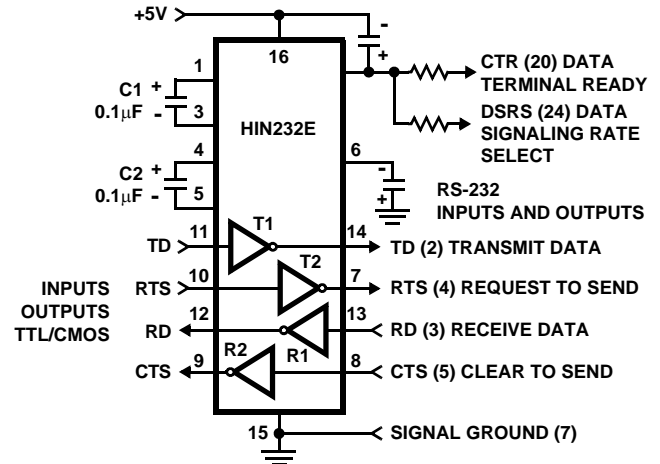


FIGURE 7. SIMPLE DUPLEX RS-232 PORT WITH CTS/RTS HANDSHAKING

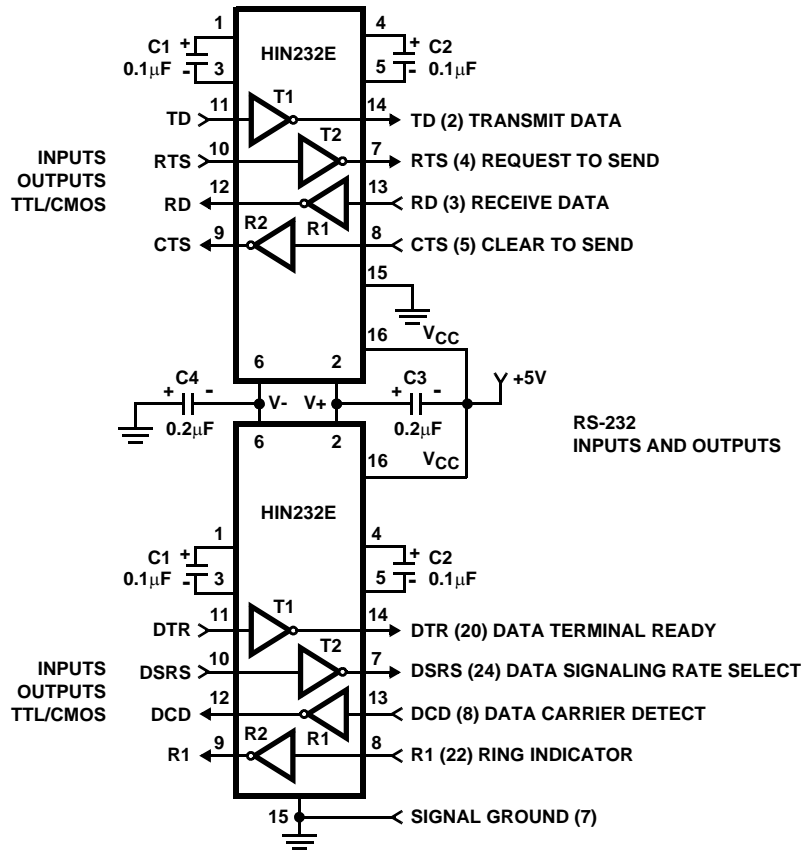


FIGURE 8. COMBINING TWO HIN232Es FOR 4 PAIRS OF RS-232 INPUTS AND OUTPUTS

### Typical Performance Curves

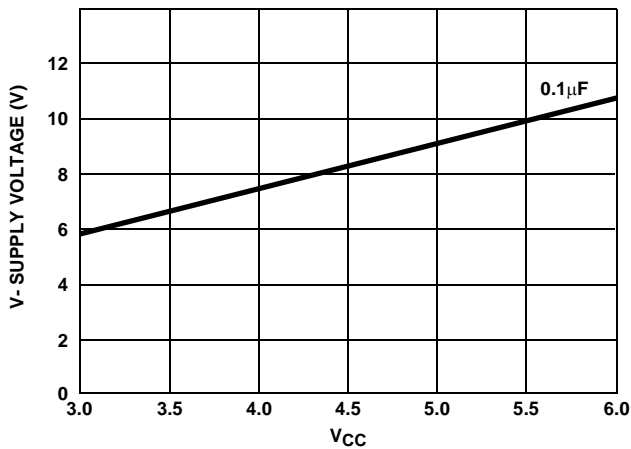


FIGURE 9. V- SUPPLY VOLTAGE vs V<sub>CC</sub>

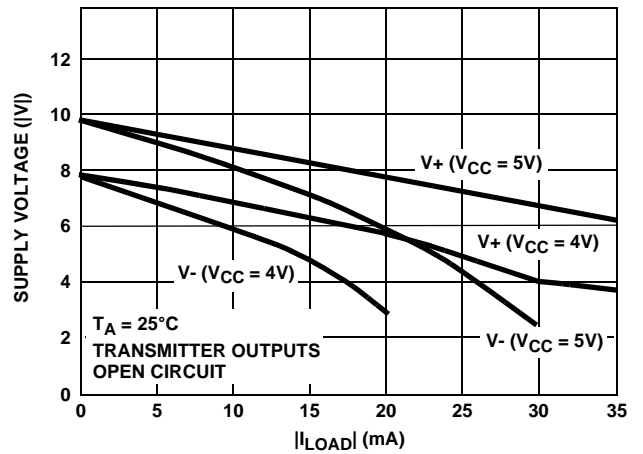


FIGURE 10. V+, V- OUTPUT VOLTAGE vs LOAD

## Die Characteristics

### DIE DIMENSIONS:

128 mils x 77 mils

### METALLIZATION:

Type: Al

Thickness:  $10\text{k}\text{\AA} \pm 1\text{k}\text{\AA}$

### SUBSTRATE POTENTIAL

GND

### PASSIVATION:

Type: Nitride over Silox

Nitride Thickness:  $8\text{k}\text{\AA}$

Silox Thickness:  $7\text{k}\text{\AA}$

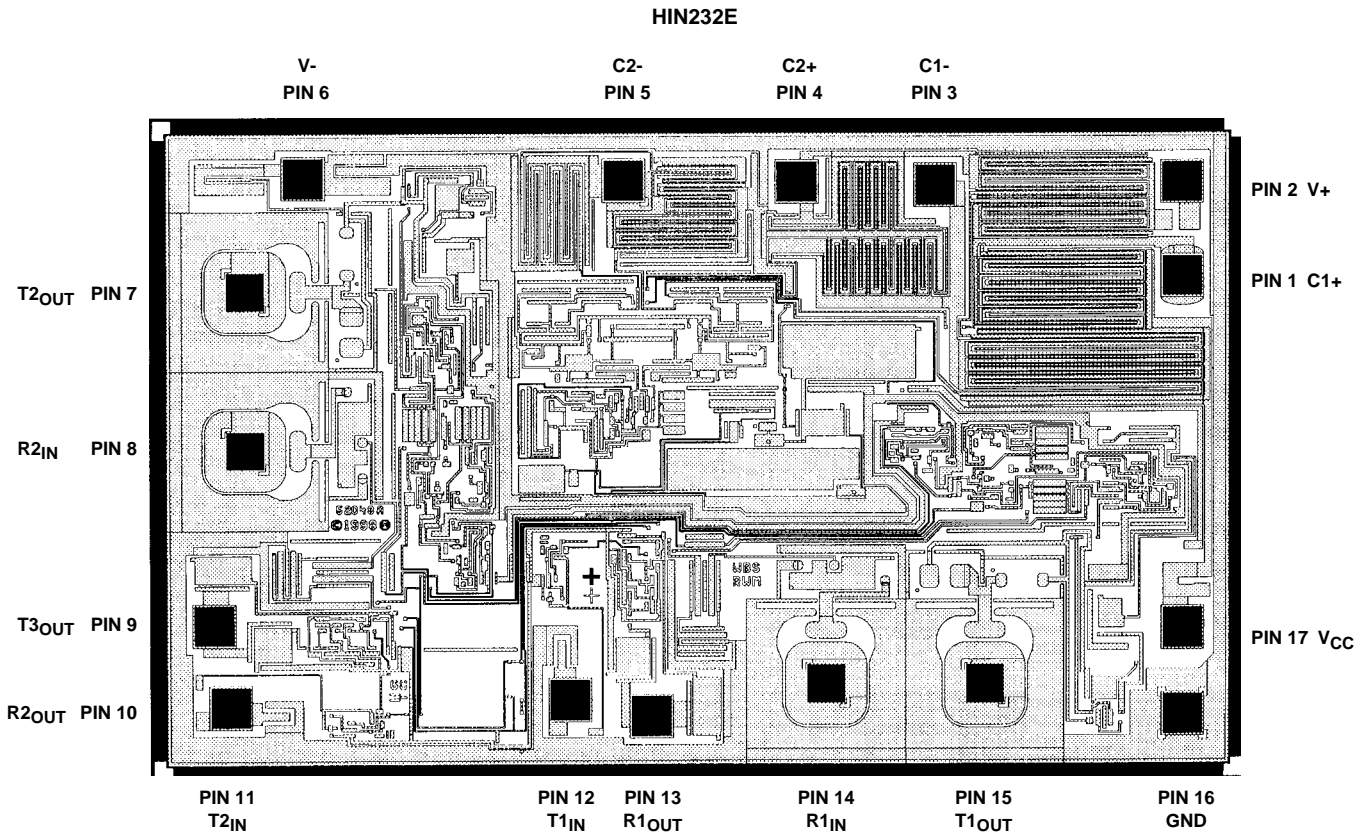
### TRANSISTOR COUNT:

185

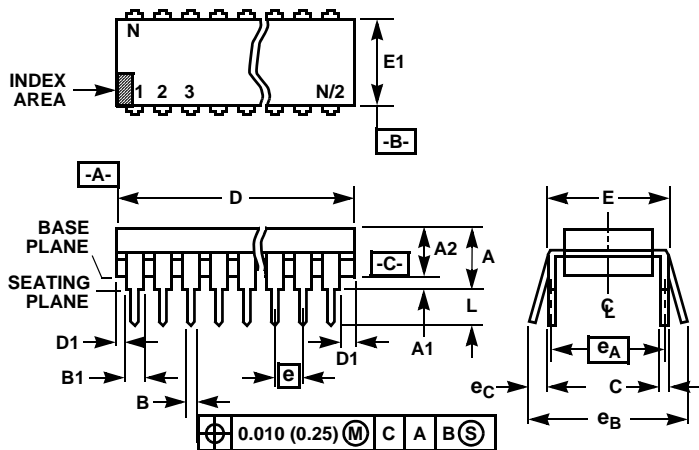
### PROCESS:

CMOS Metal Gate

## Metallization Mask Layout



Dual-In-Line Plastic Packages (PDIP)



NOTES:

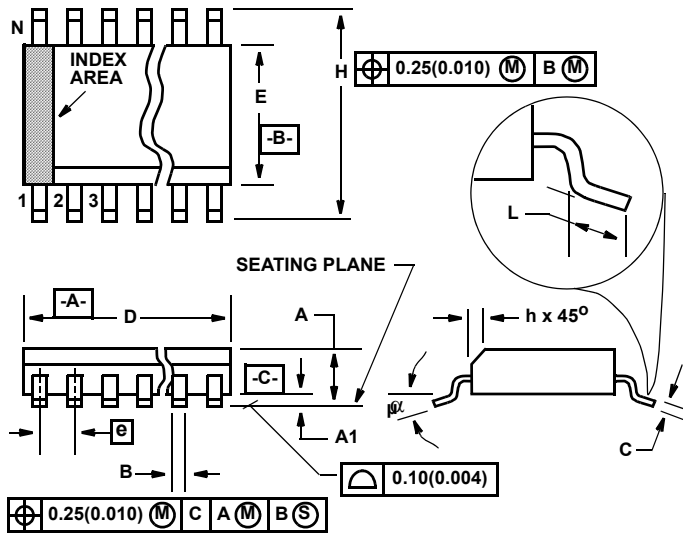
- Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
- Dimensioning and tolerancing per ANSI Y14.5M-1982.
- Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
- Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
- D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
- E and  $e_A$  are measured with the leads constrained to be perpendicular to datum  $-C-$ .
- $e_B$  and  $e_C$  are measured at the lead tips with the leads unconstrained.  $e_C$  must be zero or greater.
- B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
- N is the maximum number of terminal positions.
- Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E16.3 (JEDEC MS-001-BB ISSUE D)  
16 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8, 10
C	0.008	0.014	0.204	0.355	-
D	0.735	0.775	18.66	19.68	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
$e_A$	0.300 BSC		7.62 BSC		6
$e_B$	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	16		16		9

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**Small Outline Plastic Packages (SOIC)**



**M16.15 (JEDEC MS-012-AC ISSUE C)**  
**16 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE**

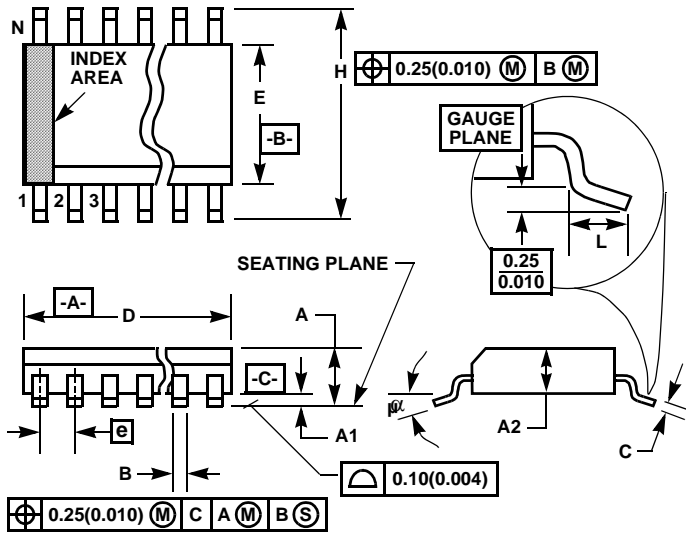
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.053	0.069	1.35	1.75	-
A1	0.004	0.010	0.10	0.25	-
B	0.014	0.019	0.35	0.49	9
C	0.007	0.010	0.19	0.25	-
D	0.386	0.394	9.80	10.00	3
E	0.150	0.157	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.228	0.244	5.80	6.20	-
h	0.010	0.020	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	16		16		7
$\alpha$	0°	8°	0°	8°	-

Rev. 1 02/02

**NOTES:**

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

Small Outline Plastic Packages (SSOP)



**M16.209 (JEDEC MO-150-AC ISSUE B)**  
**16 LEAD SHRINK SMALL OUTLINE PLASTIC PACKAGE**

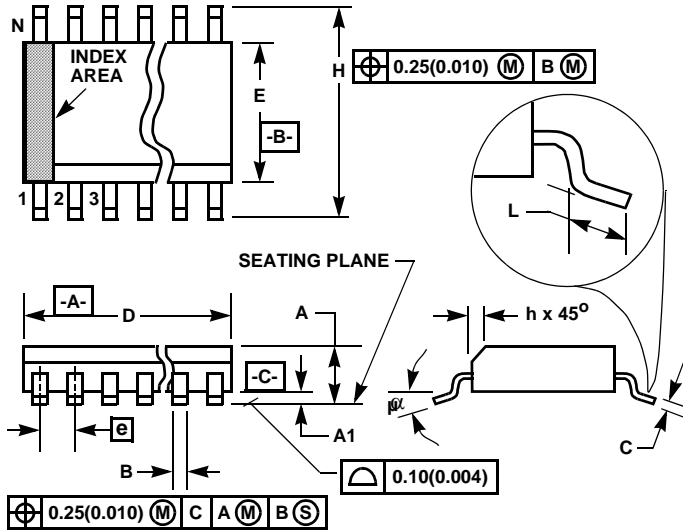
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.078	-	2.00	-
A1	0.002	-	0.05	-	-
A2	0.065	0.072	1.65	1.85	-
B	0.009	0.014	0.22	0.38	9
C	0.004	0.009	0.09	0.25	-
D	0.233	0.255	5.90	6.50	3
E	0.197	0.220	5.00	5.60	4
e	0.026 BSC		0.65 BSC		-
H	0.292	0.322	7.40	8.20	-
L	0.022	0.037	0.55	0.95	6
N	16		16		7
$\alpha$	0°	8°	0°	8°	-

NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.20mm (0.0078 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.20mm (0.0078 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension "B" does not include dambar protrusion. Allowable dambar protrusion shall be 0.13mm (0.005 inch) total in excess of "B" dimension at maximum material condition.
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

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Small Outline Plastic Packages (SOIC)



M16.3 (JEDEC MS-013-AA ISSUE C)  
16 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.0200	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.3977	0.4133	10.10	10.50	3
E	0.2914	0.2992	7.40	7.60	4
e	0.050 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.010	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	16		16		7
alpha	0°	8°	0°	8°	-

NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

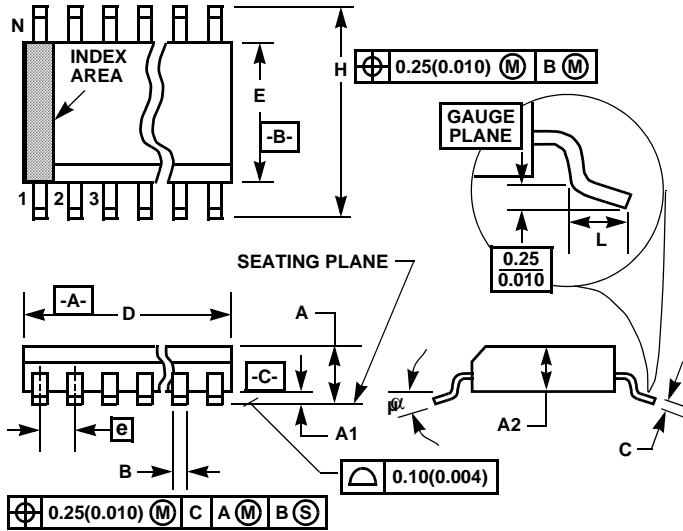
Rev. 0 12/93







Shrink Small Outline Plastic Packages (SSOP)



M28.209 (JEDEC MO-150-AH ISSUE B)  
28 LEAD SHRINK SMALL OUTLINE PLASTIC PACKAGE

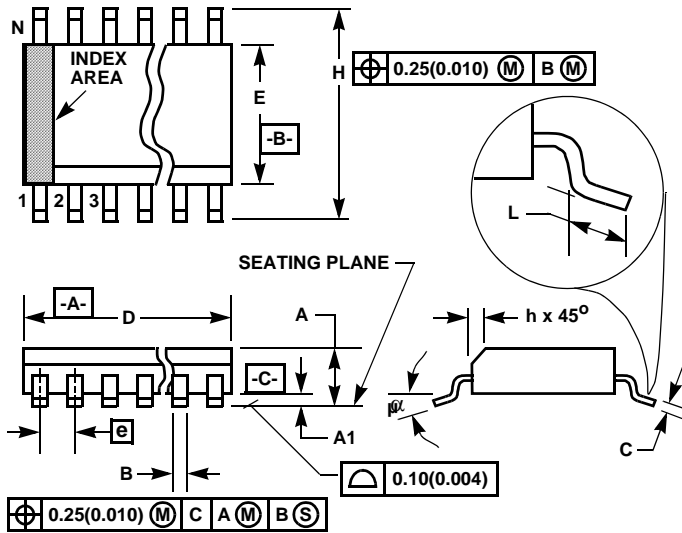
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.078	-	2.00	-
A1	0.002	-	0.05	-	-
A2	0.065	0.072	1.65	1.85	-
B	0.009	0.014	0.22	0.38	9
C	0.004	0.009	0.09	0.25	-
D	0.390	0.413	9.90	10.50	3
E	0.197	0.220	5.00	5.60	4
e	0.026 BSC		0.65 BSC		-
H	0.292	0.322	7.40	8.20	-
L	0.022	0.037	0.55	0.95	6
N	28		28		7
$\alpha$	0°	8°	0°	8°	-

NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.20mm (0.0078 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.20mm (0.0078 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension "B" does not include dambar protrusion. Allowable dambar protrusion shall be 0.13mm (0.005 inch) total in excess of "B" dimension at maximum material condition.
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

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**Small Outline Plastic Packages (SOIC)**



**M28.3 (JEDEC MS-013-AE ISSUE C)**  
**28 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE**

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.0200	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.6969	0.7125	17.70	18.10	3
E	0.2914	0.2992	7.40	7.60	4
e	0.05 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.01	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	28		28		7
$\alpha$	0°	8°	0°	8°	-

**NOTES:**

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

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