Data Sheet June 2000 File Number 4380.6

5A, 30V, 0.050 Ohm, Dual N-Channel, Logic Level UltraFET Power MOSFET

This N-Channel power MOSFET is manufactured using the innovative UltraFET™ process. This advanced process technology achieves the lowest possible on-resistance per silicon area, resulting in outstanding performance. This device is capable of withstanding high energy in the avalanche mode and the diode exhibits very low reverse recovery time and stored charge. It was designed for use in applications where power efficiency is important, such as switching regulators, switching converters, motor drivers, relay drivers, low-voltage bus switches, and power management in portable and battery operated products.

Formerly developmental type TA76105.

Ordering Information

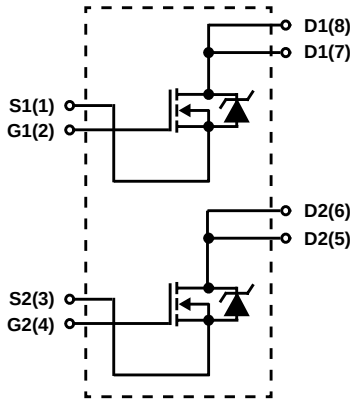
PART NUMBER	PACKAGE	BRAND
HUF76105DK8	MS-012AA	76105DK8

NOTE: When ordering, use the entire part number. Add the suffix T to obtain the variant in tape and reel, e.g., HUF76105DK8T.

Features

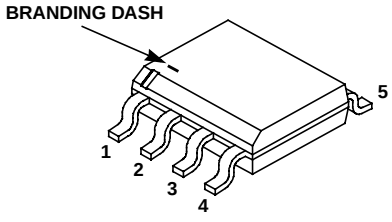
- Logic Level Gate Drive
- 5A, 30V
- Ultra Low On-Resistance, $r_{DS(ON)} = 0.050\Omega$
- Temperature Compensating PSPICE® Model
- Temperature Compensating SABER© Model
- Thermal Impedance SPICE Model
- Thermal Impedance SABER Model
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- Related Literature
  - TB334, “Guidelines for Soldering Surface Mount Components to PC Boards”

Symbol



Packaging

JEDEC MS-012AA



CAUTION: These devices are sensitive to electrostatic discharge; follow proper ESD Handling Procedures.
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PSPICE® is a registered trademark of MicroSim Corporation. SABER™ is a trademark of Analogy, Inc.
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Absolute Maximum Ratings $T_A = 25^oC$, Unless Otherwise Specified

		HUF76105DK8	UNITS
Drain to Source Voltage (Note 1)	V_{DSS}	30	V
Drain to Gate Voltage (R_{GS} = 20kΩ) (Note 1)	V_{DGR}	30	V
Gate to Source Voltage	V_{GS}	±16	V
Drain Current			
Continuous (T_A= 25°C, V_{GS} = 10V) (Figure 2) (Note 2)	I_D	5	A
Continuous (T_A= 100°C, V_{GS} = 5V) (Note 3)	I_D	1.4	A
Continuous (T_A= 100°C, V_{GS} = 4.5V) (Note 3)	I_D	1.3	A
Pulsed Drain Current	I_{DM}	Figure 4	
Pulsed Avalanche Rating	E_{AS}	Figures 6, 17, 18	
Power Dissipation (Note 2)	P_D	2.5	W
Derate Above 25°C		0.02	W/°C
Operating and Storage Temperature	T_J, T_{STG}	-55 to 150	°C
Maximum Temperature for Soldering			
Leads at 0.063in (1.6mm) from Case for 10s	T_L	300	°C
Package Body for 10s, See Techbrief 334	T_{pkg}	260	°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. T_J = 25°C to 125°C.
2. 50°C/W measured using FR-4 board at 1 second.
3. 228°C/W measured using FR-4 board with 0.006 in^2 of copper at 1000 seconds.

Electrical Specifications $T_A = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
OFF STATE SPECIFICATIONS						
Drain to Source Breakdown Voltage	BV_{DSS}	I_D = 250µA, V_{GS} = 0V (Figure 12)	30	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 25V, V_{GS} = 0V	-	-	1	µA
		V_{DS} = 25V, V_{GS} = 0V, T_C = 150°C	-	-	250	µA
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±16V	-	-	±100	nA
ON STATE SPECIFICATIONS						
Gate to Source Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250µA (Figure 11)	1	-	3	V
Drain to Source On Resistance	$r_{DS(ON)}$	I_D = 5A, V_{GS} = 10V (Figures 9, 10)	-	0.040	0.050	Ω
		I_D = 1.4A, V_{GS} = 5V (Figure 9)	-	0.055	0.072	Ω
		I_D = 1.3A, V_{GS} = 4.5V (Figure 9)	-	0.060	0.078	Ω
THERMAL SPECIFICATIONS						
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	Pad Area = 0.76 in^2 (Note 2)	-	-	50	°C/W
		Pad Area = 0.027 in^2 (See TB377)	-	-	191	°C/W
		Pad Area = 0.006 in^2 (See TB377)	-	-	228	°C/W
SWITCHING SPECIFICATIONS (V_{GS} = 4.5V)						
Turn-On Time	t_{ON}	V_{DD} = 15V, $I_D \cong$ 1.3A, R_L = 11.5Ω, V_{GS} = 4.5V, R_{GS} = 27Ω (Figure 15)	-	-	60	ns
Turn-On Delay Time	$t_{d(ON)}$		-	12	-	ns
Rise Time	t_r		-	28	-	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	31	-	ns
Fall Time	t_f		-	21	-	ns
Turn-Off Time	t_{OFF}		-	-	80	ns

Electrical Specifications $T_A = 25^oC$, Unless Otherwise Specified **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
SWITCHING SPECIFICATIONS (V_{GS} = 10V)							
Turn-On Time	t_{ON}	V_{DD} = 15V, $I_D \cong$ 5A, R_L = 3Ω, V_{GS} = 10V, R_{GS} = 27Ω (Figure 16)		-	-	60	ns
Turn-On Delay Time	$t_{d(ON)}$			-	17	-	ns
Rise Time	t_r			-	21	-	ns
Turn-Off Delay Time	$t_{d(OFF)}$			-	60	-	ns
Fall Time	t_f			-	20	-	ns
Turn-Off Time	t_{OFF}			-	-	120	ns
GATE CHARGE SPECIFICATIONS							
Total Gate Charge	$Q_{g(TOT)}$	V_{GS} = 0V to 10V	V_{DD} = 15V, $I_D \cong$ 1.4A, R_L = 10.7Ω $I_{g(REF)}$ = 1.0mA (Figure 14)	-	9	11	nC
Gate Charge at 5V	$Q_{g(5)}$	V_{GS} = 0V to 5V		-	5.3	6.4	nC
Threshold Gate Charge	$Q_{g(TH)}$	V_{GS} = 0V to 1V		-	0.35	0.45	nC
Gate to Source Gate Charge	Q_{gs}			-	1.00	-	nC
Gate to Drain “Miller” Charge	Q_{gd}			-	2.40	-	nC
CAPACITANCE SPECIFICATIONS							
Input Capacitance	C_{ISS}	V_{DS} = 25V, V_{GS} = 0V, f = 1MHz (Figure 13)		-	325	-	pF
Output Capacitance	C_{OSS}			-	180	-	pF
Reverse Transfer Capacitance	C_{RSS}			-	35	-	pF

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage	V_{SD}	I_{SD} = 5A	-	-	1.25	V
		I_{SD} = 1.4A			1.00	V
Reverse Recovery Time	t_{rr}	I_{SD} = 1.4A, dI_{SD}/dt = 100A/µs	-	-	39	ns
Reverse Recovered Charge	Q_{RR}	I_{SD} = 1.4A, dI_{SD}/dt = 100A/µs	-	-	42	nC

Typical Performance Curves

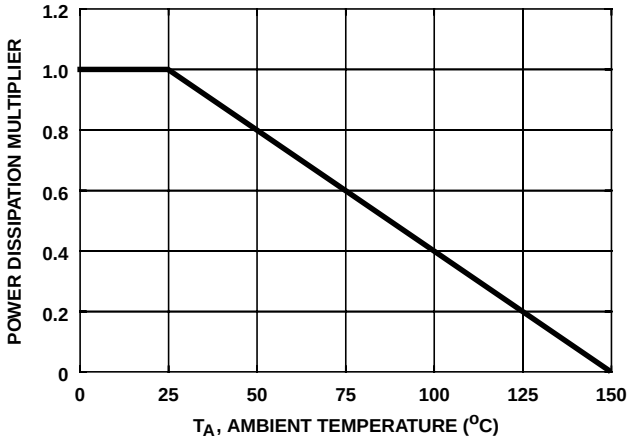


FIGURE 1. NORMALIZED POWER DISSIPATION vs AMBIENT TEMPERATURE

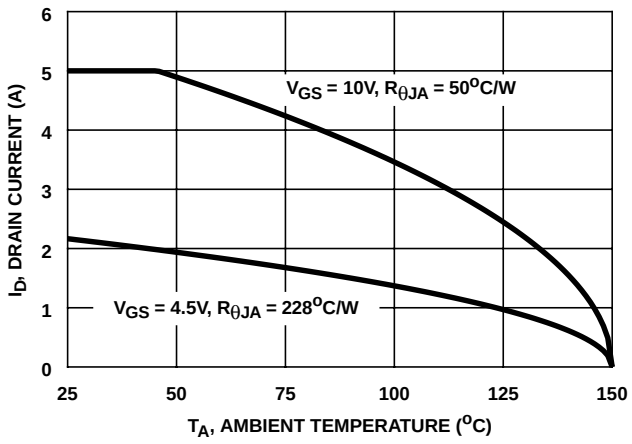


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs AMBIENT TEMPERATURE

Typical Performance Curves (Continued)

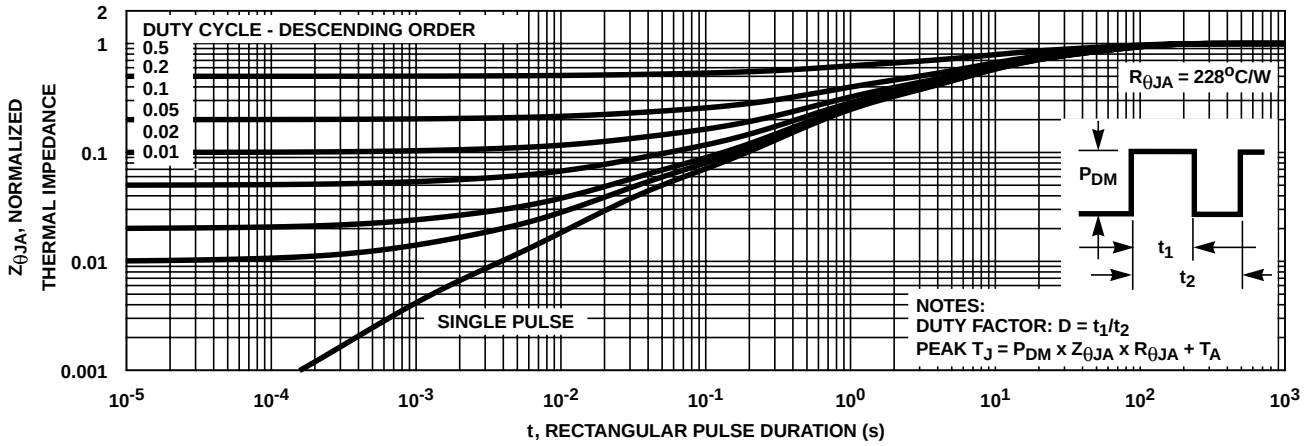


FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

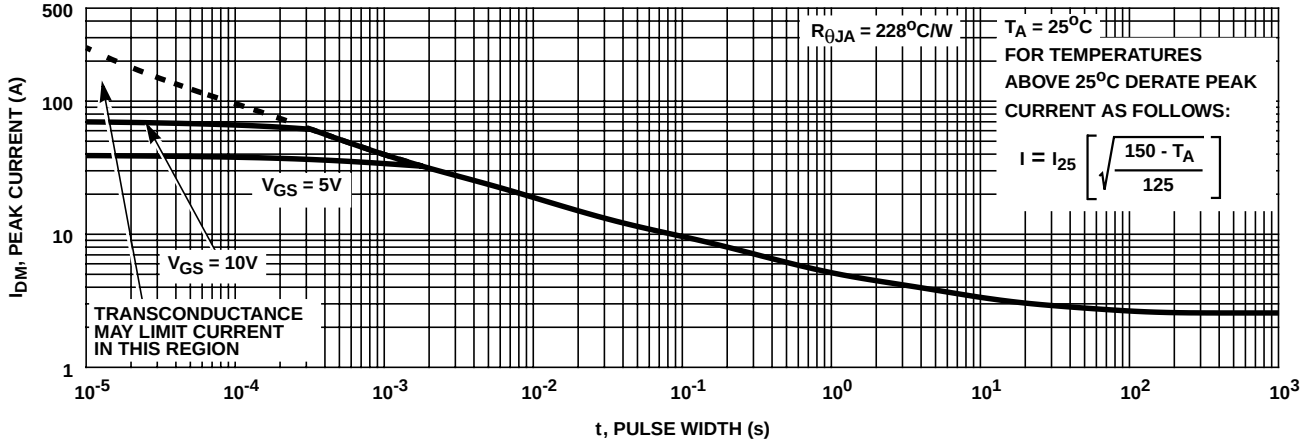


FIGURE 4. PEAK CURRENT CAPABILITY

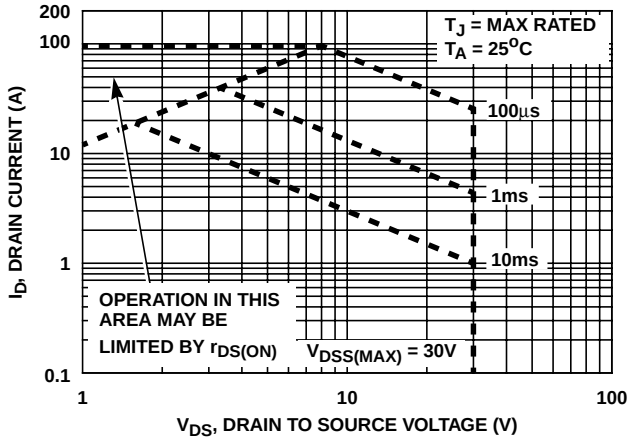
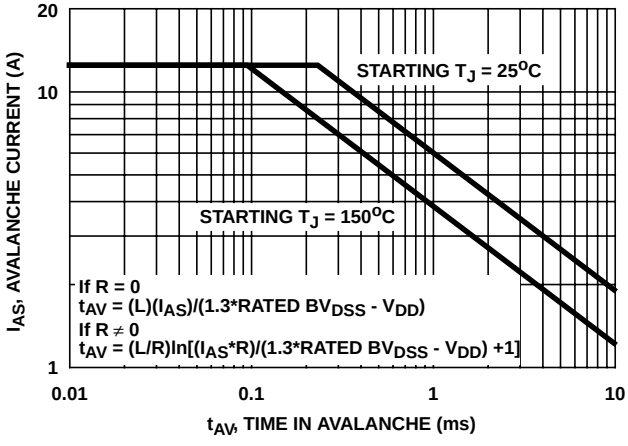


FIGURE 5. FORWARD BIAS SAFE OPERATING AREA



NOTE: Refer to Intersil Application Notes AN9321 and AN9322.

FIGURE 6. UNCLAMPED INDUCTIVE SWITCHING CAPABILITY

Typical Performance Curves (Continued)

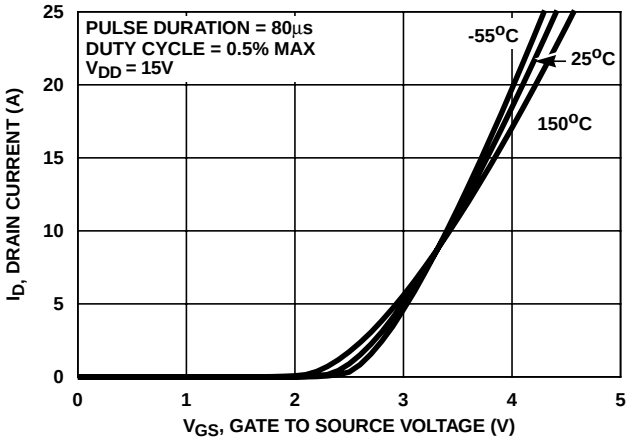


FIGURE 7. TRANSFER CHARACTERISTICS

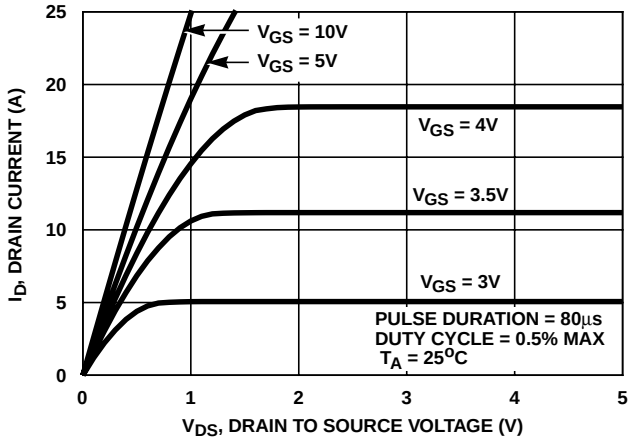


FIGURE 8. SATURATION CHARACTERISTICS

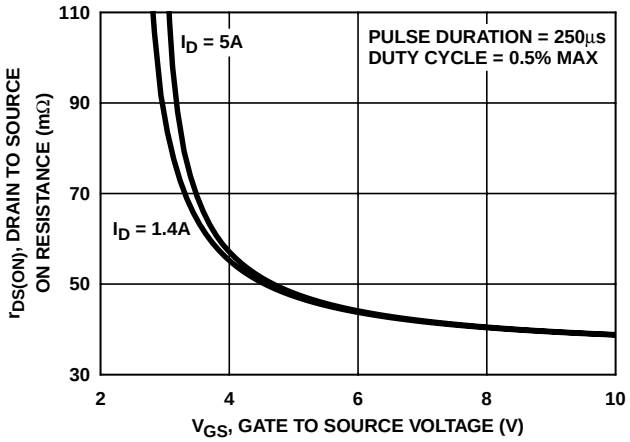


FIGURE 9. DRAIN TO SOURCE ON RESISTANCE vs GATE VOLTAGE AND DRAIN CURRENT

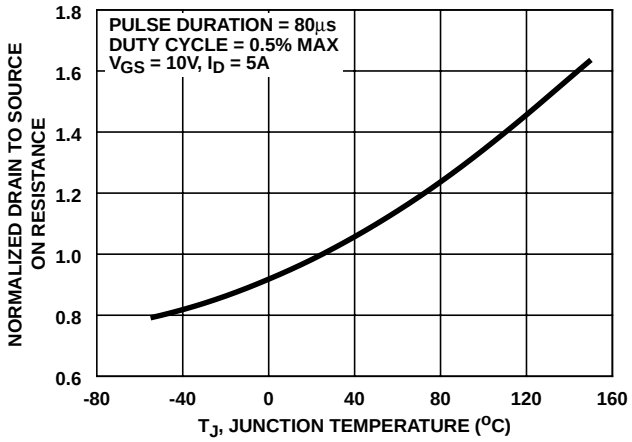


FIGURE 10. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

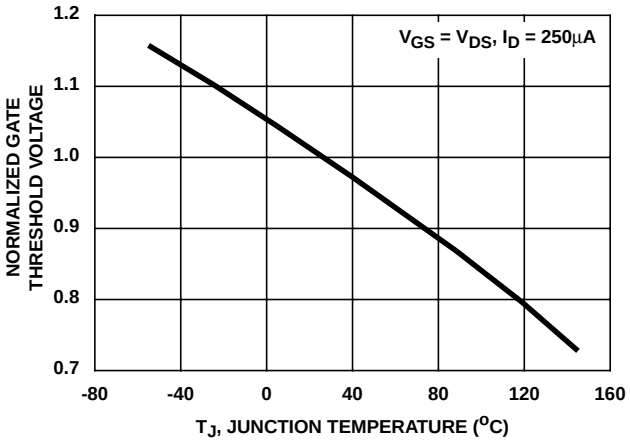


FIGURE 11. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

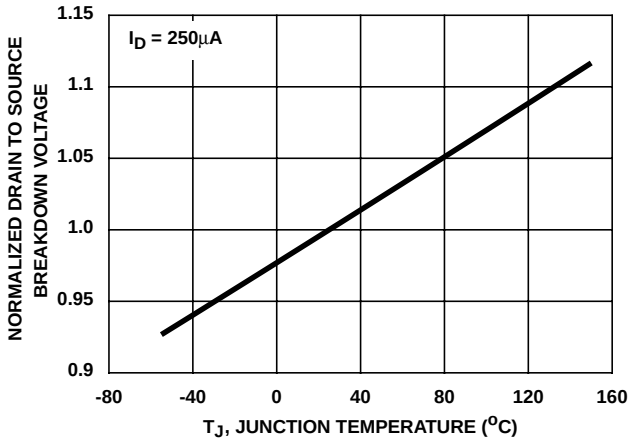


FIGURE 12. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

Typical Performance Curves (Continued)

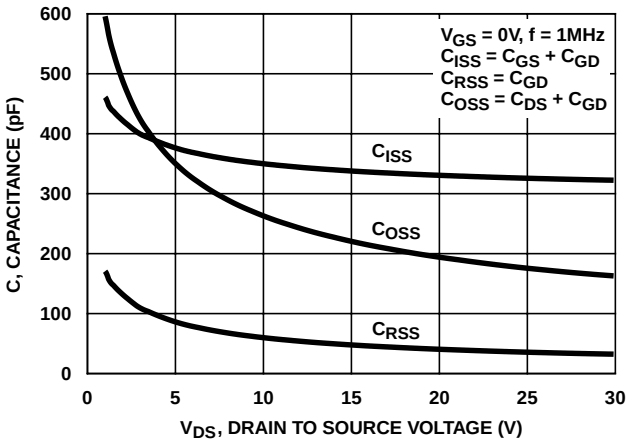
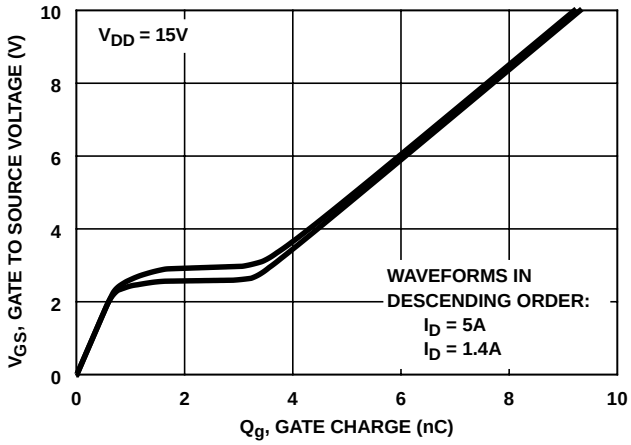


FIGURE 13. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Intersil Application Notes AN7254 and AN7260.

FIGURE 14. GATE CHARGE WAVEFORMS FOR CONSTANT GATE CURRENT

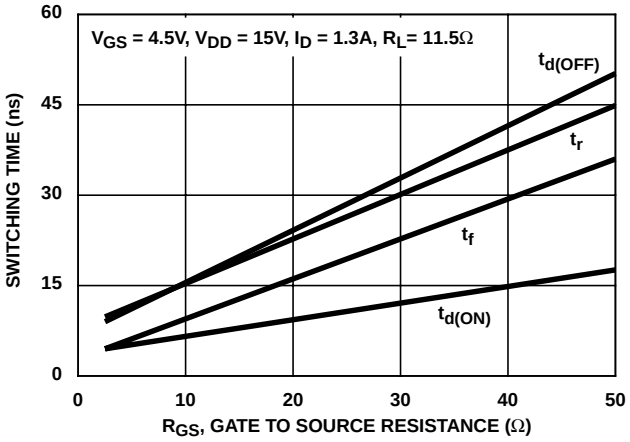


FIGURE 15. SWITCHING TIME vs GATE RESISTANCE

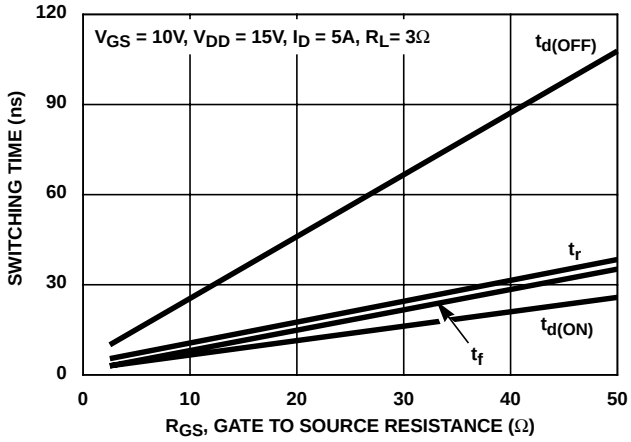


FIGURE 16. SWITCHING TIME vs GATE RESISTANCE

Test Circuits and Waveforms

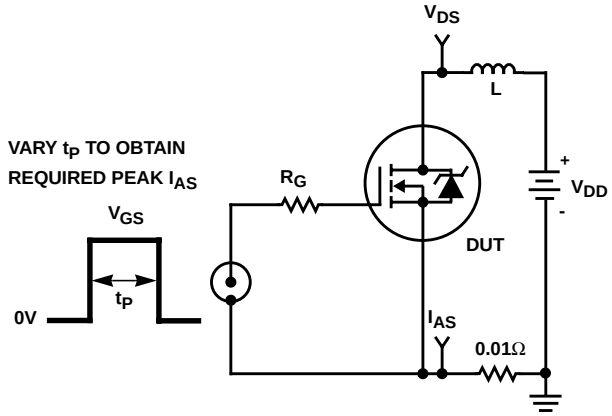


FIGURE 17. UNCLAMPED ENERGY TEST CIRCUIT

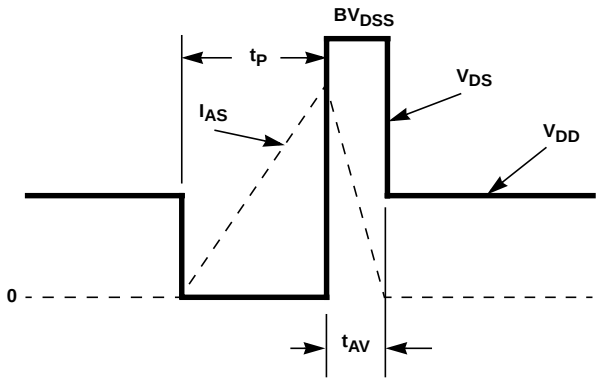


FIGURE 18. UNCLAMPED ENERGY WAVEFORM

Test Circuits and Waveforms (Continued)

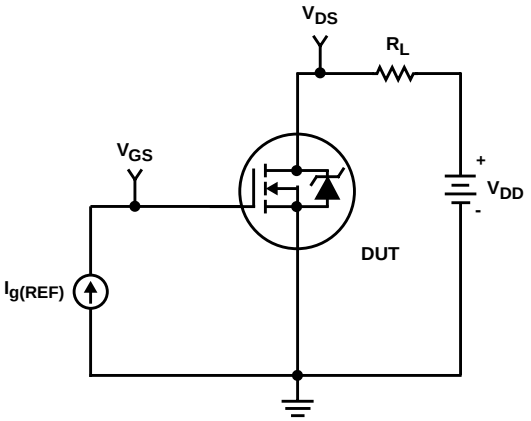


FIGURE 19. GATE CHARGE TEST CIRCUIT

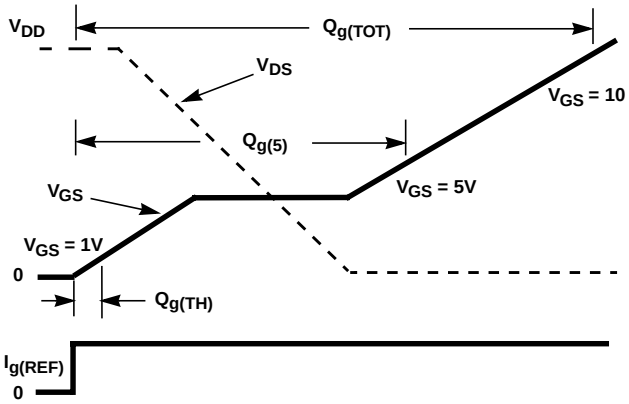


FIGURE 20. GATE CHARGE WAVEFORMS

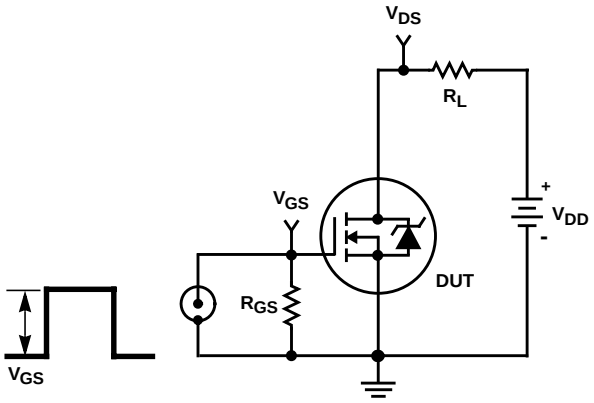


FIGURE 21. SWITCHING TIME TEST CIRCUIT

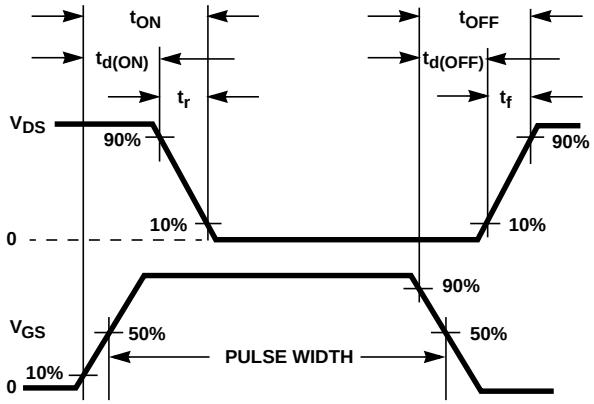


FIGURE 22. SWITCHING TIME WAVEFORMS

Thermal Resistance vs. Mounting Pad Area

The maximum rated junction temperature, T_{JM}, and the thermal resistance of the heat dissipating path determines the maximum allowable device power dissipation, P_{DM}, in an application. Therefore the application's ambient temperature, T_A (^oC), and thermal resistance $R_{\theta JA}$ ($^oC/W$) must be reviewed to ensure that T_{JM} is never exceeded. Equation 1 mathematically represents the relationship and serves as the basis for establishing the rating of the part.

$$P_{DM} = \frac{(T_{JM} - T_A)}{Z_{\theta JA}} \quad \text{(EQ. 1)}$$

In using surface mount devices such as the SOP-8 package, the environment in which it is applied will have a significant influence on the part's current and maximum power dissipation ratings. Precise determination of P_{DM} is complex and influenced by many factors:

1. Mounting pad area onto which the device is attached and whether there is copper on one side or both sides of the board
2. The number of copper layers and the thickness of the board
3. The use of external heat sinks
4. The use of thermal vias
5. Air flow and board orientation
6. For non-steady state applications, the pulse width, the duty cycle and the transient thermal response of the part, the board and the environment they are in

Intersil provides thermal information to assist the designer's preliminary application evaluation. Figure 23 defines the $R_{\theta JA}$ for the device as a function of the top copper (component side) area. This is for a horizontally positioned FR-4 board with 1oz copper after 1000 seconds of steady state power with no air flow. This graph provides the necessary information for calculation of the steady state junction temperature or power dissipation. Pulse applications can be evaluated using the Intersil device Spice thermal model or manually utilizing the normalized maximum transient thermal impedance curve.

Displayed on the curve are $R_{\theta JA}$ values listed in the Electrical Specifications table. The points were chosen to depict the compromise between the copper board area, the thermal resistance and ultimately the power dissipation, P_{DM}.

Thermal resistances corresponding to other copper areas can be obtained from Figure 23 or by calculation using Equation 2. $R_{\theta JA}$ is defined as the natural log of the area times a coefficient added to a constant. The area, in square inches is the top copper area including the gate and source pads.

$$R_{\theta JA} = 103.2 - 24.3 \times \ln(\text{Area}) \quad \text{(EQ. 2)}$$

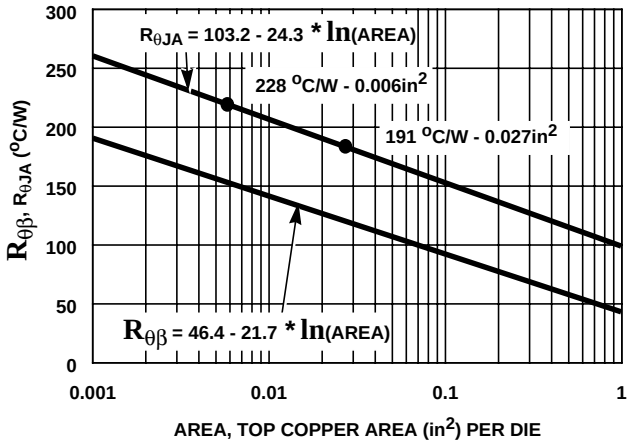


FIGURE 23. THERMAL RESISTANCE vs MOUNTING PAD AREA

While Equation 2 describes the thermal resistance of a single die, several of the new UltraFETs are offered with two die in the SOP-8 package. The dual die SOP-8 package introduces an additional thermal component, thermal coupling resistance, $R_{\theta\beta}$. Equation 3 describes $R_{\theta\beta}$ as a function of the top copper mounting pad area.

$$R_{\theta\beta} = 46.4 - 21.7 \times \ln(\text{Area}) \quad \text{(EQ. 3)}$$

The thermal coupling resistance vs. copper area is also graphically depicted in Figure 23. It is important to note the thermal resistance ($R_{\theta JA}$) and thermal coupling resistance ($R_{\theta\beta}$) are equivalent for both die. For example at 0.1 square inches of copper:

$R_{\theta JA1} = R_{\theta JA2} = 159^oC/W$

$R_{\theta\beta 1} = R_{\theta\beta 2} = 97^oC/W$

T_{J1} and T_{J2} define the junction temperature of the respective die. Similarly, P_1 and P_2 define the power dissipated in each die. The steady state junction temperature can be calculated using Equation 4 for die 1and Equation 5 for die 2.

Example: Use Equation 4 to calculate T_{J1} and Equation 5 to calculate T_{J2} with the following conditions. Die 2 is dissipating 0.5 Watts; die 1 is dissipating 0 Watts; the ambient temperature is 70^oC; the package is mounted to a top copper area of 0.1 square inches per die.

$$T_{J1} = P_1 R_{\theta JA} + P_2 R_{\theta\beta} + T_A \quad \text{(EQ. 4)}$$

$T_{J1} = (0 \text{ Watts})(159^oC/W) + (0.5 \text{ Watts})(97^oC/W) + 70^oC$

$T_{J1} = 119^oC$

$$T_{J2} = P_2 R_{\theta JA} + P_1 R_{\theta\beta} + T_A \quad \text{(EQ. 5)}$$

$T_{J2} = (0.5 \text{ Watts})(159^oC/W) + (0 \text{ Watts})(97^oC/W) + 70^oC$

$T_{J2} = 150^oC$

The transient thermal impedance ($Z_{\theta JA}$) is also effected by varied top copper board area. Figure 24 shows the effect of copper pad area on single pulse transient thermal impedance. Each trace represents a copper pad area in square inches corresponding to the descending list in the graph. SPICE and SABER thermal models are provided for each of the listed pad areas.

Copper pad area has no perceivable effect on transient thermal impedance for pulse widths less than 100ms. For pulse widths less than 100ms the transient thermal impedance is determined by the die and package. Therefore, CTHERM1 through CTHERM5 and RTHERM1 through RTHERM5 remain constant for each of the thermal models. A listing of the model component values is available in Table 1.

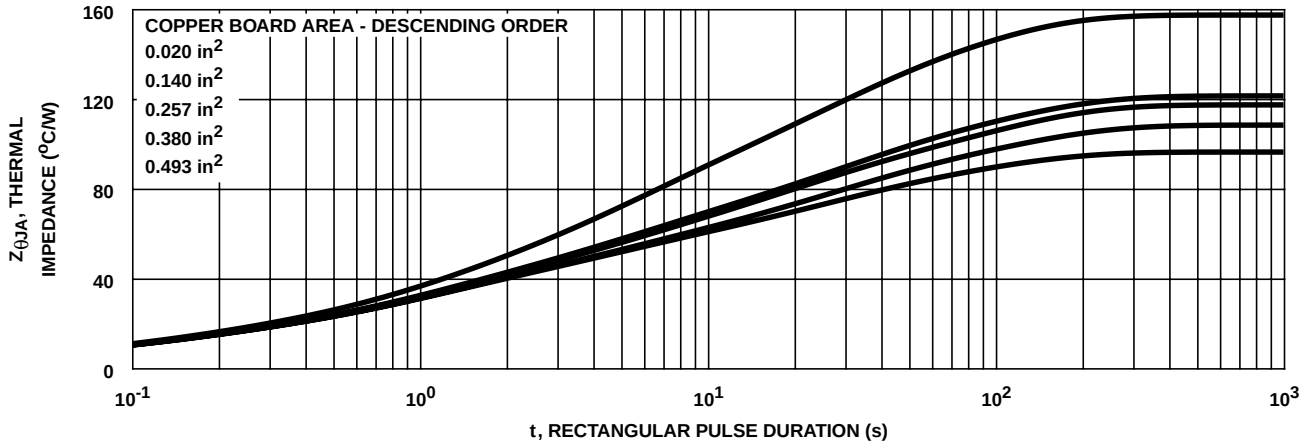


FIGURE 24. THERMAL RESISTANCE vs MOUNTING PAD AREA

SPICE Thermal Model

REV June 1998

HUF76105DK8

Copper Area = 0.02 in^2

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CTHERM1 th 8 8.5e-4
CTHERM2 8 7 1.8e-3
CTHERM3 7 6 5.0e-3
CTHERM4 6 5 1.3e-2
CTHERM5 5 4 4.0e-2
CTHERM6 4 3 9.0e-2
CTHERM7 3 2 4.0e-1
CTHERM8 2 tl 1.4

RTHERM1 th 8 3.5e-2
RTHERM2 8 7 6.0e-1
RTHERM3 7 6 2
RTHERM4 6 5 8
RTHERM5 5 4 18
RTHERM6 4 3 39
RTHERM7 3 2 42
RTHERM8 2 tl 48
```

SABER Thermal Model

Copper Area = 0.02 in^2

```
template thermal_model th tl
thermal_c th, tl
{
ctherm.ctherm1 th 8 = 8.5e-4
ctherm.ctherm2 8 7 = 1.8e-3
ctherm.ctherm3 7 6 = 5.0e-3
ctherm.ctherm4 6 5 = 1.3e-2
ctherm.ctherm5 5 4 = 4.0e-2
ctherm.ctherm6 4 3 = 9.0e-2
ctherm.ctherm7 3 2 = 4.0e-1
ctherm.ctherm8 2 tl = 1.4

rtherm.rtherm1 th 8 = 3.5e-2
rtherm.rtherm2 8 7 = 6.0e-1
rtherm.rtherm3 7 6 = 2
rtherm.rtherm4 6 5 = 8
rtherm.rtherm5 5 4 = 18
rtherm.rtherm6 4 3 = 39
rtherm.rtherm7 3 2 = 42
rtherm.rtherm8 2 tl = 48
}
```

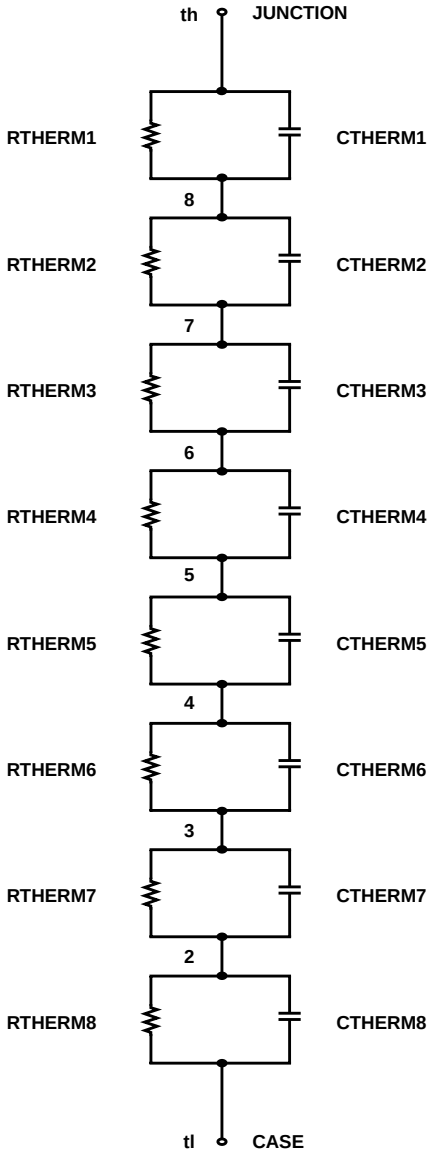


TABLE 1. THERMAL MODELS

COMPONENT	0.02 in^2	0.14 in^2	0.257 in^2	0.38 in^2	0.493 in^2
CTHERM6	9.0e-2	1.3e-1	1.5e-1	1.5e-1	1.5e-1
CTHERM7	4.0e-1	6.0e-1	4.5e-1	6.5e-1	7.5e-1
CTHERM8	1.4	2.5	2.2	3	3
RTHERM6	39	26	20	20	20
RTHERM7	42	32	31	29	23
RTHERM8	48	35	38	31	25

PSPICE Electrical Model

.SUBCKT HUF76105 2 1 3 ; REV June 1998

CA 12 8 4.95e-10
CB 15 14 5.15e-10
CIN 6 8 2.9e-10

DBODY 7 5 DBODYMOD
DBREAK 5 11 DBREAKMOD
DPLCAP 10 5 DPLCAPMOD

EBREAK 11 7 17 18 33.87
EDS 14 8 5 8 1
EGS 13 8 6 8 1
ESG 6 10 6 8 1
EVTHRES 6 21 19 8 1
EVTEMP 20 6 18 22 1

IT 8 17 1

LDRAIN 2 5 1e-9
LGATE 1 9 9.2e-10
LSOURCE 3 7 3.2e-10

MMED 16 6 8 8 MMEDMOD
MSTRO 16 6 8 8 MSTROMOD
MWEAK 16 21 8 8 MWEAKMOD

RBREAK 17 18 RBREAKMOD 1
RDRAIN 50 16 RDRAINMOD 9e-3
RGATE 9 20 3.39
RLDRAIN 2 5 10
RLGATE 1 9 9.2
RLSOURCE 3 7 3.2
RSLC1 5 51 RSLCMOD 1e-6
RSLC2 5 50 1e3
RSOURCE 8 7 RSOURCEMOD 22e-3
RVTHRES 22 8 RVTHRESMOD 1
RVTEMP 18 19 RVTEMPMOD 1

S1A 6 12 13 8 S1AMOD
S1B 13 12 13 8 S1BMOD
S2A 6 15 14 13 S2AMOD
S2B 13 15 14 13 S2BMOD

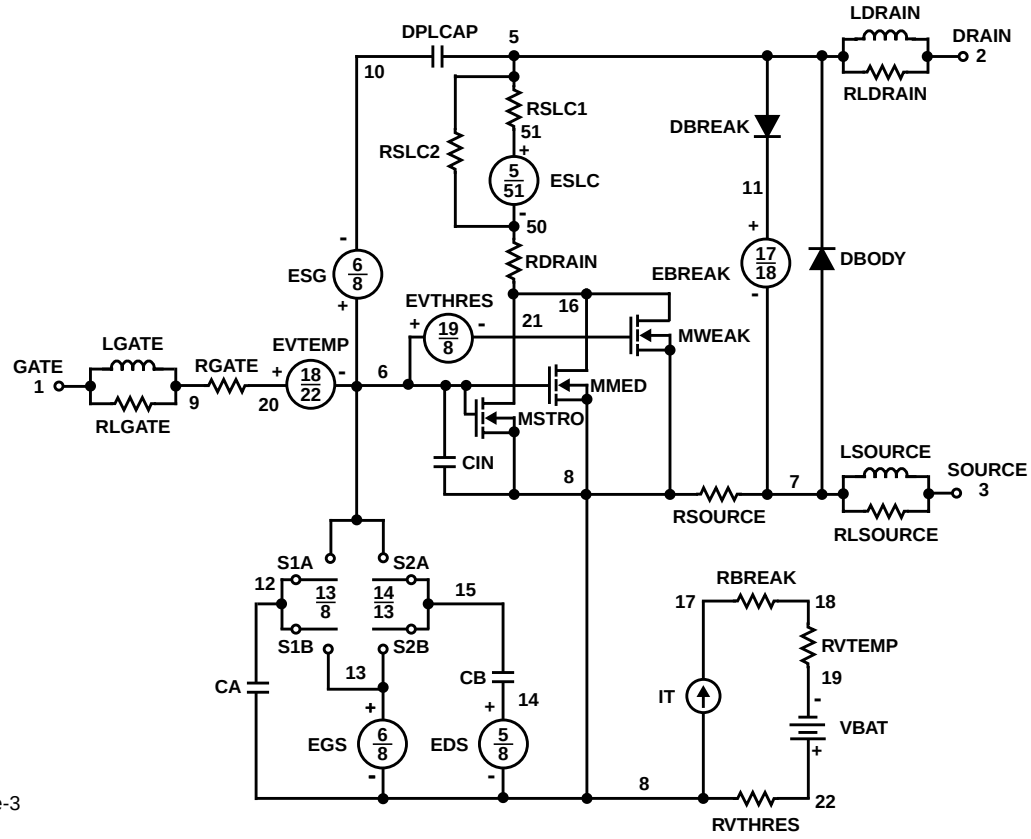
VBAT 22 19 DC 1

ESLC 51 50 VALUE={(V(5,51)/ABS(V(5,51)))*(PWR(V(5,51)/(1e-6*42),6))}

.MODEL DBODYMOD D (IS = 3.01e-13 IKF = 20 RS = 1.47e-2 TRS1 = -1.7e-3 TRS2 = 4e-5 CJO = 5.74e-10 TT = 2.88e-8 M = 0.43)
.MODEL DBREAKMOD D (RS = 3.94e-1 TRS1 = 9.94e-4 TRS2 = 9.12e-7)
.MODEL DPLCAPMOD D (CJO = 2.55e-10 IS = 1e-30 N = 10 M = 0.6)
.MODEL MMEDMOD NMOS (VTO = 1.92 KP = 2.1 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 3.39)
.MODEL MSTROMOD NMOS (VTO = 2.26 KP = 19 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u)
.MODEL MWEAKMOD NMOS (VTO = 1.7 KP = 0.1 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 33.9 RS = 0.1)
.MODEL RBREAKMOD RES (TC1 = 9.94e-4 TC2 = 9.84e-8)
.MODEL RDRAINMOD RES (TC1 = 8e-3 TC2 = 5.3e-5)
.MODEL RSLCMOD RES (TC1 = 1.e-3 TC2 = -1e-6)
.MODEL RSOURCEMOD RES (TC1 = 1e-3 TC2 = 0)
.MODEL RVTHRESMOD RES (TC1 = -1.87e-3 TC2 = -1.2e-6)
.MODEL RVTEMPMOD RES (TC1 = -1.5e-3 TC2 = 1.7e-6)

.MODEL S1AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -6.2 VOFF= -2)
.MODEL S1BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -2 VOFF= -6.2)
.MODEL S2AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -0.5 VOFF= 0.5)
.MODEL S2BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 0.5 VOFF= -0.5)

.ENDS



NOTE: For further discussion of the PSPICE model, consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; IEEE Power Electronics Specialist Conference Records, 1991, written by William J. Hepp and C. Frank Wheatley.

SABER Electrical Model

REV June
1998

```
template huf76105 n2,n1,n3
electrical n2,n1,n3
{
var i iscl
d..model dbodymod =  (is = 3.01e-13, cjo = 5.74e-10, tt = 2.88e-8, xti = 4.5, m = 0.43)
d..model dbreakmod = ()
d..model dplcapmod =  (cjo = 2.55e-10, is = 1e-30, n = 10, m = 0.6)
m..model mmedmod = (type=_n, vto = 1.92, kp = 2.1, is = 1e-30, tox = 1)
m..model mstrongmod = (type=_n, vto = 2.26, kp = 19, is = 1e-30, tox = 1)
m..model mweakmod = (type=_n, vto = 1.7, kp = 0.1, is = 1e-30, tox = 1)
sw_vcsp..model s1amod =  (ron = 1e-5, roff = 0.1, von = -6.2, voff = -2)
sw_vcsp..model s1bmod =  (ron =1e-5, roff = 0.1, von = -2, voff = -6.2)
sw_vcsp..model s2amod =  (ron = 1e-5, roff = 0.1, von = -0.5, voff = 0.5)
sw_vcsp..model s2bmod =  (ron = 1e-5, roff = 0.1, von = 0.5, voff = -0.5)

c.ca n12 n8 = 4.95e-10
c.cb n15 n14 = 5.15e-10
c.cin n6 n8 = 2.9e-10

d.dbody n7 n71 = model=dbodymod
d.dbreak n72 n11 = model=dbreakmod
d.dplcap n10 n5 = model=dplcapmod

i.it n8 n17 = 1

l.ldrain n2 n5 = 1e-9
l.lgate n1 n9 = 9.2e-10
l.lsource n3 n7 = 3.2e-10

m.mmed n16 n6 n8 n8 = model=mmedmod, l=1u, w=1u
m.mstrong n16 n6 n8 n8 = model=mstrongmod, l=1u, w=1u
m.mweak n16 n21 n8 n8 = model=mweakmod, l=1u, w=1u

res.rbreak n17 n18  = 1, tc1 = 9.94e-4, tc2 = 9.84e-8
res.rdbody n71 n5 = 1.47e-2, tc1 = -1.7e-3, tc2 = 4e-5
res.rdbreak n72 n5 = 3.94e-1, tc1 = 9.94e-4, tc2 = 9.12e-7
res.rdrain n50 n16  = 9e-3, tc1 = 8e-3, tc2 = 5.3e-5
res.rgate n9 n20 = 3.39
res.rldrain n2 n5 = 10
res.rlgate n1 n9 = 9.2
res.rlsource n3 n7 = 3.2
res.rslc1 n5 n51  = 1e-6, tc1 = 1e-3, tc2 = 1e-6
res.rslc2 n5 n50 = 1e3
res.rsource n8 n7  = 22e-3, tc1 = 1e-3, tc2 = 0
res.rvtemp n18 n19  = 1, tc1 = -1.5e-3, tc2 = 1.7e-6
res.rvthres n22 n8  = 1, tc1 = -1.87e-3, tc2 = -1.2e-6

spe.ebreak n11 n7 n17 n18 = 33.87
spe.eds n14 n8 n5 n8 = 1
spe.egs n13 n8 n6 n8 = 1
spe.esg n6 n10 n6 n8 = 1
spe.evtemp n20 n6 n18 n22 = 1
spe.evthres n6 n21 n19 n8 = 1

sw_vcsp.s1a n6 n12 n13 n8 = model=s1amod
sw_vcsp.s1b n13 n12 n13 n8 = model=s1bmod
sw_vcsp.s2a n6 n15 n14 n13 = model=s2amod
sw_vcsp.s2b n13 n15 n14 n13 = model=s2bmod

v.vbat n22 n19 = dc=1

equations {
i (n51->n50) +=iscl
iscl: v(n51,n50) = ((v(n5,n51)/(1e-9+abs(v(n5,n51))))*((abs(v(n5,n51)*1e6/42))** 6))
}
}
```

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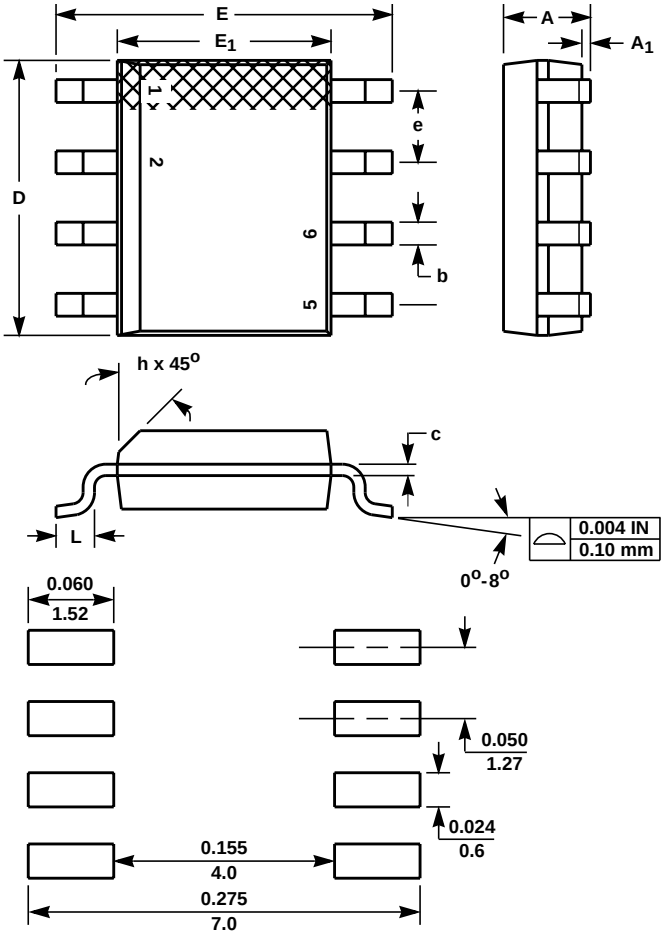
MS-012AA

8 LEAD JEDEC MS-012AA SMALL OUTLINE PLASTIC PACKAGE



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A_1	0.004	0.0098	0.10	0.25	-
b	0.013	0.020	0.33	0.51	-
c	0.0075	0.0098	0.19	0.25	-
D	0.189	0.1968	4.80	5.00	2
E	0.2284	0.244	5.80	6.20	-
E_1	0.1497	0.1574	3.80	4.00	3
e	0.050 BSC		1.27 BSC		-
H	0.0099	0.0196	0.25	0.50	-
L	0.016	0.050	0.40	1.27	4

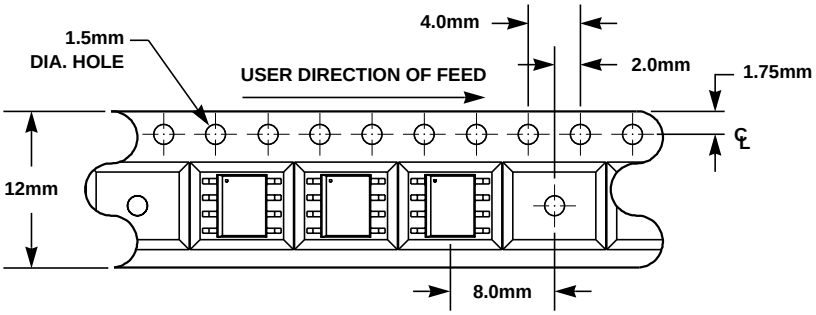
NOTES:

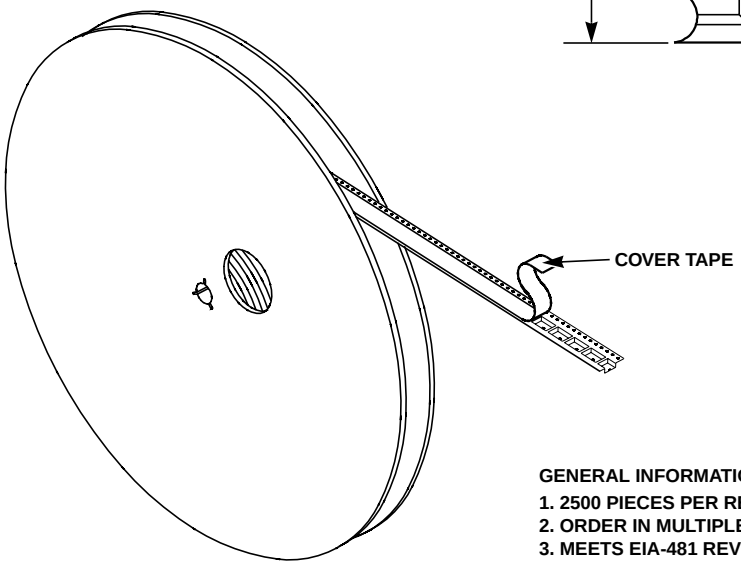
1. All dimensions are within allowable dimensions of Rev. C of JEDEC MS-012AA outline dated 5-90.
2. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.006 inches (0.15mm) per side.
3. Dimension “E_1” does not include inter-lead flash or protrusions. Inter-lead flash and protrusions shall not exceed 0.010 inches (0.25mm) per side.
4. “L” is the length of terminal for soldering.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. Controlling dimension: Millimeter.
7. Revision 8 dated 5-99.

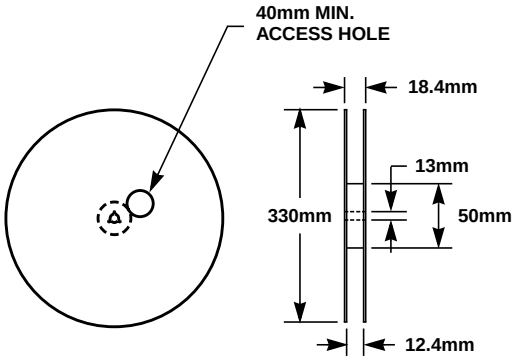
MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE-MOUNTED APPLICATIONS

MS-012AA

12mm TAPE AND REEL







GENERAL INFORMATION

1. 2500 PIECES PER REEL.
2. ORDER IN MULTIPLES OF FULL REELS ONLY.
3. MEETS EIA-481 REVISION “A” SPECIFICATIONS.