

Dual SPDT CMOS Analog Switch

The IH5043 analog switch uses an improved, high voltage CMOS monolithic technology. These devices provide ease of use and performance advantages not previously available from solid state switches.

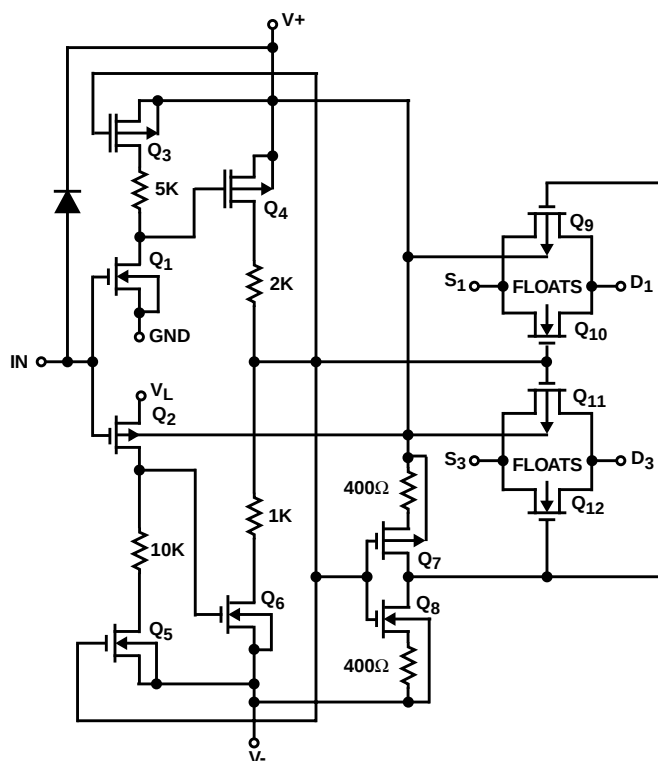
Key performance advantage is TTL compatibility and ultra low power operation. The quiescent current requirement is less than 1mA. Also, the IH5043 guarantees Break-Before-Make switching, accomplished by extending the t_{ON} time (300ns Typ), so that it exceeds t_{OFF} time (200ns Typ). This insures that an ON channel will be turned OFF before an OFF channel can turn ON. The need for external logic required to avoid channel to channel shorting during switching is eliminated.

Part Number Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
IH5043CPE	0 to 70	16 Ld PDIP	E16.3
IH5043CY	0 to 70	16 Ld SOIC	M16.15

Schematic Diagram

FUNCTIONAL DRIVER, TYPICAL DRIVER, GATE ($\frac{1}{2}$ AS SHOWN)

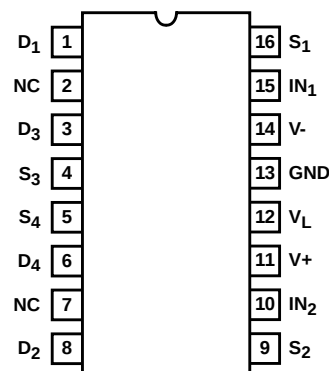


Features

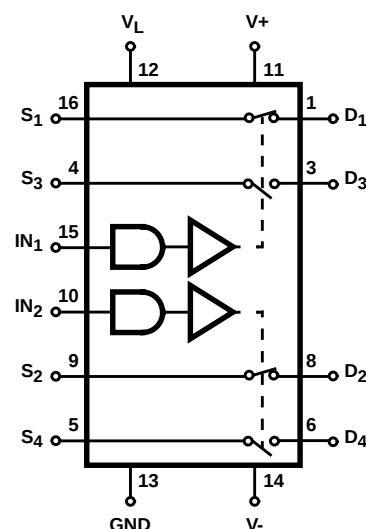
- See HI504X for Other Functions
- Dual SPDT
- Switches Greater than 20V_{P-P} Signals with $\pm 15V$ Supplies
- Quiescent Current Less than 1mA
- Break-Before-Make Switching t_{OFF} 200ns, t_{ON} 300ns (Typ)
- TTL, DTL, CMOS, PMOS Compatible

Pinout

**IH5043
(PDIP, SOIC)
TOP VIEW**



Functional Diagram



SWITCH STATES SHOWN ARE FOR LOGIC "1" INPUT

TRUTH TABLE

LOGIC	SWITCH 1, 2	SWITCH 3, 4
0	Off	On
1	On	Off

Absolute Maximum Ratings

V+ to V-	<36V
V+ to V _D	<30V
V _D to V-	<30V
V _D to V _S	<±22V
V _L to V-	<33V
V _L to V _{IN}	<30V
V _L to GND	<20V
V _{IN} to GND	<20V
Continuous Current (S-D)	30mA
Peak Current S-D (Pulsed 1ms, 10% Duty Cycle Max)	70mA

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)
PDIP Package	90
SOIC Package	115
Maximum Junction Temperature (Plastic Packages)	150°C
Maximum Storage Temperature	-65°C to 150°C
Maximum Lead Temperature (Soldering 10s)	300°C (SOIC - Lead Tips Only)

Operating Conditions

Temperature Range 0°C to 70°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications V+ = +15V, V- = -15V, V_L = +5V

PER CHANNEL PARAMETER	TEST CONDITIONS	(NOTES 2, 3)			UNITS
		0°C	25°C	70°C	
DYNAMIC CHARACTERISTICS					
Turn ON Time, t _{ON}	R _L = 1kΩ, V _{ANALOG} = -10V to +10V, See Figure 6	-	1000	-	ns
Turn OFF Time, t _{OFF}		-	500	-	ns
Charge Injection, Q	See Figure 7	-	20 (Typ)	-	mV
OFF Isolation, OIRR	f = 1MHz, R _L = 100Ω, C _L ≤ 5pF, See Figure 4	-	50 (Typ)	-	dB
Crosstalk, CCRR	One Channel Off; Any Other Channel Switches as per Figure 3	-	-50 (Typ)	-	dB
DIGITAL INPUT CHARACTERISTICS					
Input Logic Current, I _{IN(ON)}	V _{IN} = 2.4V	±1	±1	10	μA
Input Logic Current, I _{IN(OFF)}	V _{IN} = 0.8V	±1	±1	10	μA
ANALOG SWITCH CHARACTERISTICS					
Drain-Source ON Resistance, r _{DS(ON)}	I _S = 10mA, V _{ANALOG} = -10V to +10V	80	80	130	Ω
Channel-to-Channel r _{DS(ON)} Match, Δr _{DS(ON)}		-	30 (Typ)	-	Ω
Minimum Analog Signal Handling Capability, V _{ANALOG}		-	±10 (Typ)	-	V
Switch OFF Leakage Current, I _{D(OFF)} , I _{S(OFF)}	V _{ANALOG} = -10V to +10V	-	±5	100	nA
Switch ON Leakage Current, I _{D(ON)} +I _{S(ON)}	V _D = V _S = -10V to +10V	-	±10	100	nA
POWER SUPPLY CHARACTERISTICS					
+ Power Supply Quiescent Current, I ₊		10	10	100	μA
- Power Supply Quiescent Current, I ₋		10	10	100	μA
+5V Supply Quiescent Current, I _L		10	10	100	μA
Ground Quiescent Current, I _{GND}		10	10	100	μA

NOTES:

2. Typical values are for design aid only, not guaranteed and not subject to production testing.
3. Min or Max value unless otherwise specified.

Test Circuits and Waveforms

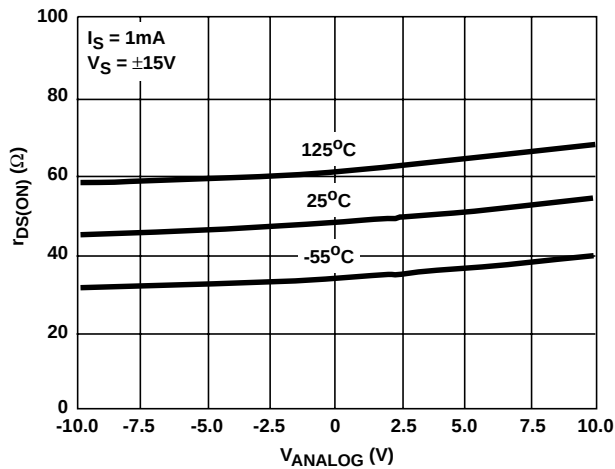
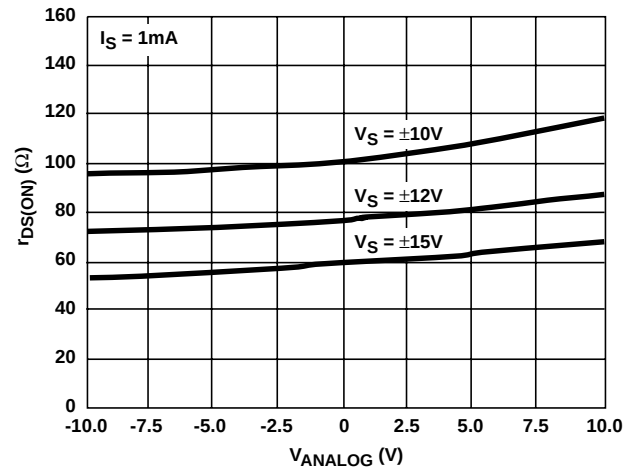
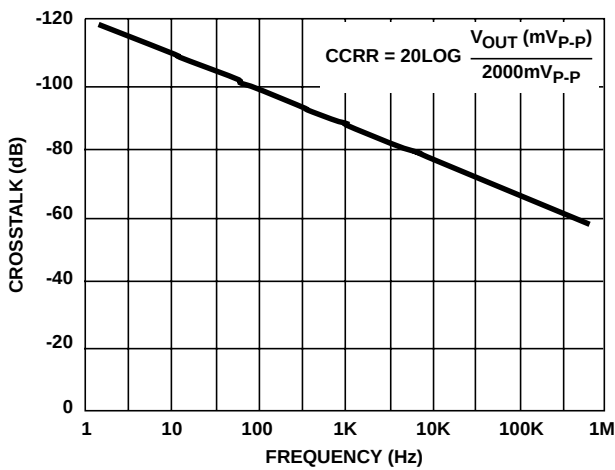
FIGURE 1. $r_{DS(ON)}$ vs ANALOG INPUT VOLTAGEFIGURE 2. $r_{DS(ON)}$ vs POWER SUPPLY VOLTAGE

FIGURE 3A. CROSSTALK vs FREQUENCY

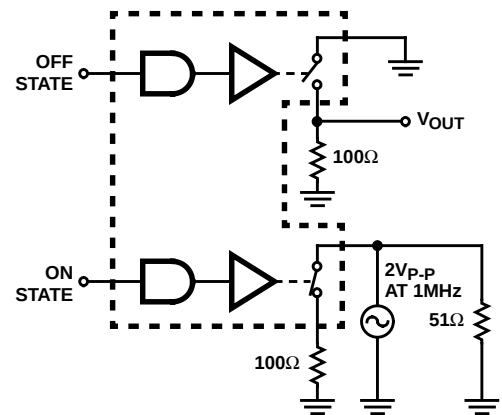


FIGURE 3B. TEST CIRCUIT

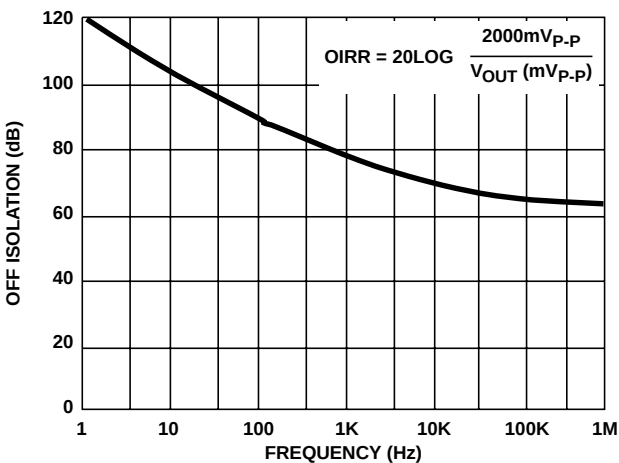


FIGURE 4A. OFF ISOLATION vs FREQUENCY

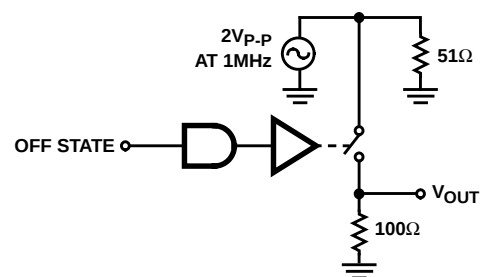


FIGURE 4B. TEST CIRCUIT

FIGURE 4. OFF ISOLATION

Test Circuits and Waveforms (Continued)

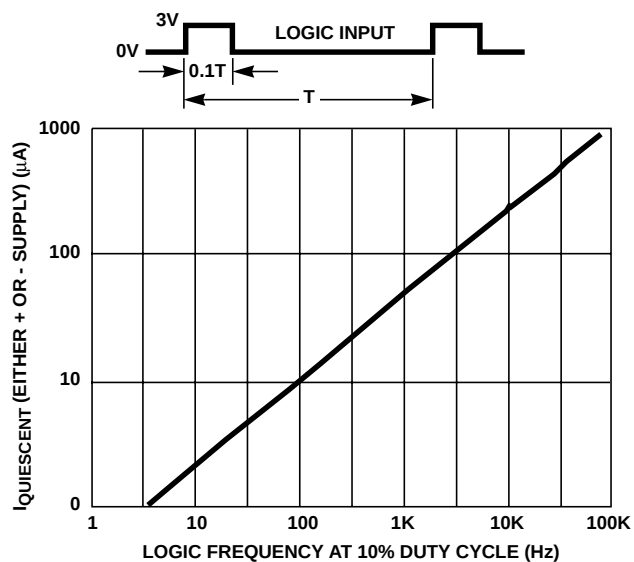


FIGURE 5. SUPPLY CURRENT vs LOGIC FREQUENCY

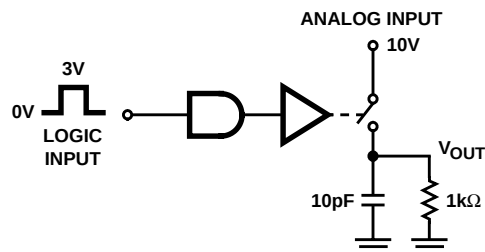
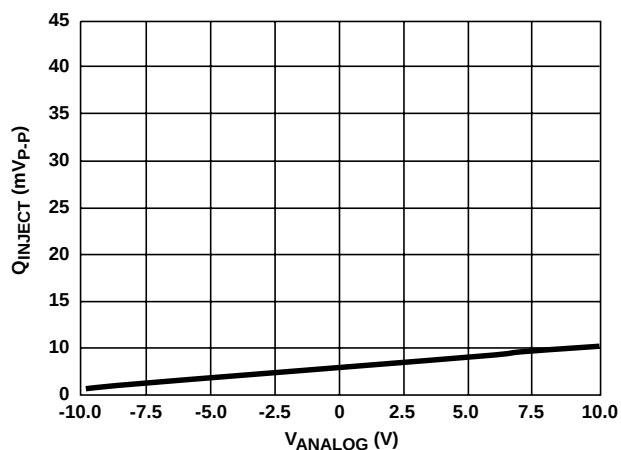
FIGURE 6. t_{ON} AND t_{OFF} TEST CIRCUIT

FIGURE 7A. CHARGE INJECTION vs ANALOG INPUT VOLTAGE

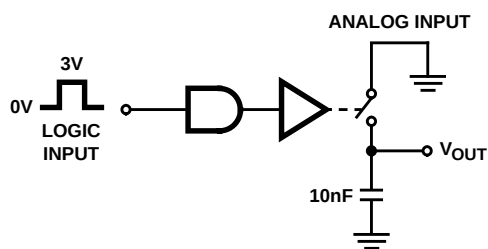


FIGURE 7B. TEST CIRCUIT

FIGURE 7. CHARGE INJECTION

Typical Applications

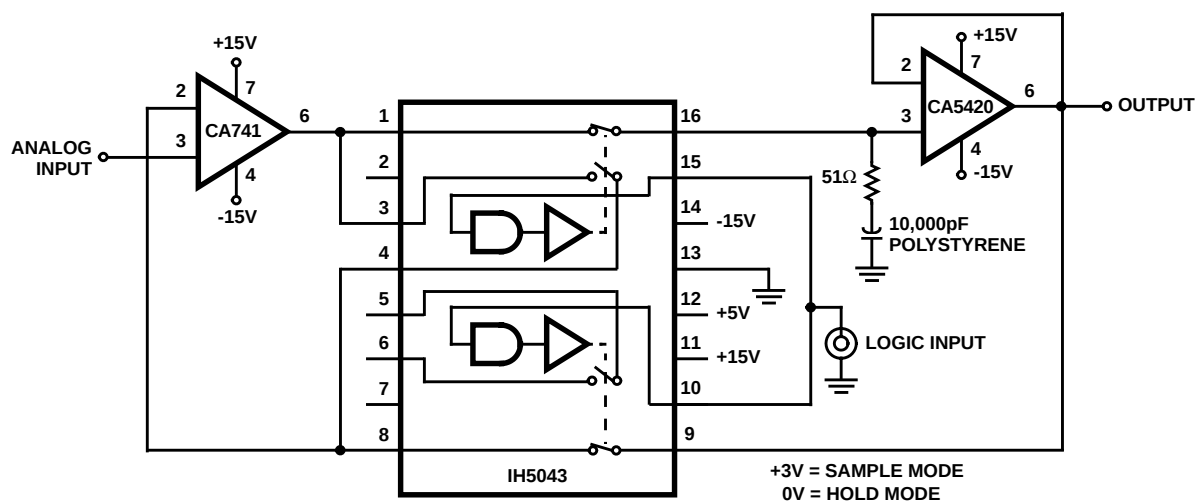


FIGURE 8. IMPROVED SAMPLE AND HOLD

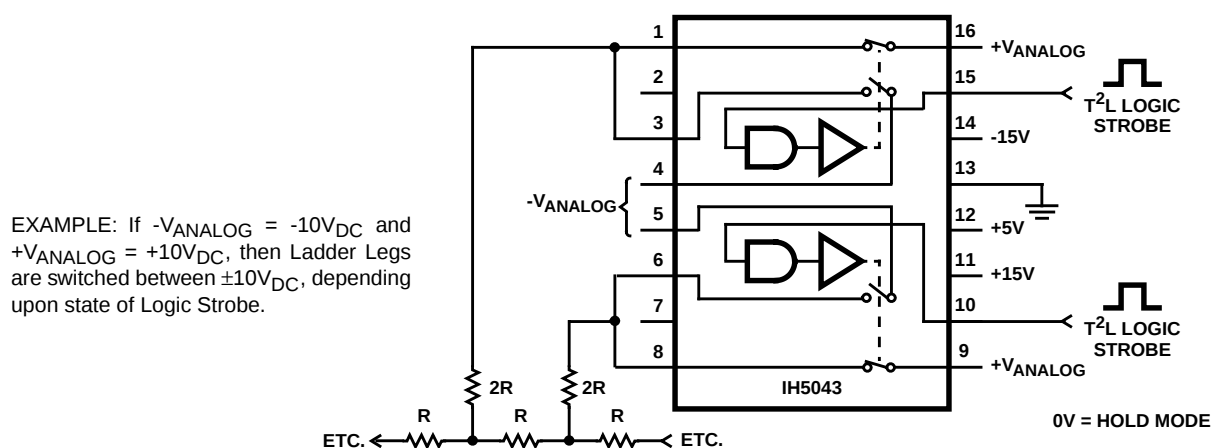


FIGURE 9. USING THE CMOS SWITCH TO DRIVE AN R/2R LADDER NETWORK (2 LEGS)

Typical Applications (Continued)

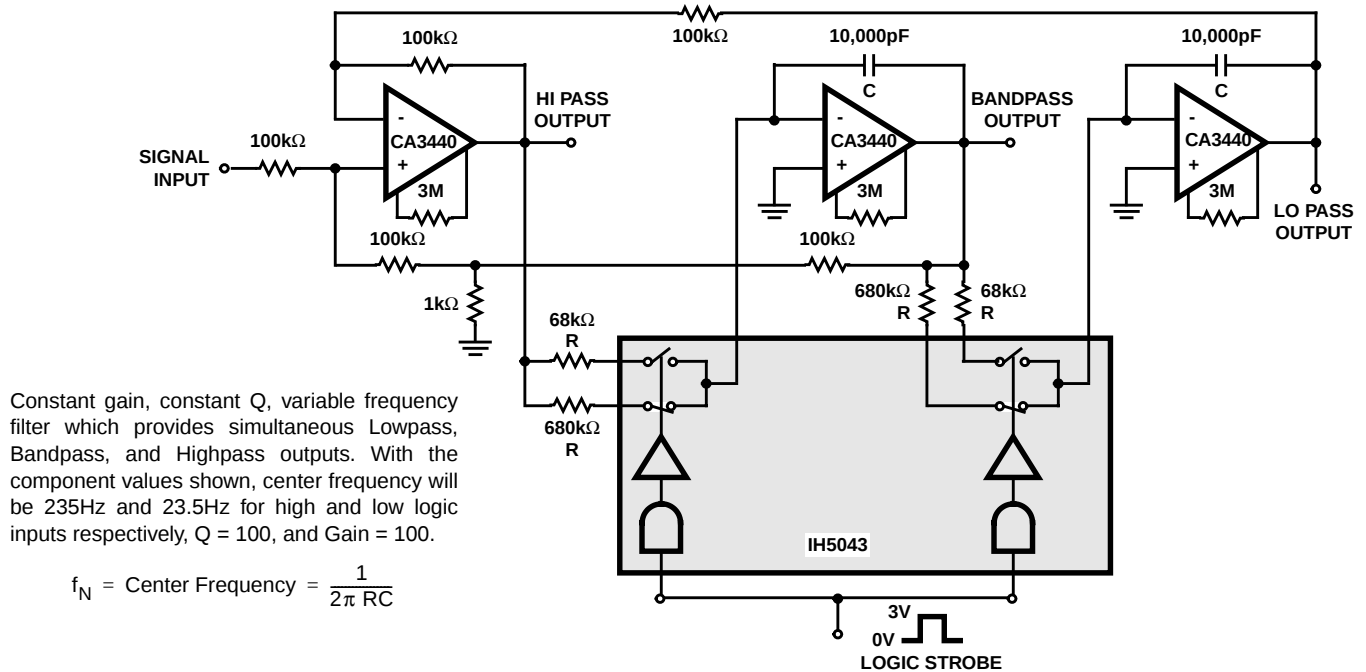


FIGURE 10. DIGITALLY TUNED LOW POWER ACTIVE FILTER

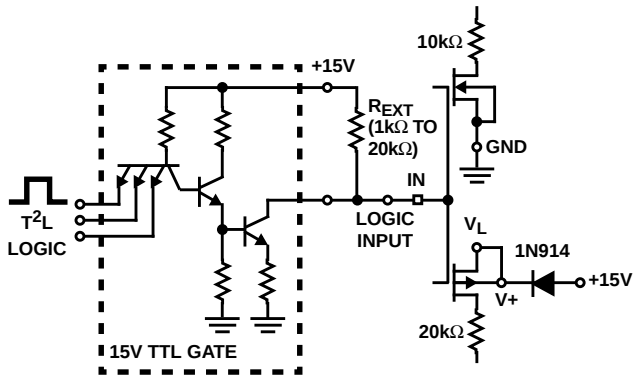


FIGURE 11. INTERFACING WITH TTL OPEN COLLECTOR LOGIC (TYP EXAMPLE FOR +15V CASE SHOWN)

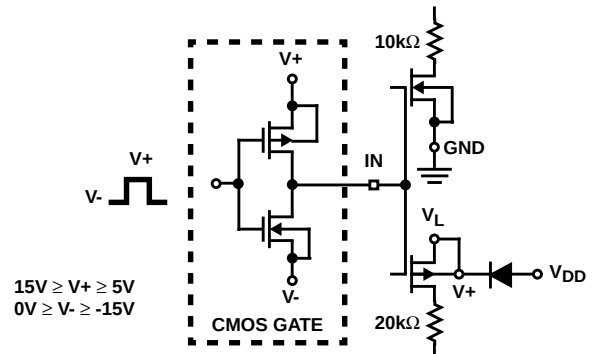


FIGURE 12. INTERFACING WITH CMOS LOGIC

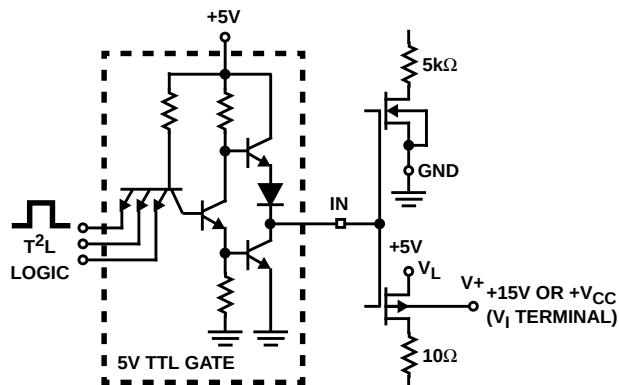


FIGURE 13. TTL LOGIC INTERFACE

Die Characteristics

DIE DIMENSIONS:

1778 μ m x 1905 μ m

METALLIZATION:

Type: Al

Thickness: 10k $\text{\AA}$ $\pm$ 1k $\text{\AA}$

PASSIVATION:

Type: PSG/Nitride

PSG Thickness: 7k $\text{\AA}$ $\pm$ 1.4k $\text{\AA}$

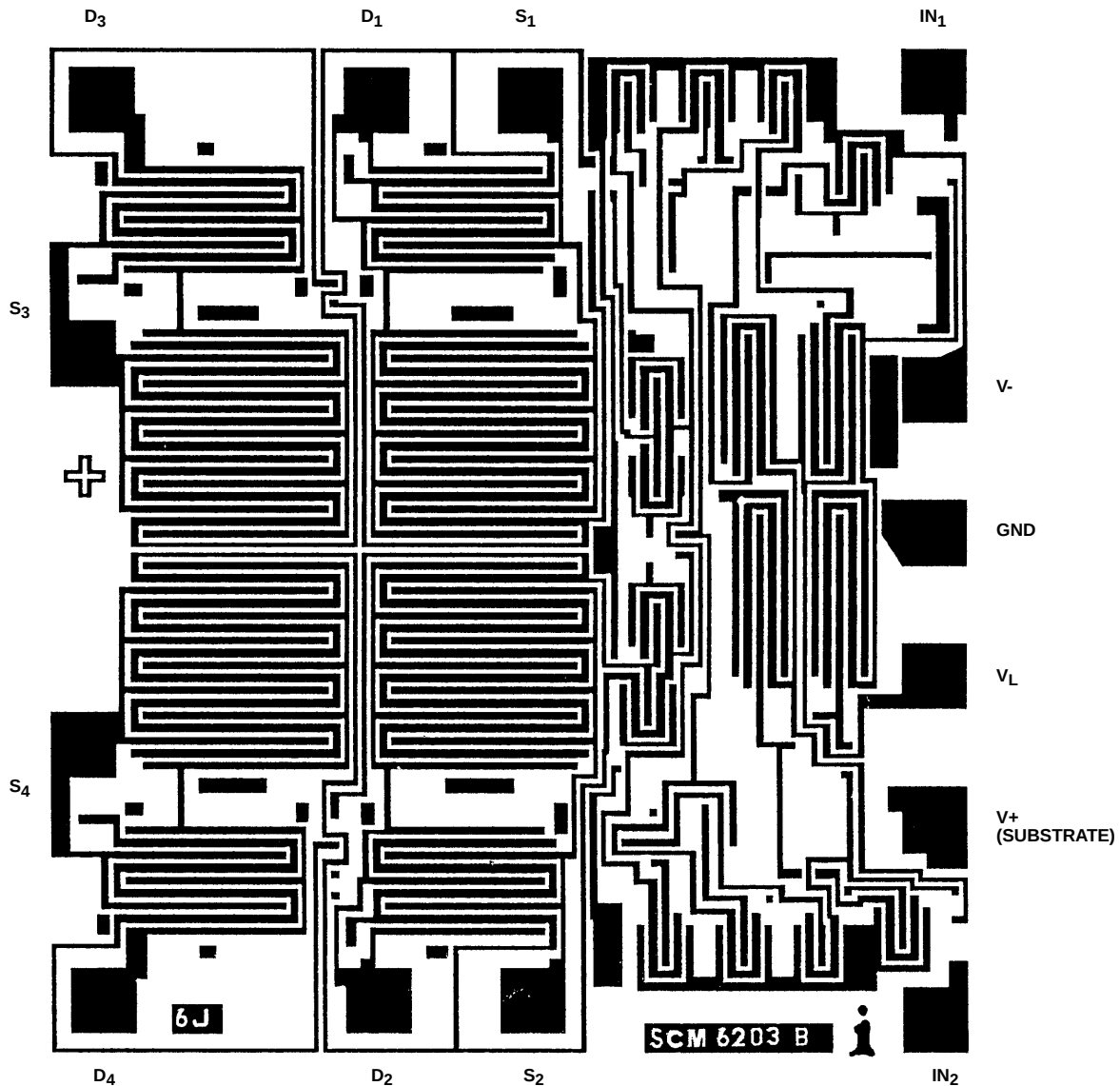
Nitride Thickness: 8k $\text{\AA}$ $\pm$ 1.2k $\text{\AA}$

WORST CASE CURRENT DENSITY:

9.1 x 10⁴ A/cm²

Metallization Mask Layout

IH5043



All Intersil semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.

Intersil semiconductor products are sold by description only. Intersil Corporation reserves the right to make changes in circuit design and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.

For information regarding Intersil Corporation and its products, see web site www.intersil.com