

October 1997

Features

- 4.0A and 5.0A, 150V and 200V
- $r_{DS(ON)} = 0.8\Omega$ and 1.2Ω
- SOA is Power Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device
- Related Literature
 - TB334 "Guidelines for Soldering Surface Mount Components to PC Boards"

Description

These are N-Channel enhancement mode silicon gate power field effect transistors. They are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high power bipolar switching transistors requiring high speed and low gate drive power. These types can be operated directly from integrated circuits.

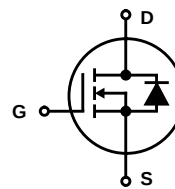
Formerly developmental type TA09600.

Ordering Information

PART NUMBER	PACKAGE	BRAND
IRF220	TO-204AA	IRF220
IRF221	TO-204AA	IRF221
IRF222	TO-204AA	IRF222
IRF223	TO-204AA	IRF223

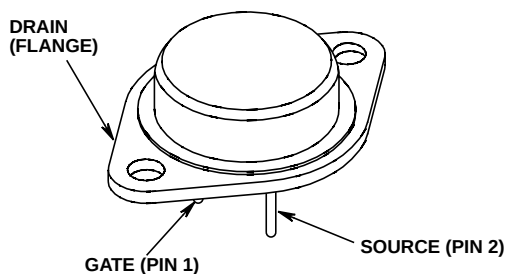
NOTE: When ordering, use the entire part number.

Symbol



Packaging

JEDEC TO-204AA



IRF220, IRF221, IRF222, IRF223

Absolute Maximum Ratings $T_C = 25^{\circ}\text{C}$, Unless Otherwise Specified

	IRF220	IRF221	IRF222	IRF223	UNITS
Drain to Source Voltage (Note 1) V_{DS}	200	150	200	150	V
Drain to Gate Voltage ($R_{GS} = 20\text{k}\Omega$) (Note 1) V_{DGR}	200	150	200	150	V
Continuous Drain Current I_D	5.0	5.0	4.0	4.0	A
$T_C = 100^{\circ}\text{C}$ I_D	3.0	3.0	2.5	2.5	A
Pulsed Drain Current (Note 3) I_{DM}	20	20	16	16	A
Gate to Source Voltage V_{GS}	± 20	± 20	± 20	± 20	V
Maximum Power Dissipation P_D	40	40	40	40	W
Linear Derating Factor	0.32	0.32	0.32	0.32	$\text{W}/^{\circ}\text{C}$
Single Pulse Avalanche Rating E_{AS}	85	85	85	85	mJ
Operating and Storage Temperature T_J, T_{STG}	-55 to 150	-55 to 150	-55 to 150	-55 to 150	$^{\circ}\text{C}$
Maximum Temperature for Soldering					
Leads at 0.063in (1.6mm) from Case for 10s T_L	300	300	300	300	$^{\circ}\text{C}$
Package Body for 10s, See Techbrief 334 T_{pkg}	260	260	260	260	$^{\circ}\text{C}$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

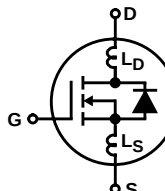
1. $T_J = 25^{\circ}\text{C}$ to 125°C .

Electrical Specifications $T_C = 25^{\circ}\text{C}$, Unless Otherwise Specified

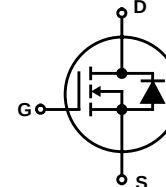
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV_{DSS}	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}$, (Figure 10)	200	-	-	V
IRF220, IRF222						
IRF221, IRF223						
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$	2.0	-	4.0	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = \text{Rated } BV_{DSS}, V_{GS} = 0\text{V}$	-	-	25	μA
		$V_{DS} = 0.8 \times \text{Rated } BV_{DSS}, V_{GS} = 0\text{V}, T_J = 125^{\circ}\text{C}$	-	-	250	μA
On-State Drain Current (Note 2)	$I_{D(ON)}$	$V_{DS} > I_{D(ON)} \times r_{DS(ON)MAX}, V_{GS} = 10\text{V}$	5.0	-	-	A
IRF220, IRF221						
IRF222, IRF223						
Gate to Source Leakage Current	I_{GSS}	$V_{GS} = \pm 20\text{V}$	-	-	± 100	nA
Drain to Source On Resistance (Note 2)	$r_{DS(ON)}$	$I_D = 2.5\text{A}, V_{GS} = 10\text{V}$, (Figure 8)	-	0.5	0.8	Ω
IRF220, IRF221						
IRF222, IRF223						
Forward Transconductance (Note 2)	g_{fs}	$V_{DS} > I_{D(ON)} \times r_{DS(ON)MAX}, I_D = 2.5\text{A}$	1.3	2.5	-	S
Turn-On Delay Time	$t_{d(ON)}$	$V_{DD} = 0.5 \times \text{Rated } BV_{DSS}, I_D \approx 2.5\text{A}, R_G = 50\Omega$ For IRF220, 222 $R_L = 80\Omega$ For IRF221, 223 $R_L = 60\Omega$ (Figures 17, 18) MOSFET Switching Times are Essentially Independent of Operating Temperature	-	20	40	ns
Rise Time	t_r		-	30	60	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	50	100	ns
Fall Time	t_f		-	30	60	ns
Total Gate Charge (Gate to Source + Gate to Drain)	$Q_{g(TOT)}$		-	11	15	nC
Gate to Source Charge	Q_{gs}	$V_{GS} = 10\text{V}, I_D = 6.0\text{A}, V_{DS} = 0.8 \times \text{Rated } BV_{DSS}$ $I_{g(REF)} = 1.5\text{mA}$, (Figures 14, 19, 20) Gate Charge is Essentially Independent of Operating Temperature	-	5.0	-	nC
Gate to Drain "Miller" Charge	Q_{gd}		-	6.0	-	nC

IRF220, IRF221, IRF222, IRF223

Electrical Specifications $T_C = 25^\circ\text{C}$, Unless Otherwise Specified (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Input Capacitance	C _{ISS}	V _{DS} = 25V, V _{GS} = 0V, f = 1MHz (Figure 11)		-	450	-	pF
Output Capacitance	C _{OSS}			-	150	-	pF
Reverse Transfer Capacitance	C _{RSS}			-	40	-	pF
Internal Drain Inductance	L _D	Measured Between the Contact Screw on the Flange that is Closer to Source and Gate Pins and the Center of Die	Modified MOSFET Symbol Showing the Internal Device Inductances 	-	5.0	-	nH
Internal Source Inductance	L _S	Measured From the Source Lead, 6mm (0.25in) From the Flange and the Source Bonding Pad		-	12.5	-	nH
Thermal Resistance Junction to Case	R _{θJC}			-	-	3.12	°C/W
Thermal Resistance Junction to Ambient	R _{θJA}	Free Air Operation		-	-	30	°C/W

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS	
Continuous Source to Drain Current IRF220, IRF221	I _{SD}	Modified MOSFET Symbol Showing the Integral Reverse P-N Junction Rectifier		-	-	5.0	A	
IRF222, IRF223				-	-	4.0	A	
Pulse Source to Drain Current (Note 3) IRF220, IRF221	I _{SDM}			-	-	20	A	
IRF222, IRF223				-	-	16	A	
Source to Drain Diode Voltage (Note 2) IRF220, IRF221	V _{SD}			T _C = 25 ⁰ C, I _{SD} = 5.0A, V _{GS} = 0V, (Figure 13)	-	-	2.0	V
IRF222, IRF223				T _C = 25 ⁰ C, I _{SD} = 4.0A, V _{GS} = 0V, (Figure 13)	-	-	1.8	V
Reverse Recovery Time	t _{rr}	T _J = 150 ⁰ C, I _{SD} = 5.0A, dI _{SD} /dt = 100A/μs	-	350	-	ns		
Reverse Recovery Charge	Q _{RR}	T _J = 150 ⁰ C, I _{SD} = 5.0A, dI _{SD} /dt = 100A/μs	-	2.3	-	μC		

NOTES:

- Pulse test: pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$.
- Repetitive rating: pulse width limited by maximum junction temperature. See Transient Thermal Impedance curve (Figure 3).
- $V_{DD} = 10\text{V}$, starting $T_J = 25^\circ\text{C}$, $L = 6.18\text{mH}$, $R_G = 50\Omega$, peak $I_{AS} = 5\text{A}$. See Figures 15, 16.

Typical Performance Curves Unless Otherwise Specified

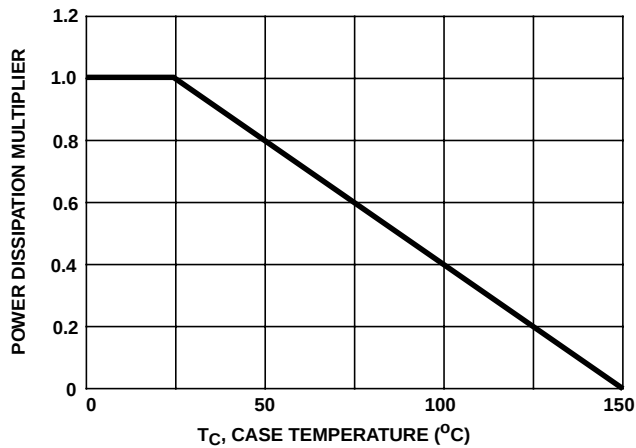


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

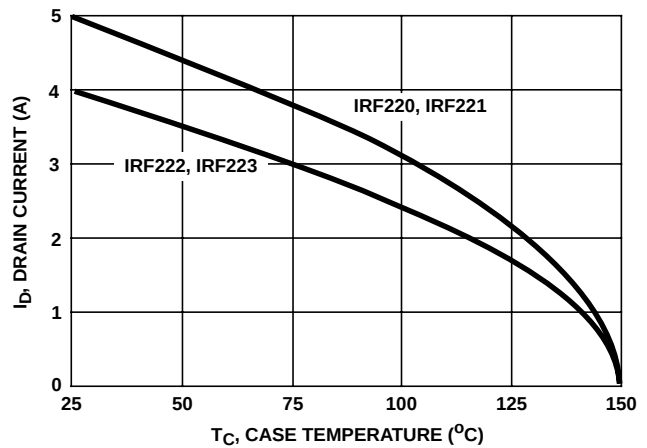


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

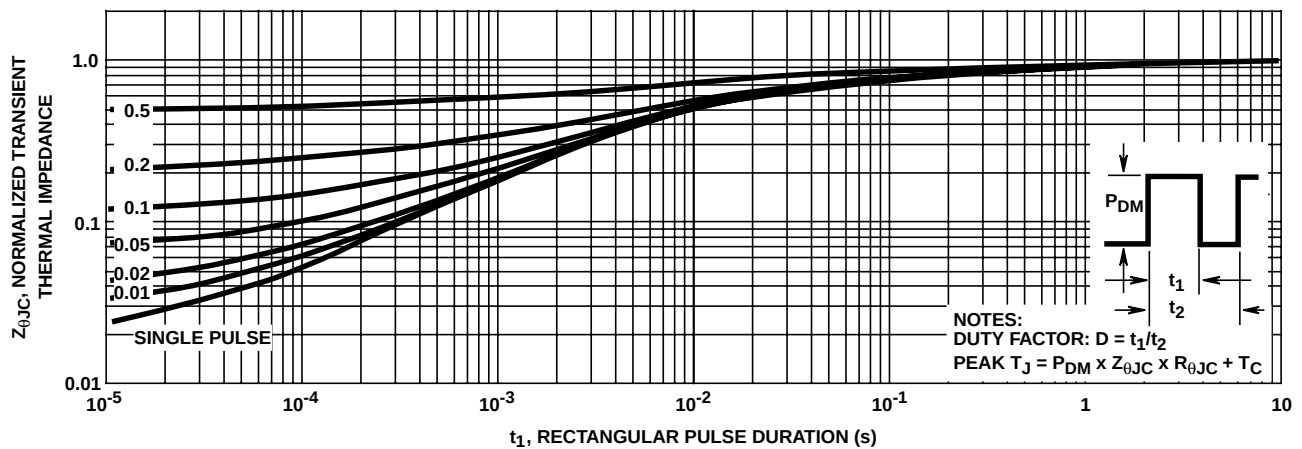


FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

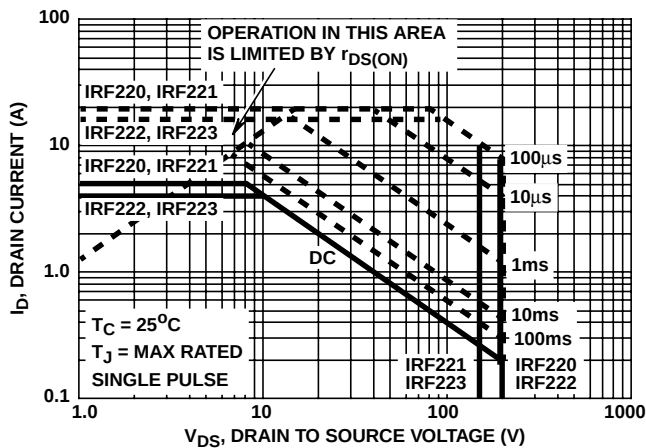


FIGURE 4. FORWARD BIAS SAFE OPERATING AREA

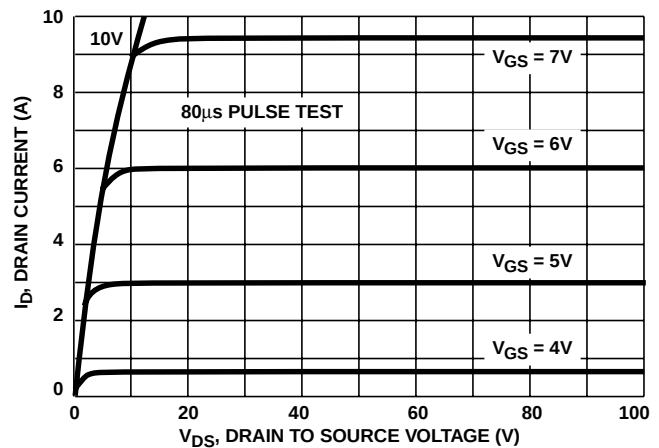


FIGURE 5. OUTPUT CHARACTERISTICS

Typical Performance Curves Unless Otherwise Specified (Continued)

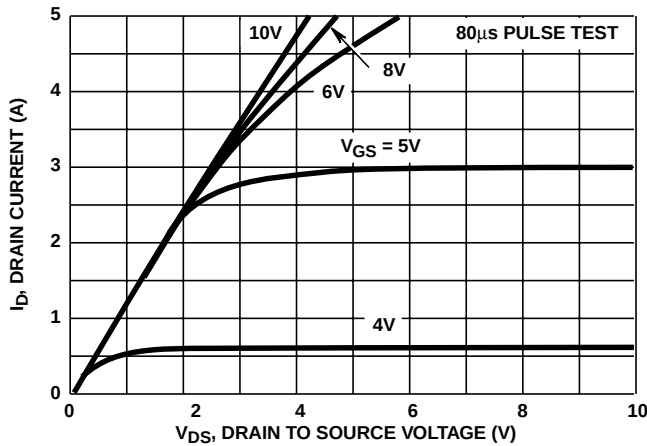


FIGURE 6. SATURATION CHARACTERISTICS

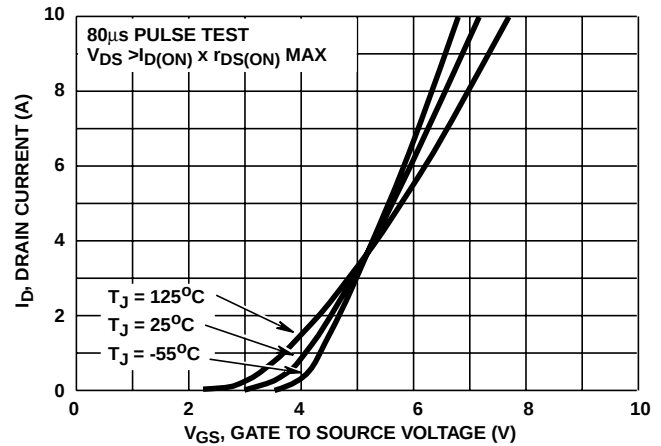
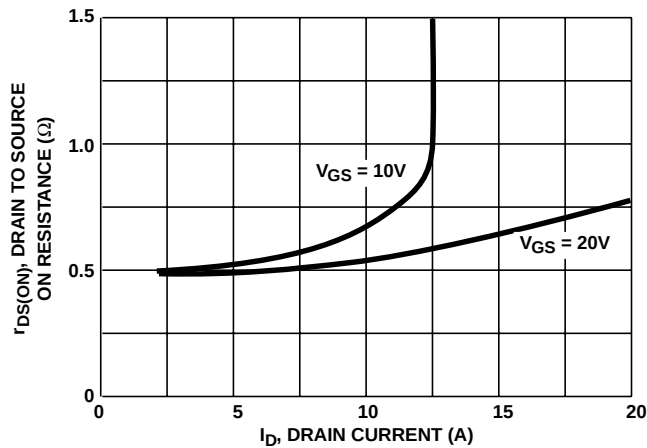


FIGURE 7. TRANSFER CHARACTERISTICS



NOTE: Heating effect of 2 μ s is minimal.

FIGURE 8. DRAIN TO SOURCE ON RESISTANCE vs GATE VOLTAGE AND DRAIN CURRENT

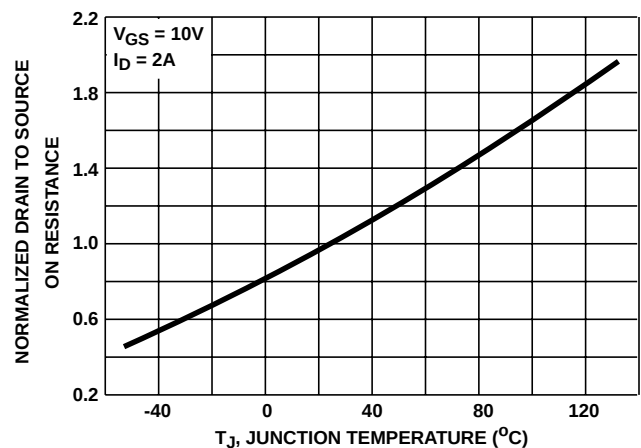


FIGURE 9. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

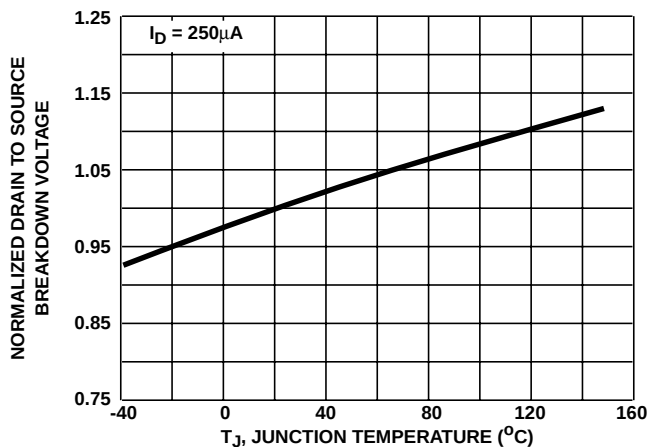


FIGURE 10. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

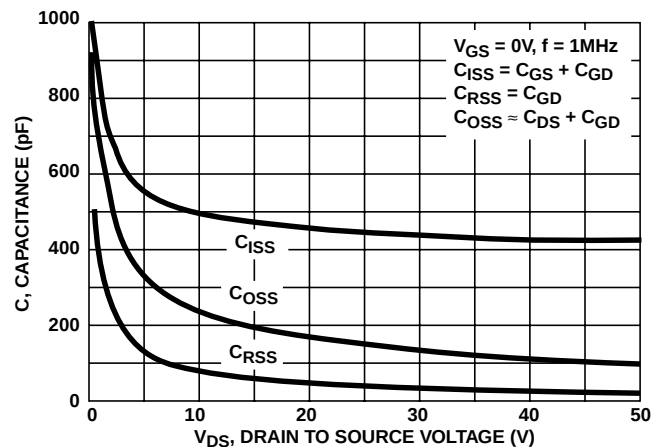


FIGURE 11. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE

Typical Performance Curves Unless Otherwise Specified (Continued)

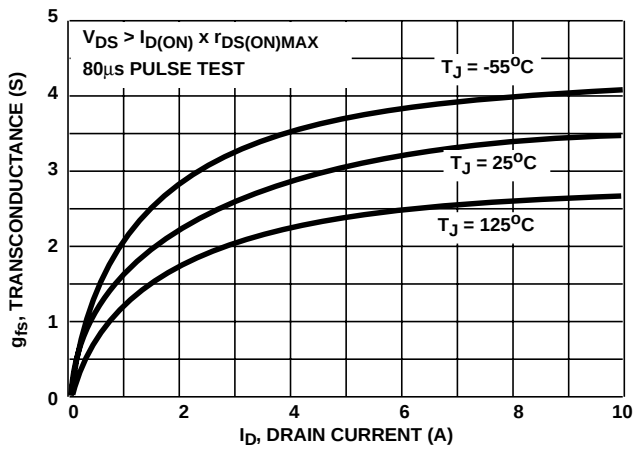


FIGURE 12. TRANSCONDUCTANCE vs DRAIN CURRENT

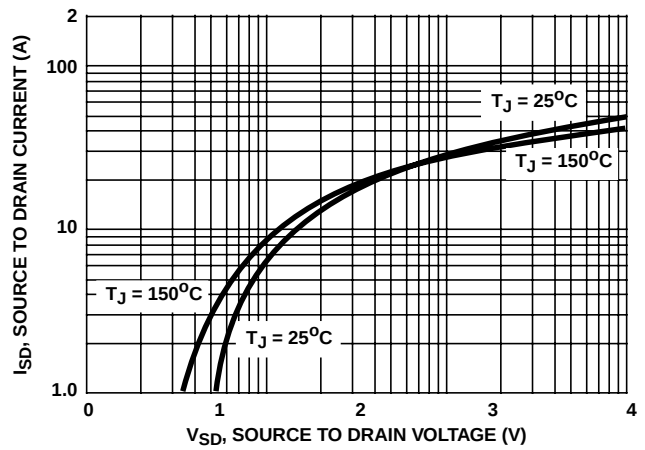


FIGURE 13. SOURCE TO DRAIN DIODE VOLTAGE

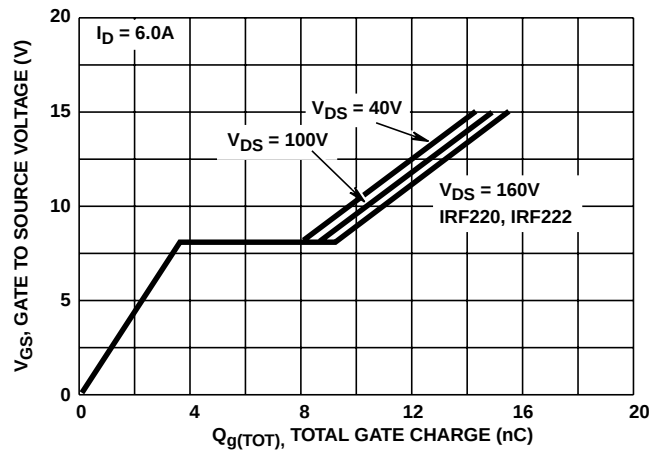


FIGURE 14. GATE TO SOURCE VOLTAGE vs GATE CHARGE

Test Circuits and Waveforms

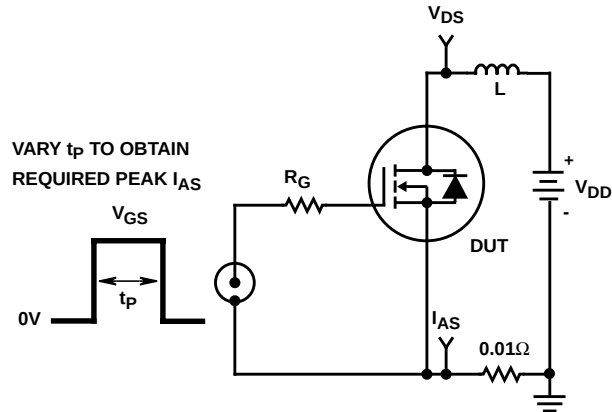


FIGURE 15. UNCLAMPED ENERGY TEST CIRCUIT

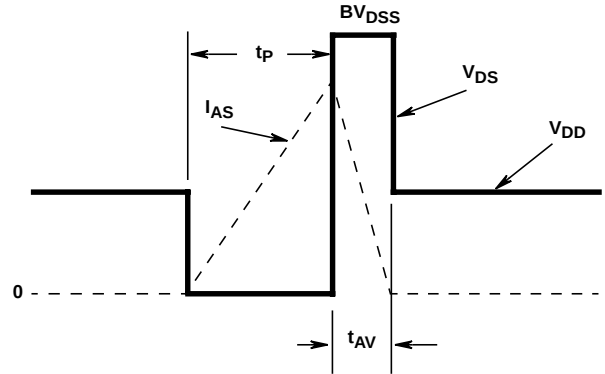


FIGURE 16. UNCLAMPED INDUCTIVE WAVEFORMS

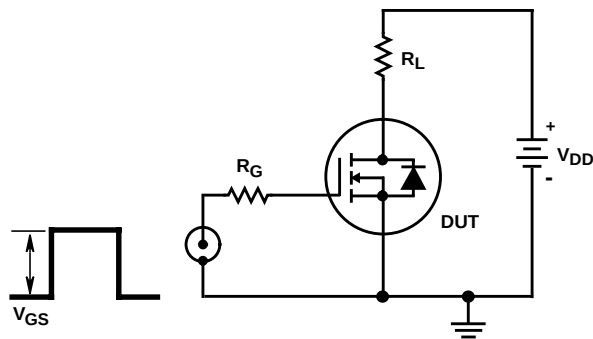


FIGURE 17. SWITCHING TIME TEST CIRCUIT

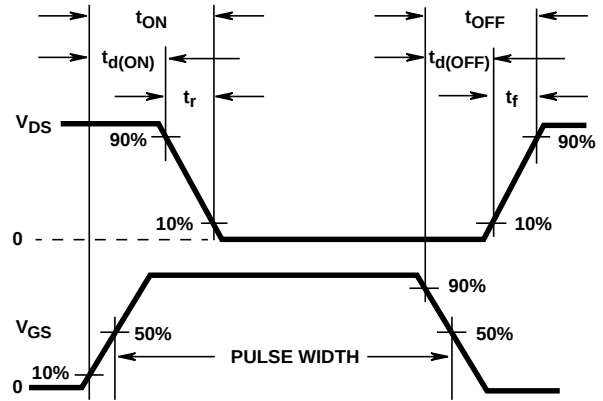


FIGURE 18. RESISTIVE SWITCHING WAVEFORMS

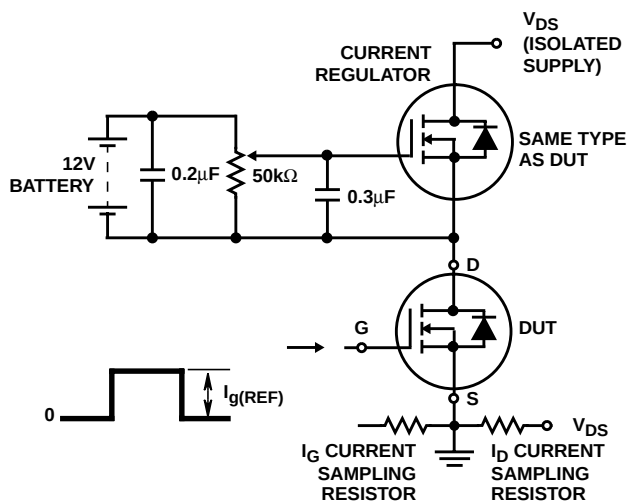


FIGURE 19. GATE CHARGE TEST CIRCUIT

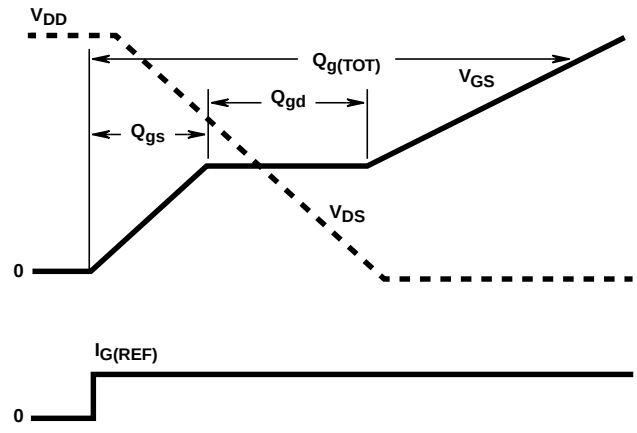


FIGURE 20. GATE CHARGE WAVEFORMS