J111-J113
N-Channel JFET Switch

INTERSIL

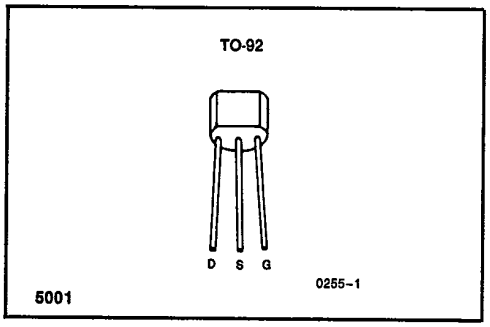
T-35-25

J111-J113

FEATURES
- Low Cost
- Automated Insertion Package
- Low Insertion Loss
- No Offset or Error Voltage Generated By Closed Switch
  - —Purely Resistive
  - —High Isolation Resistance From Driver
- Fast Switching
- Short Sample and Hold Aperture Time

APPLICATIONS
- Analog Switches
- Choppers
- Commutators

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted)

Gate-Drain or Gate-Source Voltage ..... −35V
Gate Current 50mA
Storage Temperature Range ..... −55°C to +150°C
Operating Temperature Range ..... −55°C to +135°C
Lead Temperature (Soldering, 10sec) ..... +300°C
Power Dissipation 360mW
Derate Above 25°C ..... 3.3mW/°C

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

ORDERING INFORMATION

TO-92
J111
J112
J113

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	J111			J112			J113			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{GSSR}	Gate Reverse Current (Note 1)	V_{DS}=0V, V_{GS}=−15V			−1			−1			−1	nA
$V_{GS(off)}$	Gate Source Cutoff Voltage	V_{DS}=5V, I_D=1μA	−3		−10	−1		−5	−0.5		−3	V
BV_{GSS}	Gate Source Breakdown Voltage	V_{DS}=0V, I_G=−1μA	−35			−35			−35			
I_{DSS}	Drain Saturation Current (Note 2)	V_{DS}=15V, V_{GS}=0V	20			5			2			mA
$I_{D(off)}$	Drain Cutoff Current (Note 1)	V_{DS}=5V, V_{GS}=−10V			1			1			1	nA
$r_{DS(on)}$	Drain Source ON Resistance	V_{DS}=0.1V, V_{GS}=0V			30			50			100	Ω
$C_{dg(off)}$	Drain Gate OFF Capacitance	V_{DS}=0V, V_{GS}=−10V (Note 3), f=1MHz			5			5			5	pF
$C_{sg(off)}$	Source Gate OFF Capacitance				5			5			5	
$C_{dg(on)}$ + $C_{sg(on)}$	Drain Gate Plus Source Gate ON Capacitance	V_{DS}=V_{GS}=0 (Note 3)			28			28			28	
$t_{d(on)}$	Turn On Delay Time	Switching Time-Test Conditions (Note 3)		7			7			7		ns
t_r	Rise Time			6			6			6		
$t_{d(off)}$	Turn Off Delay Time	V_{DD}: J111 10V, J112 10V, J113 10V; $V_{GS(off)}$: −12V, −7V, −5V; R_L: 0.8kΩ, 1.6kΩ, 3.2kΩ		20			20			20		
t_f	Fall Time			15			15			15		

NOTES: 1. Approximately doubles for every 10°C increase in T_A.
2. Pulse Test duration 300μs; duty cycle≤3%.
3. For design reference only, not 100% tested.

NOTE: All typical values have been characterized but are not tested.